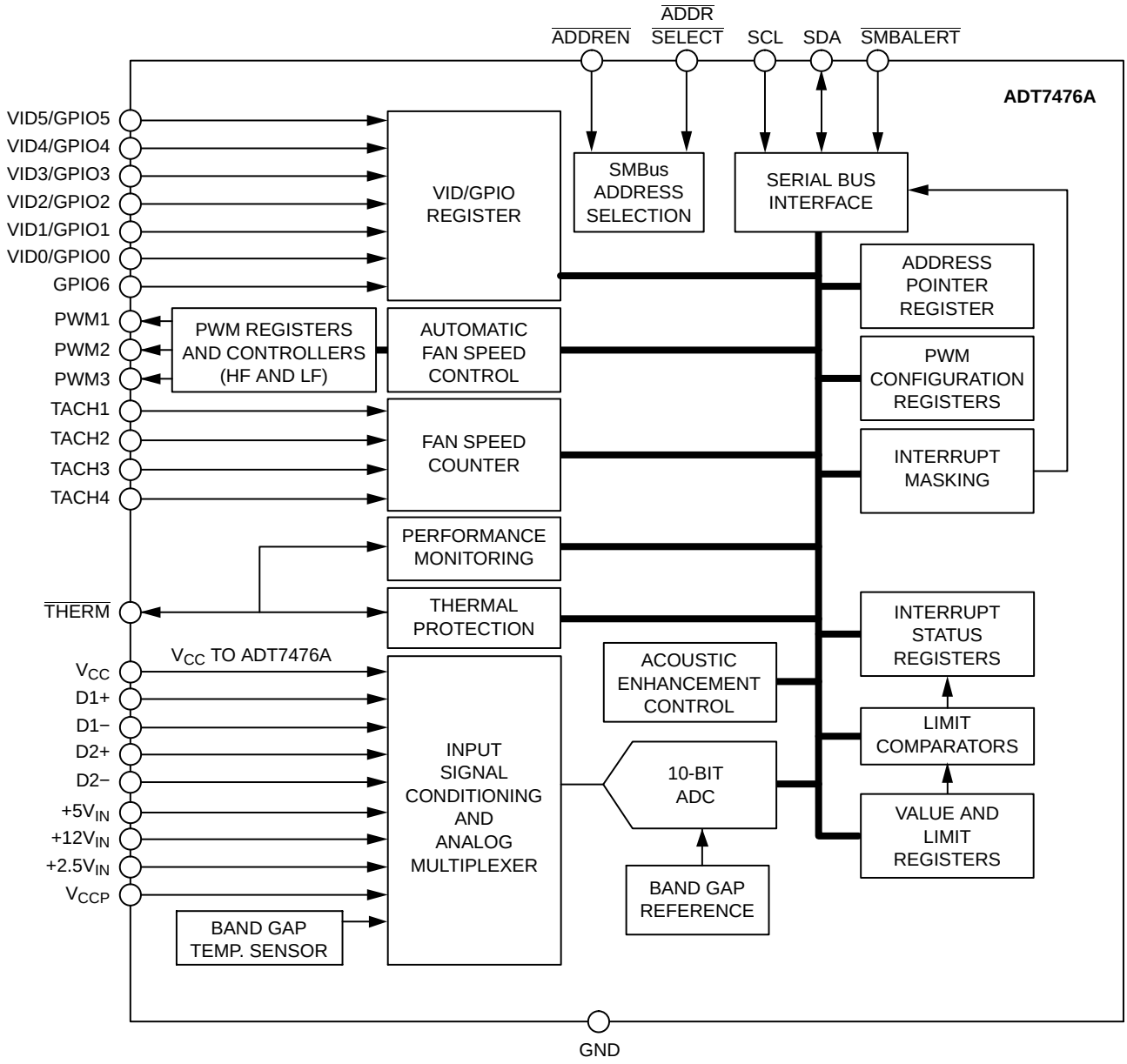

Figure 1. Functional Block Diagram

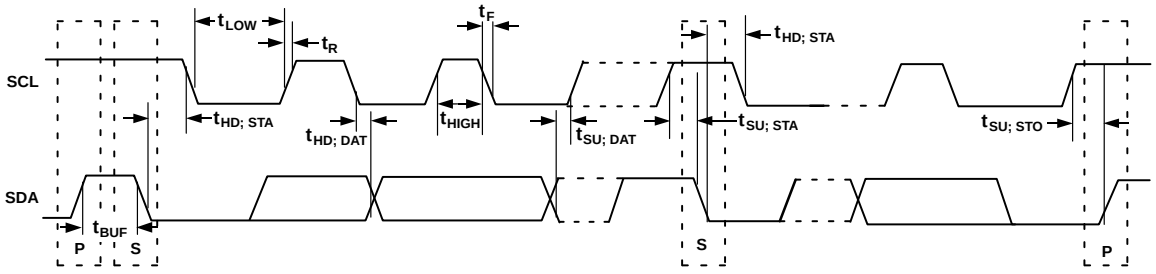

Figure 2. Serial Bus Timing Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Maximum Voltage on +12V_{IN} Pin	16	V
Maximum Voltage on +5.0V_{IN} Pin	6.25	V
Maximum Voltage on SDA, SCL, $\overline{\text{THERM}}$ (Pin 22) and GPIO1−5 Pins	3.6	V
Maximum Voltage on all Tach and PWM Pins	+5.5	V
Voltage on Remaining Input or Output Pins	−0.3 to +4.2	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Pb-Free Peak Temperature Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1,500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS (Note 1)

Package Type	θ_{JA}	θ_{JC}	Unit
24-lead QSOP	122	31.25	°C/W

1. $_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. ELECTRICAL CHARACTERISTICS

($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface Inactive, ADC Active		1.5	3.0	mA
Temperature-to-Digital Converter					
Local Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	− − −	±0.5 − 0.25	±1.5 ±2.5 −	°C
Remote Diode Sensor Accuracy Resolution	0°C ≤ T_A ≤ 85°C −40°C ≤ T_A ≤ 125°C	− − −	±0.5 − 0.25	±1.5 ±2.5 −	

Table 4. PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires SMBus pullup.
2	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
3	GND	Ground Pin.
4	V_{CC}	Power Supply. Powered by 3.3 V standby, if monitoring in low power states is required. V_{CC} is also monitored through this pin.
5	VID0/ GPIO0	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
6	VID1/ GPIO1	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
7	VID2/ GPIO2	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
8	VID3/ GPIO3	Digital Input. Voltage supply readouts from CPU. This value is read into the VID/GPIO register (0x43). General-Purpose Open Drain Digital I/O.
9	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
10	PWM2/ $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$

TYPICAL PERFORMANCE CHARACTERISTICS

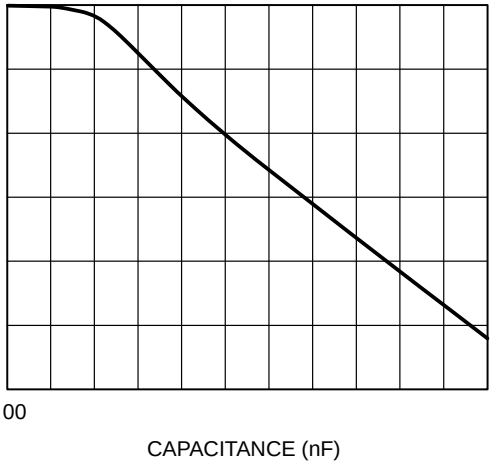

Figure 3. Temperature Error vs. Capacitance Between D+ and D−

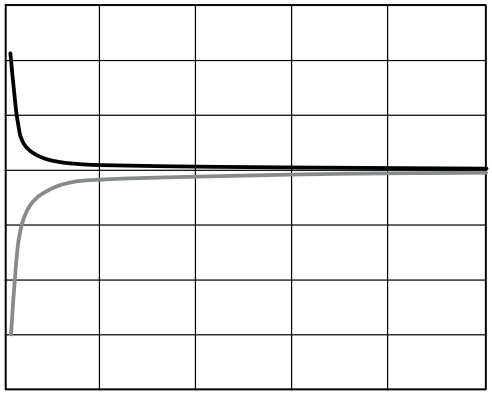

Figure 4. Remote Temperature Error vs. PCB Resistance

Figure 5. Remote Temperature Error vs. Common-Mode Noise Frequency

Figure 6. Remote Temperature Error vs. Differential-Mode Noise Frequency

Figure 7. Normal I_{DD} vs. Power Supply

Figure 8. Internal Temperature Error vs. Power Supply Noise

ADT7476A

Product Description

The ADT7476A is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7476A are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Feature Comparisons Between ADT7476A and ADT7468

- Dynamic T_{MIN}, dynamic operating point, and associated registers are no longer available in the ADT7476A. The following related registers are gone:
  - Calibration Control 1 (0x36)
  - Calibration Control 2 (0x37)
  - Operating Point (0x33, 0x34, and 0x35)
- Previously (in the ADT7468), T_{RANGE} defined the slope of the automatic fan control algorithm. T_{RANGE} now defines a true temperature range (in the ADT7476A).
- Acoustic filtering is now assigned to temperature zones, not to fans. Available smoothing times have been increased for better acoustic performance.
- Temperature measurements are now made with two switching currents instead of three. SRC is not available in the ADT7476A.
- High frequency PWM can now be enabled/disabled on each PWM output individually.
- $\overline{\text{THERM}}$ can now be enabled/disabled on each temperature channel individually.
- The ADT7476A does not support full shutdown mode.
- The ADT7476A offers increased temperature accuracy on all temperature channels.
- The ADT7476A defaults to twos complement temperature measurement mode.
- Some pins have swapped/added functions.
- The powerup routine for the ADT7476A is simplified.
- The ADT7476A has a higher maximum input voltage TACH/PWM spec, supporting a wider range of fans.
- $V_{CORE\_LOW\_ENABLE}$ has been reallocated to Bit 7 of Configuration Register 1 (0x40).

Recommended Implementation

Configuring the ADT7476A as shown in Figure 13 allows the system designer to use the following features:

- Two PWM outputs for fan control of up to three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 4.
- CPU temperature measured using Remote 1 temperature channel.
- Remote temperature zone measured through Remote 2 temperature channel.
- Local temperature zone measured through the internal temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. It can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

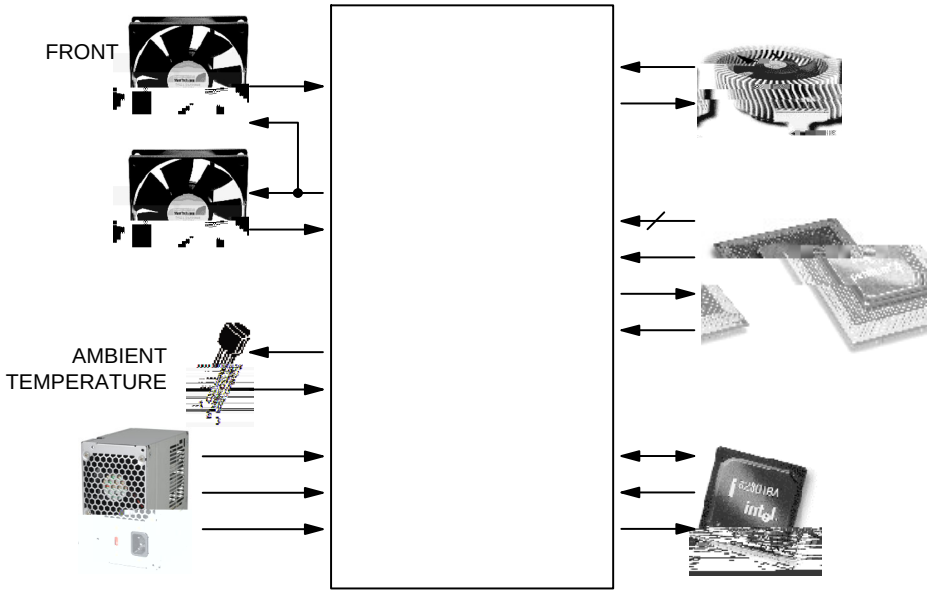

Figure 13. ADT7476A Configuration

Serial Bus Interface

Control of the ADT7476A is carried out using the serial system management bus (SMBus). The ADT7476A is connected to this bus as a slave device, under the control of a master controller. The ADT7476A has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/$\overline{\text{ADDREN}}$) high, the ADT7476A has a default SMBus address of 0101110 or 0x2E. The

clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as no acknowledge. The master then takes the data line low during the low period before the 10^{th} clock pulse, and then high during the 10^{th} clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. However, it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation. In the ADT7476A, write operations contain either one or two bytes, and read operations contain one byte.

To write data to one of the device data registers or read data from it, the address pointer register must be set so the correct data register is addressed. Then, data can be written into that register or read from it. The first byte of a write operation always contains an address stored in the address pointer register. If data is to be written to the device, then the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 18. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

When reading data from a register, there are two possibilities:

1. If the ADT7476A's address pointer register value is unknown, or not the desired value, then it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the ADT7476A as before, but only the data byte containing the register address is sent, because no data is written to the register (see Figure 19).
   A read operation is then performed consisting of the serial bus address; R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register (see Figure 20.)
2. If the address pointer register is already known to be at the desired address, data can be read from the

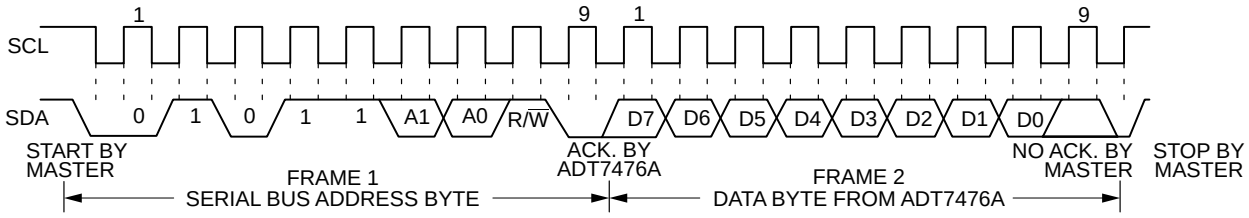

Figure 20. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7476A are discussed below. The following abbreviations are used in the diagrams:

- S – START
- P – STOP
- R – READ
- $\overline{W}$– WRITE
- A – ACKNOWLEDGE
- $\overline{A}$ – NO ACKNOWLEDGE

The ADT7476A uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7476A, the send byte protocol is used to write a register address to RAM for a subsequent single-byte read from the same address. This operation is illustrated in Figure 21.

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices, allowing an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of this device is now known and can be interrogated per usual.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7476A responds to the alert response address, the master must read the status registers, and $\overline{\text{SMBALERT}}$ is cleared only if the error condition goes away.

SMBus Timeout

The ADT7476A includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7476A assumes the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so if necessary, it can be disabled.

Table 6. CONFIGURATION REGISTER 1 (REG. 0x40)

Bit	Description
[6] TODIS	0: SMBus Timeout Enabled (Default) 1: SMBus Timeout Disabled

Virus Protection

To prevent rogue programs or viruses from accessing critical ADT7476A register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the ADT7476A is powered down and powered up again. For more information on which registers are locked see Table 49.

Voltage Measurement Input

The ADT7476A has four external voltage measurement channels. It can also measure its own supply voltage, V

ADT7476A

Table 13. 10-BIT ADC OUTPUT CODE VS. V_{IN}

Input Voltage	ADC Output

VID Code Monitoring

The ADT7476A has five dedicated voltage ID (VID code) inputs. These are digital inputs that can be read back through the VID/GPIO register (0x43) to determine the processor voltage required or the system being used. Five VID code inputs support VRM9.x solutions. In addition, Pin 21 (12 V input) can be reconfigured as a sixth VID input to satisfy future VRM requirements.

VID/GPIO Register (0x43)

[0] = VID0, reflects logic state of Pin 5.

[1] = VID1, reflects logic state of Pin 6.

[2] = VID2, reflects logic state of Pin 7.

[3] = VID3, reflects logic state of Pin 8.

[4] = VID4, reflects logic state of Pin 19.

[5] = VID5, reconfigurable 12 V input. This bit reads 0 when Pin 21 is configured as the 12 V input. This bit reflects the logic state of Pin 21 when the pin is configured as VID5.

VID Code Input Threshold Voltage

The switching threshold for the VID code inputs is approximately 1.0 V. To enable future compatibility, it is possible to reduce the VID code input threshold to 0.6 V. Bit 6 (THLD) of the VID/GPIO register (0x43) controls the VID input threshold voltage.

VID/GPIO Register (0x43)

[6] THLD = 0, VID switching threshold = 1 V,
V_{OL} < 0.8 V, V_{IH} > 1.7 V, V_{MAX} = 3.3 V.

[6] THLD = 1, VID switching threshold = 0.6 V,
V_{OL} < 0.4 V, V_{IH} > 0.8 V, V_{MAX} = 3.3 V.

Reconfiguring Pin 21 as VID5 Input

Pin 21 can be reconfigured as a sixth VID code input (VID5) for VRM10 compatible systems. Because the pin is configured as VID5, it is not possible to monitor a 12 V supply.

Bit 7 of the VID/GPIO register (0x43) determines the function of Pin 21. System or BIOS software can read the state of Bit 7 to determine whether the system is designed to monitor 12 V or a sixth VID input.

VID/GPIO Register (0x43)

[7] VIDSEL = 0, Pin 21 functions as a 12 V measurement input. Software can read this bit to determine that there are

Table 14. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)

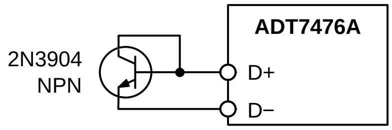

Figure 26. Measuring Temperature by Using an NPN Transistor

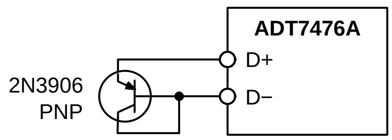

Figure 27. Measuring Temperature by Using an PNP Transistor

To measure ΔV_{BE}, the sensor switches between operating currents of I and N × I. The resulting waveform passes through a 65 kHz low-pass filter to remove noise and through a chopper-stabilized amplifier. The amplifier performs the amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

A remote temperature measurement takes nominally 38 ms. The results of remote temperature measurements are stored in 10-bit, twos complement format, as illustrated in Table 22. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice placed a capacitor across the D+ pin and the D− pin to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF.

This d-a2S9(b20T1905)TD-0)]TJ4 52[(the D)]collece od recba)]e

and null it out using the offset registers. The offset registers automatically add a twos complement 8-bit reading to every temperature measurement.

Changing Bit 1 of Configuration Register 5 (0x7C) changes the resolution and therefore, the range of the temperature offset as either having a −63°C to +127°C range with a resolution of 1°C or having a −63°C to +64°C range with a resolution of 0.5°C. This temperature offset can be used to compensate for linear temperature errors introduced by noise.

Table 16. TEMPERATURE OFFSET REGISTERS

Register	Description	Default
0x70	Remote 1 Temperature Offset	0x00 (0°C)
0x71	Local Temperature Offset	0x00 (0°C)
0x72	Remote 2 Temperature Offset	0x00 (0°C)

ADT7463/ADT7476A Backwards Compatible Mode

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7476A into single-channel ADC conversion mode. In this mode, the ADT7476A can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 27. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits have been programmed, the ADT7476A can be enabled for monitoring. The ADT7476A measures all voltage and temperature measurements in round robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round robin cycle. Comparisons are done differently depending on whether the measured value is being compared to a high or low limit.

High Limit: > Comparison Performed
Low Limit: ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). The ADC measures each analog input in turn, and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

- Four Dedicated Supply Voltage Inputs
- Supply Voltage (V_{CC} Pin)
- Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round robin conversions and takes 11 ms for each voltage measurement, 12 ms for a local temperature reading, and 39 ms for each remote temperature reading. The total monitoring cycle time for averaged voltage and temperature monitoring is, therefore, nominally:

$$(5 \times 11) + 12 + (2 \times 39) = 145 \text{ ms} \quad \text{(eq. 3)}$$

Table 30. INTERRUPT MASK REGISTER 1 (0x74)

Bit	Mnemonic	Description
[7]	OOL	1 masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Interrupt Status Register 2.
[6]	R2T	1 masks $\overline{\text{SMBALERT}}$ for Remote 2 temperature.
[5]	LT	1 masks $\overline{\text{SMBALERT}}$ for Local temperature.
[4]	R1T	1 masks $\overline{\text{SMBALERT}}$ for Remote 1 temperature.
[3]	5.0 V	1 masks $\overline{\text{SMBALERT}}$ for the 5.0 V channel.
[2]	V_{CC}	1 masks $\overline{\text{SMBALERT}}$ for the V_{CC} channel.
[1]	V_{CCP}	1 masks $\overline{\text{SMBALERT}}$ for the V_{CCP} channel.
[0]	2.5 V	1 masks $\overline{\text{SMBALERT}}$ for the 2.5 V_{IN}/THERM

THERM Timer

The ADT7476A has an internal timer to measure THERM assertion time. For example, the THERM input can be connected to the PROCHOT output of a Pentium® 4 CPU to measure system performance. The THERM input can also be connected to the output of a trip-point temperature sensor.

The timer is started on the assertion of the ADT7476A's THERM input and stopped when THERM is de-asserted. The timer counts THERM times cumulatively; that is, the timer resumes counting on the next THERM assertion. The THERM timer continues to accumulate THERM assertion times until the timer is read (where it is cleared), or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit THERM timer status register (0x79) is designed so that Bit 0 is set to 1 on the first THERM assertion. Once the cumulative THERM assertion time has exceeded 45.52 ms, Bit 1 of the THERM timer is set and Bit 0 now becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 32).

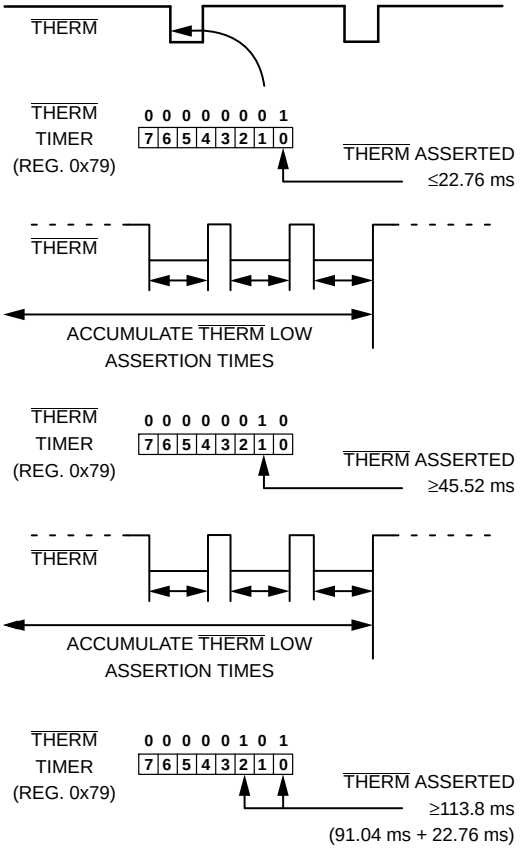

Figure 32. Understanding the THERM Timer

When using the THERM timer, be aware of the following:

After a THERM timer read (0x79)

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following occurs:

1. The contents of the timer are cleared.
2. Bit 0 of the THERM timer is set to 1, because a THERM assertion is occurring.
3. The THERM timer increments from zero.
4. If the THERM timer limit register (0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM

below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after $\overline{\text{THERM}}$ asserts, it is guaranteed to remain low for at least one monitoring cycle.

The $\overline{\text{THERM}}$ pin can be configured to assert low, if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bits [5:7] of Configuration Register 5 (0x7C) enables the $\overline{\text{THERM}}$

Figure 35 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5.5 V maximum to prevent damaging the ADT7476A.

Figure 36 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements. Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

Because the fan drive circuitry in 4-wire fans is not switched on or off, as with previous PWM driven/powered fans, the internal drive circuit is always on and uses the PWM input as a signal instead of a power supply. This enables the internal fan drive circuit to perform better than 3-wire fans, especially for high frequency applications.

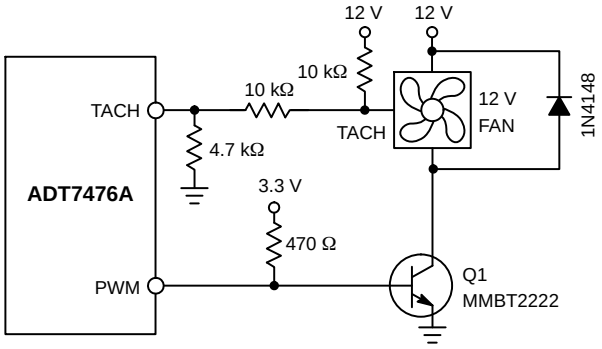

Figure 36. Driving a 3-wire Fan Using an NPN Transistor

Figure 37 shows a typical drive circuit for 4-wire fans.

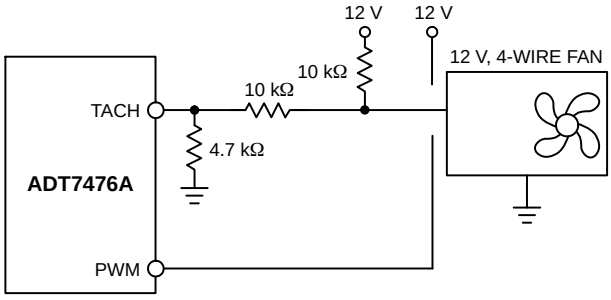

Figure 37. Driving a 4-wire Fan

Laying Out 3-Wire Fans

Figure 40 shows how to lay out a common circuit arrangement for 3-wire fans.

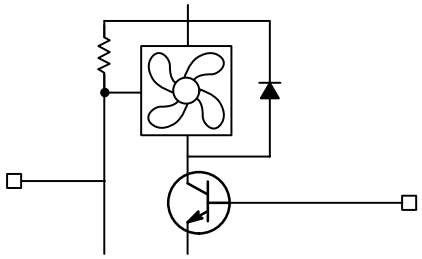

Figure 40. Planning for 3-wire Fans on a PCB

The fan counter does not count the fan TACH output pulses directly because the fan speed could be less than 1,000 RPM, and it takes several second9 1 accutput

Example:

TACH1 High Byte (0x29) = 0x17
TACH1 Low Byte (0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)
RPM = (f × 60)/Fan 1 TACH Reading
RPM = (90,000 × 60)/6143
Fan Speed = 879 RPM

TACH Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the TACH Pulses per Revolution Register (0x7B) for each fan. Alternatively, this register can be used to determine the number of pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution settings, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Table 37. FAN PULSES PER REVOLUTION REGISTER (REG. 0x7B)

Bit	Mnemonic	Description
[1:0]	FAN1 Default	2 Pulses per Revolution
[3:2]	FAN2 Default	2 Pulses per Revolution
[5:4]	FAN3 Default	2 Pulses per Revolution
[7:6]	FAN4 Default	2 Pulses per Revolution

Table 38. FAN PULSES PER REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

Fan Spin-up

The ADT7476A has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. Fans have different spin-up characteristics and take different times to overcome inertia. The advantage of the ADT7476A is that it runs the fans just fast enough to overcome inertia and is quieter on spin-up than fans that are programmed to spin up for a given time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up (because it is below running speed), the ADT7476A includes a fan startup timeout function. During this time, the ADT7476A looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated.

Fan startup timeout can be disabled by setting Bit 5 (FSPDIS) of Configuration Register 1 (0x40).

Table 39. PWM1 TO PWM3 CONFIGURATION (REG. 0x5C TO 0x5E)

Bit	Mnemonic	Description
[2:0]	SPIN	These Bits Control the Startup Timeout for PWM1 (0x5C), PWM2 (0x5D), PWM3 (0x5E). 000 = No Startup Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s

Disabling Fan Startup Timeout

Although fan startup makes fan spin-ups much quieter than fixed-time spin-ups, the option exists to use fixed spin-up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (0x40) disables the spin-up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Register 0x5C to Register 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non-inverted) or low for 100% duty cycle (inverted).

Table 40. PWM1 TO PWM3 CONFIGURATION (REG. 0x5C TO 0x5E) BITS

Bit	Mnemonic	Description
[4]	INV	0 = Logic High for 100% PWM Duty

In high frequency mode, the PWM drive frequency is always 22.5 kHz. When high frequency mode is enabled, the

$\overline{\text{THERM}}$ Operation in Manual Mode

In manual mode, if the temperature increases above the programmed $\overline{\text{THERM}}$ temperature limit, the fans automatically speed up to maximum PWM or 100% PWM, whichever way the appropriate fan channel is configured.

Automatic Fan Control Overview

The ADT7476A can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7476A has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel Pentium class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible due to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan, are critical, because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so these values should be selected carefully.

Figure 47 gives a top-level overview of the automatic fan control circuitry on the ADT7476A. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7476A allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, designers can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C.

At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 47 shows fan-specific controls. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

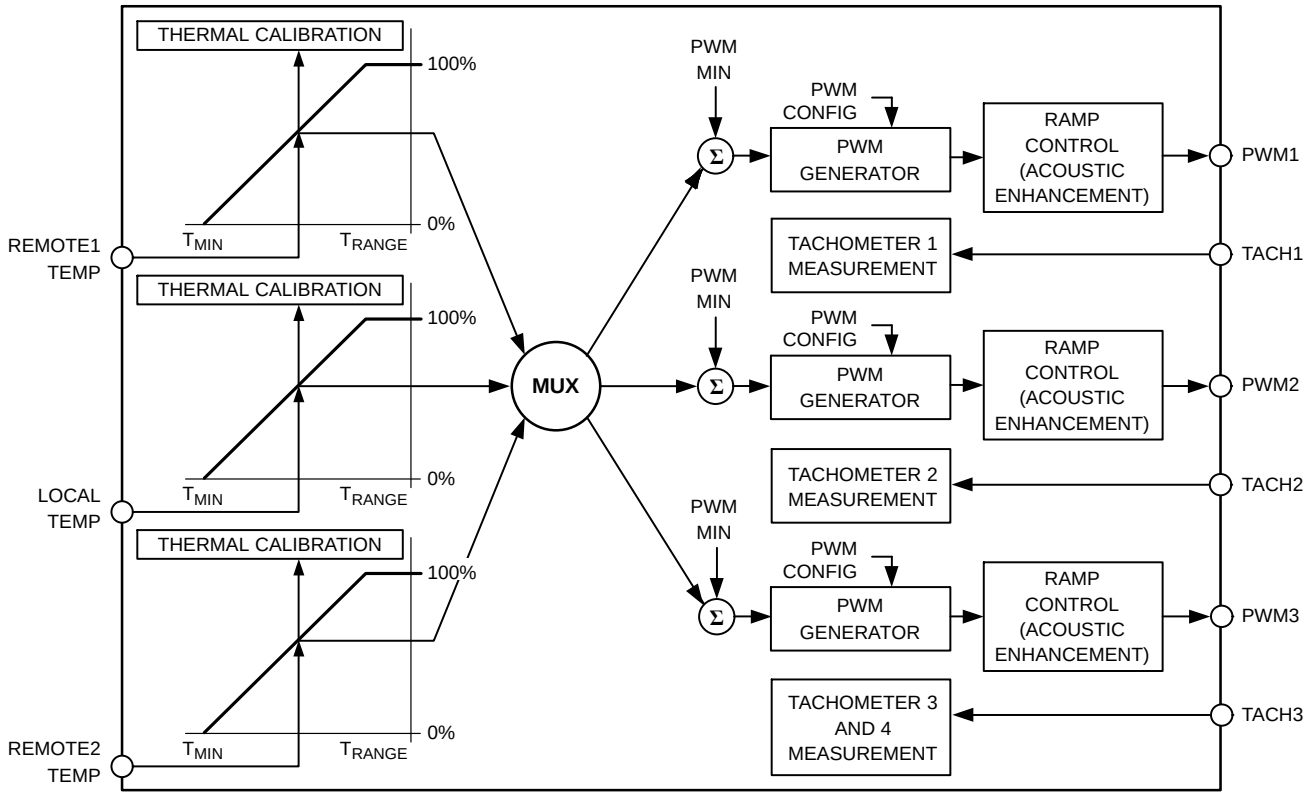

Figure 47. Automatic Fan Control Block Diagram

Step 1 − Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What ADT7476A functionality is used?
   - PWM2 or $\overline{\text{SMBALERT}}$?
   - TACH4 fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?
   - 2.5 V voltage monitoring or overtemperature $\overline{\text{THERM}}$ function?
   - 12 V voltage monitoring or VID5 input?
     The ADT7476A offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.
2. How many fans are supported in system, three or four?
   This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{\text{THERM}}$ function.
3. Is the CPU fan to be controlled using the ADT7476A, or will the CPU fan run at full speed 100% of the time?
   If run at 100%, this frees up a PWM output, but the system is louder.
4. Where will the ADT7476A be physically located in the system?
   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7476A close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

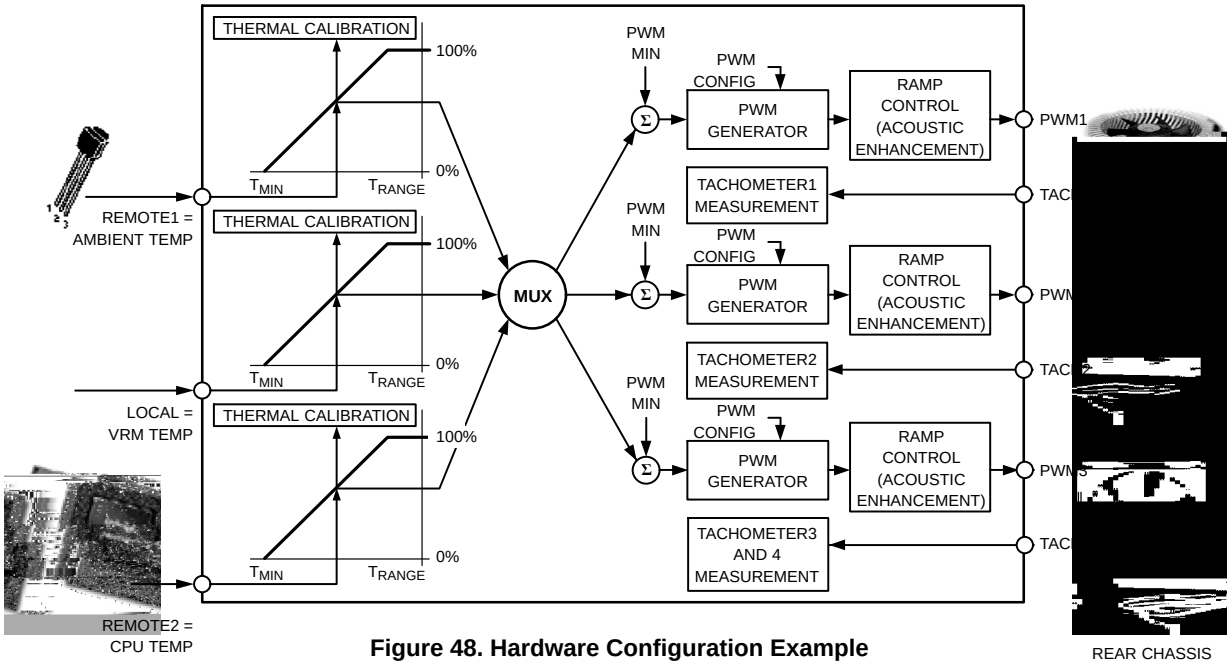

Figure 48. Hardware Configuration Example

Step 2 − Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, manually (under software control), or at the fastest speed calculated by multiple temperature channels. The mux is the bridge

Mux Configuration Example

This is an example of how to configure the mux in a system using the ADT7476A to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also being used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example Mux Settings

[7:5] (BHVR), PWM1 Configuration Register (0x5C).
101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

[7:5] (BHVR), PWM2 Configuration Register (0x5D).
000 = Remote 1 temperature controls PWM2

[7:5] (BHVR), PWM3 Configuration Register (0x5E).
000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 52.

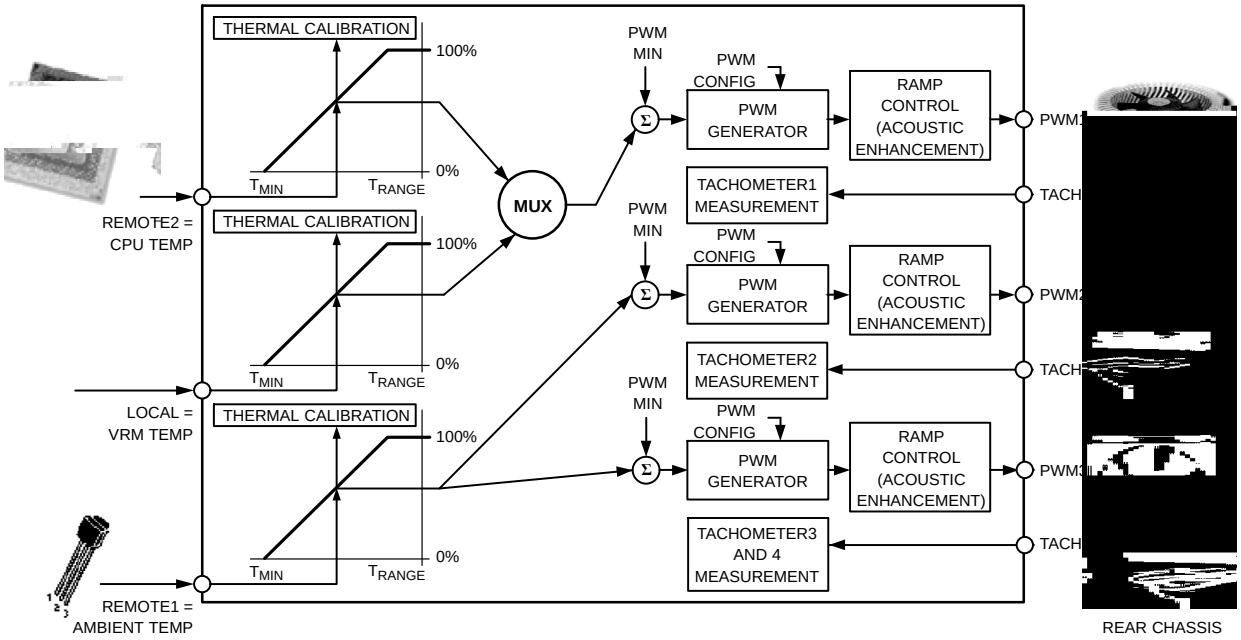

Figure 52. Mux Configuration Example

Step 4 − PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33%

Programming the PWM Maximum Duty Cycle Registers

The PWM maximum duty cycle registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM maximum duty cycle register is given by:

Value (decimal) = $PWM_{MAX}/0.39$

Example 1:

For a maximum PWM duty cycle of 50%,
Value (decimal) – 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2:

For a minimum PWM duty cycle of 75%,
Value (decimal) = 75/0.39 = 85 (decimal)
Value = 192 (decimal) or C0 (hex)

Table 46. PWM MAXIMUM DUTY CYCLE REGISTERS

Register	Description	Default
0x38	PWM1 Maximum Duty Cycle	0xFF (100%)
0x39	PWM2 Maximum Duty Cycle	0xFF (100%)
0x3A	PWM3 Maximum Duty Cycle	0xFF (100%)

Step 6 − T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is the temperature range between PWM_{MIN} and 100% PWM where the fan speed changes linearly. Otherwise stated, it is the line drawn between the T_{MIN}/PWM_{MIN} and the $(T_{MIN} + T_{RANGE})/PWM100\%$ intersection points.

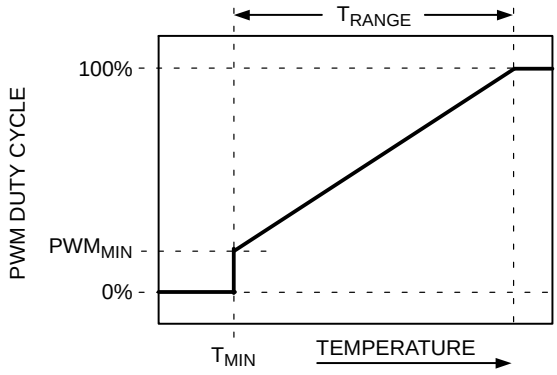

Figure 57. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine experimentally the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. For example, 70°C is reached when the fans are running at 50% PWM duty cycle.
3. Determine the slope of the required control loop to meet these requirements.
4. Using the ADT7476A evaluation software, you can graphically program and visualize this functionality.

As PWM_{MIN} is changed, the automatic fan control slope changes.

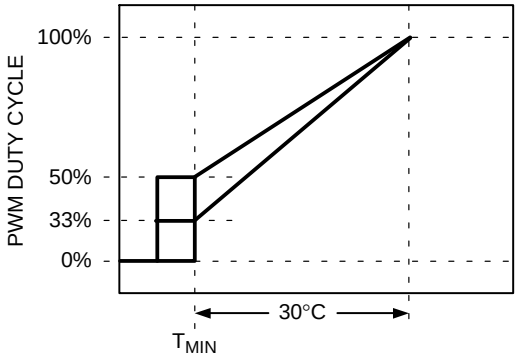

Figure 58. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

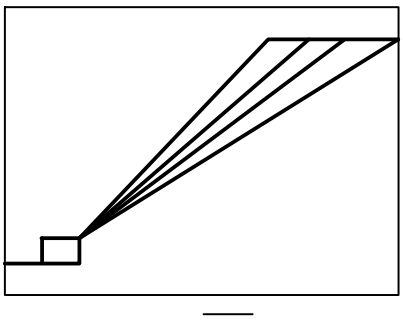

Figure 59. Increasing T_{RANGE} Changes the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, Local, and Remote 2 temperature. Bits [7:4] (T_{RANGE}) of Register 0x5F to Register 0x61 define the T_{RANGE} value for each temperature channel.

Table 47. SELECTING A T_{RANGE} VALUE

Bits [7:4] (Note 1)	**T_{RANGE} (°C)**
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (Default)
1101	40
1110	53.33
1111	80

1. Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures Local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, it is also necessary to note that the enhance acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means that if T_{RANGE} is programmed with an AFC slope that is quite steep, a relatively small change in temperature could cause a large change in PWM output and possibly an audible change in fan speed, which can be noticeable/ bothersome to end users.

Decreasing the speed the PWM output changes by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63) changes how fast the fan speed increases/decreases in the event of a temperature spike. The PWM duty cycle increases slowly until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 61 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

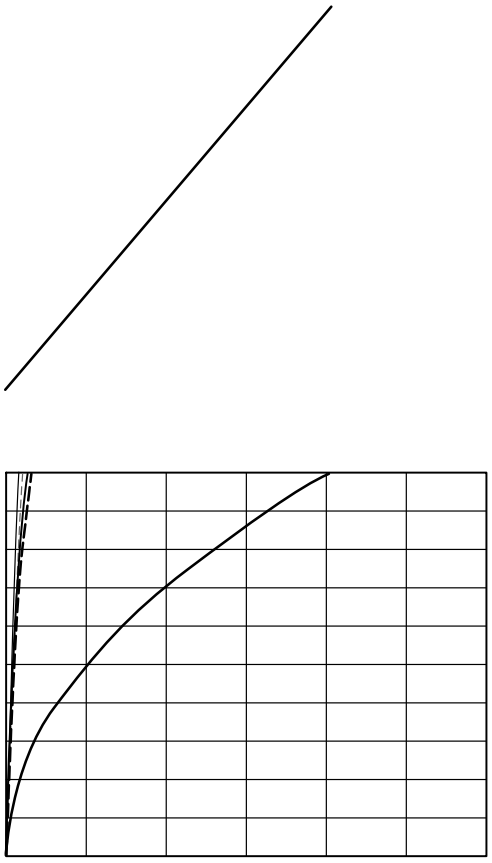

Figure 61. T_{RANGE} vs. Actual Fan Speed (Not PWM Drive) Profile

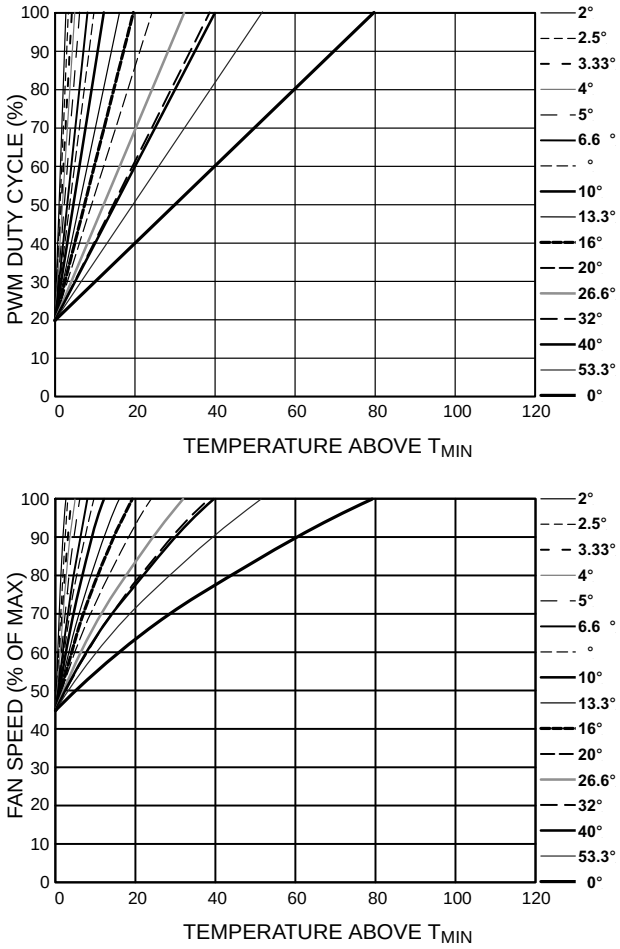

Figure 62. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

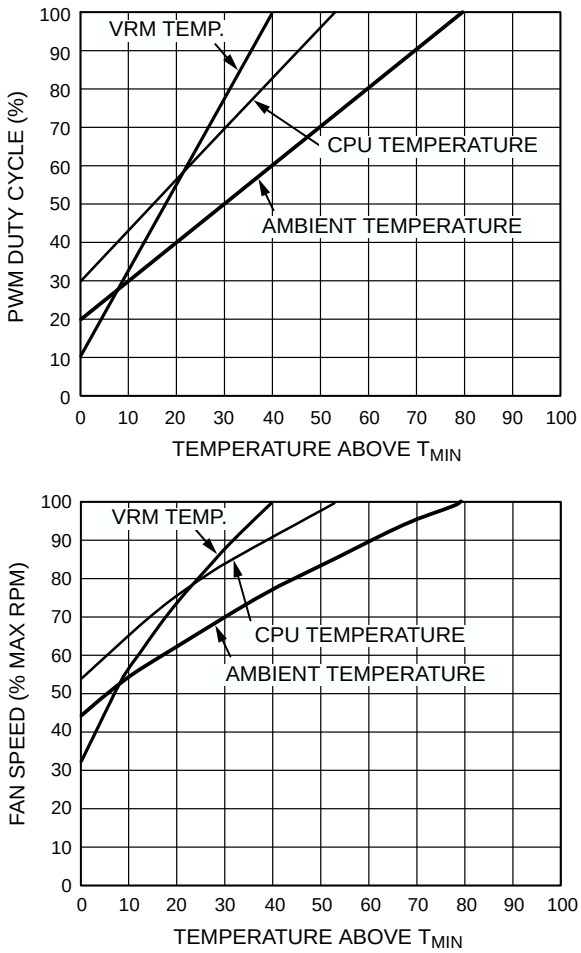

Figure 63. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for ambient temperature

T_{RANGE} = 53.33°C for CPU temperature

T_{RANGE} = 40°C for VRM temperature

This example uses the mux configuration described in Step 2 - Configuring the Mux with the ADT7476A connected as shown in Figure 52. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note: The control range for 4-wire fans is much wider than that of 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3-wire fans cannot run unless a PWM drive of 60% or more is applied.

Step 7 − $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM can operate beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and users should ensure that it is not exceeded under normal system operating conditions.

Note: $T_{\overline{THERM}}$ limits are nonmaskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

Table 48. $\overline{\text{THERM}}$ LIMIT REGISTERS

Register	Description	Default
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6B	Local $\overline{\text{THERM}}$ Limit	0x64 (100°C)
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0x64 (100°C)

$\overline{\text{THERM}}$ Hysteresis

$\overline{\text{THERM}}$ hysteresis on a particular channel is configured via the hysteresis settings (Register 0x6D and Register 0x6E). For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{\text{THERM}}$.

Hysteresis Registers

Register 0x6D, Remote 1, Local Temperature Hysteresis

[7:4], Remote 1 temperature hysteresis (4°C default).

[3:0], Local temperature hysteresis (4°C default).

Register 0x6E**,** Remote 2 Temperature Hysteresis

[7:4], Remote 2 temperature hysteresis (4°C default).

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended to program hysteresis values to 0°C, because this disables hysteresis. In effect, this causes the fans to cycle (during a $\overline{\text{THERM}}$ event**)** between normal speed and 100% speed, or, while operating close to T_{MIN}, between normal speed and off, creating unsettling acoustic noise.

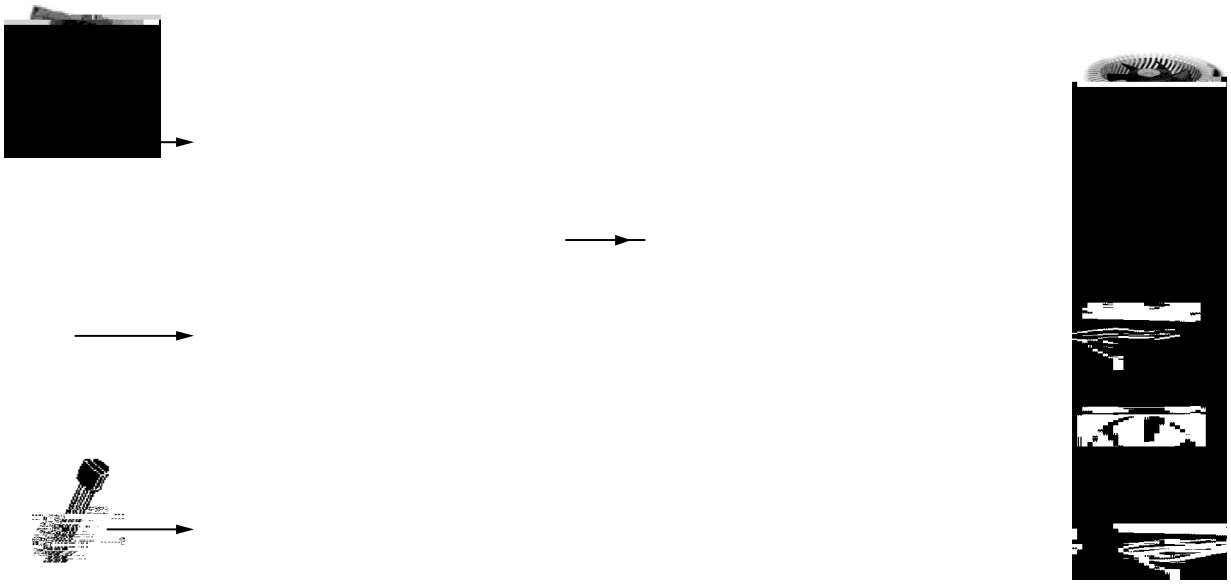

Figure 64. How $T_{\overline{\text{THERM}}}$ Relates to Automatic Fan Control

Step 8 − T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after

Enhance Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (0x10)

[0] SLOW = 1, slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by a factor of 4.

[1] SLOW = 1, slows the ramp rate for PWM changes associated with the local temperature channel by a factor of 4.

[2] SLOW = 1, slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by a factor of 4.

[7] ExtraSlow = 1, slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp-up times when enhanced acoustics is enabled for each temperature channel.

Enhance Acoustics Register 1 (0x62)

[2:0] ACOU selects the ramp rate for PWM outputs associated with the Remote Temperature 1 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Enhance Acoustics Register 2 (0x63)

[2:0] ACOU3 selects the ramp rate for PWM outputs associated with the local temperature channel.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

[6:4] ACOU2 selects the ramp rate for PWM outputs associated with the Remote Temperature 2 input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

When Bit 7 of Configuration Register 6 (0x10) = 1, the above ramp rates change to the values below.

000 = 52.2 sec
001 = 26.1 sec
010 = 17.4 sec
011 = 10.4 sec
100 = 6.5 sec
101 = 4.4 sec
110 = 2.2 sec
111 = 1.1 sec

Setting the appropriate slow bit [2:0] of Configuration Register 6 (0x10) slows the ramp rate further by a factor of 4.

Fan Presence Detect

This feature is used to determine if a 4-wire fan is directly connected to a PWM output. This feature does not work for 3-wire fans. To detect whether a 4-wire fan is connected directly to a PWM output, the following must be performed in this order:

1. Drive the appropriate PWM outputs to 100% duty cycle.
2. Set Bit 0 of Configuration Register 2 (0x73).
3. Wait 5 ms.
4. Program fans to run at a different speed if necessary.
5. Read the state of Bits [3:1] of Configuration Register 2 (0x73). The state of these bits reflects whether a 4-wire fan is directly connected to the PWM output.

As the detection time only takes 5 ms, programming the PWM outputs to 100% and then back to its normal speed is not noticeable in most cases.

Fan Sync

When two ADT7476As are used in a system, it is possible to synchronize them so that one PWM channel from each device can be effectively OR'ed together to create a PWM output that reflects the maximum speed of the two OR'ed PWMs. This OR'ed PWM can in turn be used to drive a chassis fan.

Standby Mode

The ADT7476A has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

When the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Interrupt Status Register 1 is set.
2. $\overline{\text{SMBALERT}}$ is generated, if enabled.
3. $\overline{\text{THERM}}$ monitoring is disabled. The $\overline{\text{THERM}}$ timer should hold its value prior to the S3 or S5 state.

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR Tree Test Mode

The ADT7476A includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens, or shorts, on the system board.

The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR Tree Test Enable Register (0x6F).

Figure 66 shows the signals that are exercised in the XNOR tree test mode.

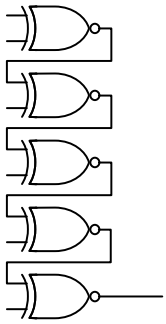

Figure 66. XNOR Tree Test

Register Tables

Table 49. ADT7476A REGISTERS

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x10	R/W	Configuration Register 6	Extra Slow									

Table 49. ADT7476A REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	5.0 V	V_{CC}	V_{CCP}	2.5 V/		

Table 49. ADT7476A REGISTERS (continued)

Table 49. ADT7476A REGISTERS (continued)

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	−
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	−
0x7C	R/W	Configuration Register 5	R2 $\overline{\text{THERM}}$	Local $\overline{\text{THERM}}$	R1 $\overline{\text{THERM}}$	VID/ GPIO	GPIO6P	GPIO6D	Temp Offset	2sC	0x01	Yes
0x7D	R/W	Configuration Register 4	BpAtt 12 V	BpAtt 5.0 V	BpAtt V_{CCP}	BpAtt 2.5 V	Max Speed on $\overline{\text{THERM}}$	$\overline{\text{THERM}}$ Disable	PIN14 FUNC	PIN14 FUNC	0x00	Yes
0x7E	R	Test 1	DO NOT WRITE TO THESE REGISTERS								0x00	Yes
0x7F	R	Test 2	DO NOT WRITE TO THESE REGISTERS								0x00	Yes

Table 50. REGISTER 0x10 − CONFIGURATION REGISTER 6 (POWER-ON DEFAULT = 0x00) (Note 1 and 2)

Bit No.	Mnemonic	R/W	Description
[0]	SlowFan Remote 1	R/W	When this bit is set, Fan 1 smoothing times are multiplied x4 for Remote 1 temperature channel (as defined in Register 0x62).
[1]	SlowFan Local	R/W	When this bit is set, Fan 2 smoothing times are multiplied x4 for local temperature channel (as defined in Register 0x63).
[2]	SlowFan Remote 2	R/W	When this bit is set, Fan 3 smoothing times are multiplied x4 for Remote 2 temperature channel (as defined in Register 0x63).
[3]	$\overline{\text{THERM}}$ in Manual	R/W	When this bit is set, $\overline{\text{THERM}}$ is enabled in manual mode. (Note 1)
[4]	SlaveEn	R/W	Setting this bit configures the ADT7476A as a slave for use in fan sync mode.
[5]	MasterEn	R/W	Setting this bit configures the ADT7476A as a master for use in fan sync mode.
[6]	V_{CCP} Low	R/W	V_{CCP}Low = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Register 0x46), the following occurs: Status Bit 1 in Interrupt Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated, if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Everything is re-enabled once V_{CCP} increases above the V_{CCP} low limit.When V_{CCP} increases above the low limit: $\overline{\text{PROCHOT}}$ monitoring is enabled. Fans return to their programmed state after a spin-up cycle.
[7]	ExtraSlow	R/W	When this bit is set, all fan smoothing times are increased by a further 39.2%

1. A $\overline{\text{THERM}}$ event always overrides any fan setting (even when fans are disabled).
2. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 51. REGISTER 0x11 − CONFIGURATION REGISTER 7 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	DisTHERM Hys	Read/Write	Setting This Bit to 1 Disables $\overline{\text{THERM}}$ Hysteresis
[7:1]	Reserved	N/A	Reserved. Do Not Write to These Bits

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 52. VOLTAGE READING REGISTERS (POWER-ON DEFAULT = 0x00)

Table 56. PWM MAXIMUM DUTY CYCLE (POWER-ON DEFAULT = 0xFF) (Note 1 and 2)

Register Address	R/W	Description
0x38	R/W	Maximum Duty Cycle for PWM1 Output, Default = 100% (0xFF)
0x39	R/W	Maximum Duty Cycle for PWM2 Output, Default = 100% (0xFF)
0x3A	R/W	Maximum Duty Cycle for PWM3 Output, Default = 100% (0xFF)

1. These registers set the maximum PWM duty cycle of the PWM output.
2. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 57. REGISTER 0x40 − CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0x04)

Bit No.	Mnemonic	R/W	Description
[0]	STRT (Notes 1, 2)	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control is based on the default powerup limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK bit) has been set.
[1]	LOCK	Write once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only and cannot be modified until the ADT7476A is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable.)
[2]	RDY	Read-only	This bit is set to 1 by the ADT7476A to indicate that the device is fully powered-up and ready to begin system monitoring.
[3]	FSPD	R/W	When set to 1, this bit runs all fans at max speed as programmed in the max PWM current duty cycle registers (0x30 to 0x32). Power-on default = 0. This bit is not locked at any time.
[4]	Vx1	R/W	BIOS should set this bit to a 1 when the ADT7476A is configured to measure current from an ADOPT® VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
[5]	FSPDIS	R/W	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
[6]	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the ADT7476A to be used with SMBus controllers that cannot handle SMBus timeouts. This bit is lockable.
[7]	Reserved	N/A	Reserved. Do not write to this bit.

1. Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after lock bit is set.
2. When monitoring (STRT) is disabled, PWM outputs always go to 100% for thermal protection.

Table 58. REGISTER 0x41 − INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	2.5 V/ $\overline{\text{THERM}}$	Read-only	2.5 V = 1 indicates that the 2.5 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 22 is configured as $\overline{\text{THERM}}$, this bit is asserted when the timer limit has been exceeded.
[1]	V_{CCP}	Read-only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[2]	V_{CC}	Read-only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[3]	5.0 V	Read-only	A 1 indicates that the 5.0 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[4]	R1T	Read-only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[5]	LT	Read-only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[6]	R2T	Read-only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[7]	OOL	Read-only	OOL = 1 indicates that an out-of-limit event has been latched in Interrupt Status Register 2. This bit is a logical OR of all status bits in Interrupt Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 2 are out-of-limit, which eliminates the need to read Interrupt Status Register 2 during every interrupt or polling cycle.

Table 59. REGISTER 0x42 − INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	12 V/VC	Read-only	A 1 indicates that the 12 V high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided. If Pin 21 is configured as VID5, this bit is the VID change bit. This bit is set when the levels on VID0 to VID5 are different than they were 11 μs previously. This pin can be used to generate an $\overline{\text{SMBALERT}}$ whenever the VID code changes.
[1]	OVT	Read-only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ − T_{HYST}.
[2]	FAN1	Read-only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
[3]	FAN2	Read-only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
[4]	FAN3	Read-only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
[5]	F4P	Read-only R/W Read-only	When Pin 14 is programmed as a TACH4 input, F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off. When Pin 14 is programmed as the GPIO6 output, writing to this bit determines the logic output of GPIO6. When GPIO6 is programmed as an input, this bit reflects the value read by GPIO6. If Pin 14 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, then this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ timer limit register (0x7A).
[6]	D1	Read-only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
[7]	D2	Read-only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 60. REGISTER 0x43 − VID/GPIO REGISTER (POWER-ON DEFAULT = 0x1F)

Bit No.	Mnemonic	R/W	Description
[4:0]	VID[4:0]/ GPIO[4:0]	R/W	The VID[4:0] inputs from the CPU indicate the expected processor core voltage. On powerup, these bits reflect the state of the VID pins, even if monitoring is not enabled. When Bit 4 of Configuration Register 5 (0x7C) = 1, these bits become general-purpose outputs. The state of these bits then reflects the state of the appropriate GPIO pin.
[5]	VID5	R/W	Reads VID5 from the CPU when Bit 7 = 1. If Bit 7 = 0, the VID5 bit always reads back 0 (power-on default).
[6]	THLD	R/W	Selects the input switching threshold for the VID inputs. THLD = 0 selects a threshold of 1 V (V_{OL} < 0.8 V, V_{IH} > 1.7 V). THLD = 1 lowers the switching threshold to 0.6 V (V_{OL} < 0.4 V, V_{IH} > 0.8 V).
[7]	VIDSEL	R/W	VIDSEL = 0 configures Pin 21 as the 12 V measurement input (Default).

Table 61. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	**Description** (Note 2)	Power-On Default
0x44	R/W	2.5 V Low Limit	0x00
0x45	R/W	2.5 V High Limit	0xFF
0x46	R/W	V_{CCP} Low Limit	0x00
0x47	R/W	V_{CCP} High Limit/Vf209 these bits then reflectsm0 Tc0 Tw(0xFt)TjET209.554 214.186 .6803 13.8t	

Table 62. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x4E	R/W	Remote 1 Temperature Low Limit	0x81
0x4F	R/W	Remote 1 Temperature High Limit	0x7F
0x50	R/W	Local Temperature Low Limit	0x81
0x51	R/W	Local Temperature High Limit	0x7F
0x52	R/W	Remote 2 Temperature Low Limit	0x81
0x53	R/W	Remote 2 Temperature High Limit	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 Lock bit has no effect on these registers.
2. High limits: An interrupt is generated when a value exceeds its high limit (> comparison). Low limits: An interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 63. FAN TACH LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x54	R/W	TACH1 Minimum Low Byte	0xFF
0x55	R/W	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	R/W	TACH2 Minimum Low Byte	0xFF
0x57	R/W	TACH2 Minimum High Byte	0xFF
0x58	R/W	TACH3 Minimum Low Byte	0xFF
0x59	R/W	TACH3 Minimum High Byte	0xFF
0x5A	R/W	TACH4 Minimum Low Byte	0xFF
0x5B	R/W	TACH4 Minimum High Byte	0xFF

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 Lock bit has no effect on these registers.

Table 64. REGISTER 0x55 − TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0xFF)

Bit No.	Mnemonic	R/W	Description
[4:0]	Reserved	Read-only	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are reserved. Otherwise, these bits represent Bits [4:0] of the TACH1 minimum high byte.
[7:5]	SCADC	R/W	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC will take measurements. Otherwise, these bits represent Bits [7:5] of the TACH1 minimum high byte.

Table 65. PWM CONFIGURATION REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x5C		R/W	PWM1 Configuration	0x62
0x5D		R/W	PWM2 Configuration	0x62
0x5E		R/W	PWM3 Configuration	0x62
Bit No.	**Name**	**R/W**	**Description**	
[2:0]	SPIN	R/W		

Table 66. T_{RANGE}/PWM FREQUENCY REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x5F		R/W	Remote 1 T_{RANGE}/PWM1 Frequency	0xC4
0x60		R/W	Local T_{RANGE}/PWM2 Frequency	0xC4
0x61		R/W	Remote 2 T_{RANGE}/PWM3 Frequency	0xC4
Bit No.	**Name**	**R/W**	**Description**	
[2:0]	FREQ	R/W	These bits control the PWMx frequency (only apply when PWM channel is in low frequency mode). 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz	
[3]	HF/LR	R/W	HF/LF = 1, High Frequency PWM Mode is Enabled for PWMx HF/LF = 0, Low Frequency PWM Mode is Enabled for PWMx.	
[7:4]	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature range for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (Default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C	

1. These registers become read-only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers have no effect.

Table 67. REGISTER 0x62 − ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[2:0]	ACOU (Note 2)	R/W	Assuming that PWMx is associated with the Remote 1 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 1 temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[3]	EN1	R/W	When this bit is 1, smoothing is enabled on Remote 1 temperature channel.
[4]	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.
[5]	MIN1	R/W	When the ADT7476A is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} − hysteresis value. 0 = 0% duty cycle below T

Table 68. REGISTER 0x63 − ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[2:0]	ACOU3	R/W	Assuming that PWMx is associated with the local temperature channel, these bits define the maximum rate of change of the PWMx output for local temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[3]	EN3	R/W	When this bit is 1, smoothing is enabled on the local temperature channel.
[6:4]	ACOU2	R/W	Assuming that PWMx is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 2 Temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan. **When Bit 7 of Configuration Register 6 (0x10) is 0** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec **When Bit 7 of Configuration Register 6 (0x10) is 1** **Time Slot Increase** — **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[7]	EN2	R/W	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 69. PWM MINIMUM DUTY CYCLE REGISTERS (Note 1)

Register Address		R/W	Description	Power-On Default
0x64		R/W	PWM1 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x65		R/W	PWM2 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x66		R/W	PWM3 Minimum Duty Cycle	0x80 (50% Duty Cycle)
Bit No.	**Name**	**R/W**	**Description**	
[7:0]	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)	

1. These registers become read-only when the ADT7476A is in automatic fan control mode.

Table 70. T_{MIN} REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x67	R/W	Remote 1 Temperature T_{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T_{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T_{MIN}	0x5A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
2. These registers become read-only when the Configuration Register 1 Lock bit is set. Any further attempts to write to these registers have no effect.

Table 71. $\overline{\text{THERM}}$ LIMIT REGISTERS (Note 1 and 2)

Register Address	R/W	Description	Power-On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temperature Limit	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ Temperature Limit	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$	

Table 73. XNOR TREE TEST ENABLE (Note 1)

Register Address	R/W	Description	Power-On Default
0x6F	R/W	XNOR tree test enable register.	0x00
[0]	XEN	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	
[7:1]	Reserved	Unused. Do not write to these bits.	

1. This register becomes read-only when the Configuration Register 1 Lock bit is set to 1. Any further attempts to write to this

Table 77. REGISTER 0x73 − CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
0	FanPresDT	R/W	When FanPresenceDT = 1, the state of Bits [3:1] of 0x73 reflects the presence of a 4-wire fan on the appropriate T2-loH cw20f3

Table 85. REGISTER 0x7B − TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0x55)

Bit No.	Mnemonic	R/W	Description
[1:0]	FAN1	R/W	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[3:2]	FAN2	R/W	Sets number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[5:4]	FAN3	R/W	Sets number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
[7:6]	FAN4	R/W	Sets number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

Table 86. REGISTER 0x7C − CONFIGURATION REGISTER 5 (POWER-ON DEFAULT = 0x01) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	2sC	R/W	2sC = 1 sets the temperature range to the twos complement temperature range. 2sC = 0 changes the temperature range to the Offset 64 temperature range. When this bit is changed, the ADT7476A interprets all relevant temperature register values as defined by this bit.
[1]	Temp Offset	R/W	TempOffset = 0 sets offset range to −63°C to +64°C with 0.5°C resolution. TempOffset = 1 sets offset range to −63°C to +127°C with 1°C resolution. These settings apply to Remote 1, Local, and Remote 2 temperature offset registers (0x70, 0x71, and 0x72).
[2]	GPIO6D	R/W	GPIO6 direction. When GPIO6 function is enabled, this determines whether GPIO6 is an input (0) or an output (1).
[3]	GPIO6P	R/W	GPIO6 polarity. When the GPIO6 function is enabled and is programmed as an output, this bit determines whether the GPIO6 is active low (0) or high (1).
[4]	VID/GPIO	R/W	VID/GPIO = 0 enables VID functionality on Pin 5, Pin 6, Pin 7, Pin 8, and Pin 19. VID/GPIO = 1 enables GPIO functionality on Pin 5, Pin 6, Pin 7, Pin 8, and Pin 19.
[5]	R1 $\overline{\text{THERM}}$	R/W	R1 $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for Remote 1 temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. R1 $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[6]	Local $\overline{\text{THERM}}$	R/W	Local $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for local temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. Local $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.
[7]	R2 $\overline{\text{THERM}}$	R/W	R2 $\overline{\text{THERM}}$ = 1 enables $\overline{\text{THERM}}$ temperature limit functionality for Remote 2 temperature channel; that is, $\overline{\text{THERM}}$ is bidirectional. R2 $\overline{\text{THERM}}$ = 0 indicates $\overline{\text{THERM}}$ is a timer input only. $\overline{\text{THERM}}$ can also be disabled on any channel by: Writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit in Offset 64 mode. Writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit in twos complement mode.

1. This register becomes read-only when the Configuration Register 1

QSOP24 NB
CASE 492B−01
ISSUE A

DATE 06 MAY 2008

SCALE 2:1