

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V _{CC})	3.6	V
Maximum Voltage on +12 V _{IN} Pin	16	V
Maximum Voltage on +5 V _{IN} Pin	6.25	V
Maximum Voltage on All Open-drain Outputs (excluding PWM pins)	3.6	V
Maximum Voltage on TACHx/PWMx Pins	+5.5	V
Voltage on Remaining Input or Output Pins	-0.3 to +4.2	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature (T _{J MAX})	150	°C
Storage Temperature Range	-65 to +150	°C

Lead Temperature, Soldering IR Reflow Peak Temperature Pb-Free Peak Temperature Lead Temperature (Soldering, 10 sec)

Table 3. ELECTRICAL CHARACTERISTICS (continued)

$(T_A$ = T_{MIN} to $T_{MAX},\,V_{CC}$ = V_{MIN} to $V_{MAX},$ unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Тур	Max	Unit
Analog-to-Digital Converter (Including	MUX and Attentuators)				
Total Unadjusted Error (TUE)	For All Channels: $-40^{\circ}C \le T_A \le +125^{\circ}C$ For All Other Channels Except +12 V _{IN} : $0^{\circ}C \le T_A \le +125^{\circ}C$		-	±2 ±1.5	%
Differential Non-linearity (DNL)	8 Bits	-	-	±1	LSB
Power Supply Sensitivity					

Table 3. ELECTRICAL CHARACTERISTICS (continued)

 $(T_A$ = T_{MIN} to $T_{MAX},\,V_{CC}$ = V_{MIN} to $V_{MAX},$ unless otherwise noted) (Note 1)

Parameter	Conditions	Min	Тур	Max	Unit
Digital Input Logic Levels (TACH1	to TACH3)				
Input High Voltage, V _{IH}	Maximum Input Voltage	2.0	_ _	_ 5.5	V
Input Low Voltage, V _{IL}	Minimum Input Voltage	-0.3		0.8 -	V
Hysteresis		-	0.5	_	V р-р
Digital Input Logic Levels (THERM	٨)				
Input High Voltage, V _{IH}		$0.75 \times V_{CCP}$	-	-	V
Input Low Voltage, V _{IL}		-	-	0.4	V
Digital Input Current					
Input High Current, IIH	$V_{IN} = V_{CC}$	-	±1	-	μΑ
Input Low Current, IIL	V _{IN} = 0	-	±1	-	μΑ
Input Capacitance, C _{IN}		-	5.0	_	pF

Table 4. PIN ASSIGNMENT

Pin No.	Mnemonic	Туре	Description
1	SDA	Digital I/O	SMBus Bidirectional Serial Data. Open drain, requires SMBus pullup.
2	SCL	Digital Input	SMBus Serial Clock Input. Open drain, requires SMBus pullup.
3	GND	Ground	Ground Pin.
4	V _{CC}	Power Supply	3.3 V ±

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

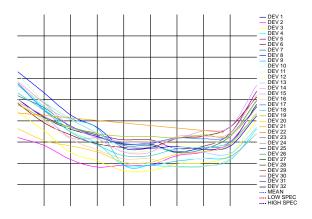


Figure 5. Local Temperature Sensor Error

Figure 6. Remote 1 Temperature Sensor Error

Figure 7. Remote 2 Temperature Sensor Error

Figure 8. ADT7490 Response to Thermal Shock

Figure 9. Temperature Error vs. Series Resistance

Figure 10. Local Temperature Error vs. Power Supply Noise Frequency

Theory of Operation

The ADT7490 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 1), and an input line for the serial clock (Pin 2). All control and programming functions for the ADT7490 are performed over the serial bus. In addition, Pin 14 can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Feature Comparisons Between the ADT7490 and ADT7476A

The ADT7490 is pin and register map compatible with the ADT7476A. The new or additional features are detailed in the following sections.

PECI Input

CPU thermal information is provided through the PECI input. The ADT7490 has PECI master capabilities and can read the CPU thermal information through the PECI the I_{MON} value and the measured V_{CCP} value on Pin 23, the CPU power consumption can be calculated. The I_{MON} information can be considered as an early indication of an increase in CPU temperature.

Startup Operation

At startup, the ADT7490 turns the fans on to 100% PWM. This allows the most robust operation at turn-on.

Serial Bus Interface

Control of the ADT7490 is carried out using the serial system management bus (SMBus). The ADT7490 is connected to this bus as a slave device, under the control of a master controller. The ADT7490 has a 7-bit serial bus address. When the device is powered up with Pin 13 (PWM3/ADDREN) high, the ADT7490 has a default SMBus address of 0101110 or 0x2E. The read/write bit must be added to obtain the 8-bit address. If more than one ADT7490 is to be used in a system, each ADT7490 is placed in address select mode by strapping Pin 13 low on powerup. The logic state of Pin 14 then determines the device's SMBus address. The logic of these pins is sampled on powerup.

The device address is monitored from powerup but not latched until the first valid SMBus transaction, more precisely on the low-to-high transition at the beginning of the eighth SCL pulse, when the serial bus address byte matches the selected slave address. The selected slave address is chosen using the ADDREN/ADDR SELECT pins. Any attempted changes in the address have no effect after this.

Table 7. HARD-WIRING THE ADT7490 SMBus DEVICE ADDRESS

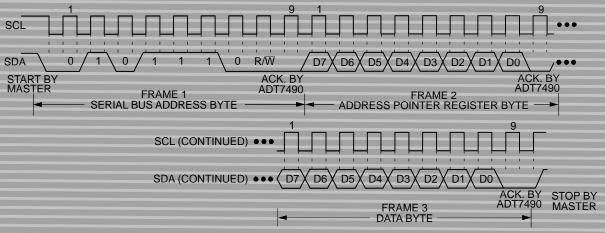
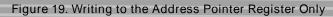


Figure 18. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

	1	9 1 .	
SCL			
302			

SDA 0	1 0 1 1 1 0	D7	D6 D5 D4 D3 D2 D1 I	00	
START BY	FRAME 1	ACK. BY	FRAME 2	ADT7490	STOP BY
MASTER	SERIAL BUS ADDRESS BYTE	ADT7490	ADDRESS POINTER REGISTER BY		MASTER



For the ADT7490, the send byte protocol is used to write

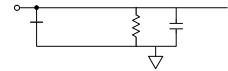
output of ON Semiconductor's VR11.1 controllers. I_{MON} is a voltage representation of the CPU current.

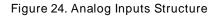
Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. This ADC has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the inputs have built-in attenuators to allow measurement of 2.5 V, 3.3 V, 5.0 V, 12 V, and the processor core voltage V_{CCP} without any external components. To allow the tolerance of these supply voltages, the ADC produces an output of 3/4 full scale (768 decimal or 0x300 hexadecimal) for the nominal input voltage, and therefore, has adequate headroom to cope with overvoltages.

Input Circuitry

The internal structure for the analog inputs is shown in Figure 24. The input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives input immunity to high frequency noise.





Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7490 to offer the system designer increased flexibility. The functions described in the following sections are

Table 13. 10-BIT ADC OUTPUT CODE VS. VIN

Input Voltage ADC Output		C Output					
+12 V _{IN}	+5 V _{IN}	V _{CC} (3.3 V _{IN})	+2.5 V _{IN}	V _{CCP}	V _{TT} /I _{MON}	Decimal	Binary (10 Bits)
<0.0156	<0.0065	<0.0042	<0.0032	<0.00293	<0.00220	0	00000000 00
0.0156 to 0.0312	0.0065 to 0.0130	0.0042 to 0.0085	0.0032 to 0.0065	0.0293 to 0.0058	0.00220 to 0.00440	1	0000000 01
0.0312 to 0.0469	0.0130 to 0.0195	0.0085 to 0.0128	0.0065 to 0.0097	0.0058 to 0.0087	0.00440 to 0,00660	2	0000000 10
0.0469 to 0.0625	0.0195 to 0.0260	0.0128 to 0.0171	0.0097 to 0.0130	0.0087 to 0.0117	0,00660 to 0.00881	3	00000000 11
0.0625 to 0.0781	0.0260 to 0.0325	0.0171 to 0.0214	0.0130 to 0.0162	0.0117 to 0.0146	0.00881 to 0.01100	4	00000001 00
0.0781 to 0.0937	0.0325 to 0.0390	0.0214 to 0.0257	0.0162 to 0.0195	0.0146 to 0.0175	0.01100 to 0.01320	5	00000001 01
0.0937 to 0.1093	0.0390 to 0.0455	0.0257 to 0.0300	0.0195 to 0.0227	0.0175 to 0.0205	0.01320 to 0.01541	6	00000001 10

0.1093 to 0.1250

Temperature Measurement

The ADT7490 has four temperature measurement channels: one local, two remote thermal diodes, and a PECI. The local and thermal diode readings are analog temperature measurements, whereas PECI is a digital temperature reading.

PECI Temperature Measurement

The PECI interface is a dedicated thermal interface. The CPU temperature measurement is carried out internally in the CPU. This information is digitized and transferred to the ADT7490 via the PECI interface. The ADT7490 is a PECI host device and therefore, polls the CPU for thermal information.

The PECI measurement differs from traditional thermal diode temperature measurements in that the measurement is a relative value instead of an absolute value. The PECI reading is a negative value that indicates how close the CPU temperature is

Table 14. PECI ERROR INDICATORS

PECI Da- ta	Description	Action
0x8000 to 0x8003	PECI Data Error	Bit 1 of Register 0x43 is set to 1
Invalid FCS	PECI Communications Error	Bit 2 of Register 0x43 is set to 1

Each PECI channel also has an associated status bit to indicate if the PECI high or low limits have been exceeded. An alert is generated on the $\overline{\text{SMBALERT}}$ pin when these status bits are asserted.

Table 15. PECI STATUS BITS

Channel	Register	Bit
PECI0	0x43	0
PECI1	0x81	3
PECI2	0x81	4
PECI3	0x81	5

Temperature Data REPLACE Mode

The REPLACE mode is configured by setting Bit 4 of Register 0x36. In this mode, the data in the existing Remote 1 registers are replaced by PECI0 data. This is a legacy mode that allows the thermal data from CPU1 to be stored in the same registers as in the ADT7476A. This reduces the software changes in systems transitioning from CPUs with thermal diodes to CPUs with a PECI interface. However, note that even though the associated registers are swapped, the correct data format (PECI vs. absolute temperature, see Table 6) must be written to and interpreted from these registers.

Notes

In Table 16, registers listed under the Remote 1 Default column are in absolute temperature format by default and are in PECI format in REPLACE mode. Registers listed under the PECI0 Default column are in PECI format by default and in absolute temperature format in REPLACE mode.

Table 16. REPLACE MODE TEMPERATURE REGISTERS

Register Name	Remote 1 Default	PECI0 Default
Value Register	Reg. 0x25	Reg. 0x33
Low Limit	Reg. 0x4E	Reg. 0x34
High Limit	Reg. 0x4F	Reg. 0x35
T _{MIN}	Reg. 0x67	Reg. 0x3B
T _{RANGE}	Reg. 0x5F, Bits [7:4]	Reg. 0x3C, Bits [7:4]
Enhanced Acoustics	Reg. 0x62, Bits [2:0]	Reg. 0x3C, Bits [2:0]
Enhanced Acoustics Enable	Reg. 0x62, Bit 3	Reg. 0x3C, Bit 3
THERM T _{CONTROL}	Reg. 0x6A	Reg. 0x3D
T _{MIN} Hysteresis	Reg. 0x6D, Bits [7:4] Reg. 0x6D, Bits [3:0] (Note 1)	Reg. 0x6E, Bits [3:0] Reg. 0x6E, Bits [7:4] (Note 1)
Temperature offset	Reg. 0x70	Reg. 0x94
Operating Point for Dynamic T _{MIN}	Reg. 0x8B	Reg. 0x8A

Digital Output (10-bit) (Note 1)
1000 0000 00 (Diode Fault)
1100 0001 00
1100 1110 00
1110 0111 00
1111 0110 00
0000 0000 00

Table 17. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

10.25

switched between I and N1 × I, giving ΔV_{BE1} , and then between I and N2 × I, giving ΔV_{BE2} . The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of any series resistance on

the following equation to calculate the error introduced at a temperature T (°C) when using a transistor whose n_f does not equal 1.008. Refer to the data sheet for the related CPU to obtain the n_f values.

 $\Delta T \,=\, (nf \,-\, 1.008) / 1.008 \,\times\, (273.15 \; \text{K} \,+\, \text{T}) \qquad (\text{eq. 4})$

To factor this in, the user can write the ΔT value to the offset register. The ADT7490 automatically adds it to or subtracts it from the temperature measurement.

• Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7490, I_{HIGH} , is 192 μ A and the low level current, I_{LOW} , is 12 μ A. If the ADT7490 current levels do not match the current levels specified by the CPU manufacturer, it may be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7490, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 12 μ A at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 192 μ A at the lowest operating temperature.
- Base resistance less than 100Ω .
- Small variation in h_{FE}

Table 20. CONVERSION TIME WITH AVERAGING
DISABLED

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x81
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 THERM Temp. Limit	0x64
0x50	Local Temperature Low Limit	0x81
0x51	Local Temperature High Limit	0x7F
0x6B	Local THERM Temperature Limit	0x64
0x52	Remote 2 Temperature Low Limit	0x81
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 THERM Temp. Limit	0x64
0x34	PECI Low Limit	0x81
0x35	PECI High Limit	0x00
0x3D	PECI T _{CONTROL} Limit	0x00

Table 24. TEMPERATURE LIMIT REGISTERS

Table 25. THERM TIMER LIMIT REGISTER

interrupt has cleared. Interrupt status register bits are sticky. Whenever an interrupt status bit is set, indicating an out-of-limit condition, it remains set even if the event that caused it has gone away (until read).

The only way to clear the interrupt status bit is to read the interrupt status register after the event has gone away. Interrupt status mask registers allow individual interrupt sources to be masked from causing an <u>SMBALERT</u> on the

dedicated alert pin. However, if one of these masked interrupt sources goes out of limit, its associated interrupt status bit is set in the interrupt status registers.

Full details of the Interrupt Status and Interrupt Mask registers associated with each measurement channels are detailed in the Table 27 and in the full register map in the Register Tables section.

Table 27. INTERRUPT STATUS AND INTERRUPT MASK REGISTER ADDRESS AND BIT ASSIGNMEN
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Interrupt Status Register	Interrupt Mask Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x41	0x74	OOL	R2T	LT	R1T	+5 V _{IN}	V _{CC}	V _{CCP}	+2.5 V _{IN} /THERM
0x42	0x75	D2 FAULT	D1 FAULT	FAN4/THERM	FAN3	FAN2	FAN1	OOL	+12 V _{IN}
0x43	0x82	OOL	RES	RES	RES	OVT	COM M	DATA	PECI0
0x81	0x83	V _{TT}	I _{MON}	PECI3	PECI2	PECI1	RES	RES	RES

SMBALERT Interrupt Behavior

The ADT7490 can be polled for status, or an <u>SMBALERT</u> interrupt can be generated for out-of-limit conditions. It is important to note how the <u>SMBALERT</u> output and status bits behave when writing interrupt handler software.

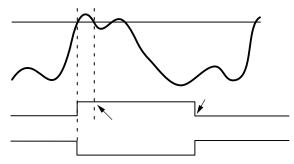


Figure 30. SMBALERT and Status Bit Behavior

Enabling the SMBALERT Interrupt Output

The <u>SMBALERT</u> interrupt function is disabled by default. Pin 10 or Pin 14 can be reconfigured as an <u>SMBALERT</u> output to signal out-of-limit conditions.

Table 28. CONFIGURING PIN 10 AS SMBALERT OUTPUT

Register	Bit Setting
Configuration Register 3 (Register 0x78), Bit 0	[1] Pin 10 = SMBALERT [0] Pin 10 = PWM2 (Default)

Assigning THERM Functionality to a Pin

Pin 14 on the ADT7490 has three possible functions: <u>SMBALERT</u>, <u>THERM</u>, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

If THERM is enabled (Bit 1, Configuration Register 3 at Address 0x78),

- Pin 22 becomes THERM.
- If Pin 14 is configured as THERM (Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D), THERM is enabled on this pin.

If $\overline{\text{THERM}}$ is not enabled,

- Pin 22 becomes a 2.5 V_{IN} measurement input.
- If Pin 14 is configured as THERM, THERM is disabled on this pin.

Bit 1	Bit 0	Function
0	0	TACH4
0	1	THERM
1	0	SMBALERT
1	1	Reserved

Table 29. CONFIGURING PIN 14 IN REGISTER 0x7D

THERM as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the PROCHOT output of a CPU to gauge system performance.

The user can also set up the ADT7490 so that the fans run at 100% when the $\overline{\text{THERM}}$

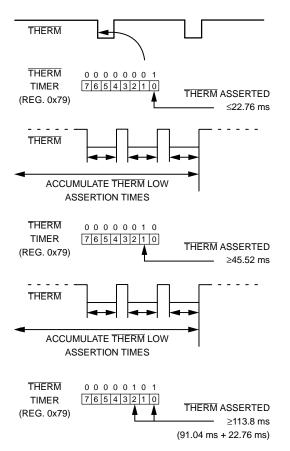


Figure 33. Understanding the THERM Timer

When using the $\overline{\text{THERM}}$ timer, be aware of the following: After a $\overline{\text{THERM}}$ timer read (Register 0x79):

- The contents of the timer are cleared on read.
- Bit 5 of Interrupt Status 2 register (0x42) needs to be cleared (assuming that the THERM timer limit has been exceeded).

If the THERM timer is read during a THERM assertion, the following happens:

- The contents of the timer are cleared.
- Bit 0 of the THERM timer is set to 1, because a THERM assertion is occurring.
- The THERM timer increments from zero.
- If the THERM timer limit (Register 0x7A) = 0x00, the F4P bit is set.

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7490 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 sec (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM

timer value exceeds the THERM timer limit value, the FAN4 bit (Bit 5) of Status Register 2 is set and an SMBALERT is generated.

Note that depending on which pins are configured as a THERM timer, setting the FAN4/THERM bit (Bit 5) of the Interrupt Mask Register 2 (0x75), or bit 0 of the Interrupt Mask Register 1 (0x74), masks out SMBALERT; although the FAN4 bit of Interrupt Status Register 2 is still set if the THERM timer limit is exceeded.

Figure 34 is a functional block diagram of the THERM timer, THERM limit, and its associated circuitry. Writing a value of 0x00 to the THERM Timer Limit register (0x7A) causes an SMBALERT to be generated on the first THERM assertion. A THERM18 NET366.917 582.962 TD.3928 Tw[(F)74.3(AN4) BIOS can read the THERM timer once an hour to determine the cumulative THERM assertion time. If, for example, the total THERM assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and

>2.914 sec in Hour 3, this indicates that system performance is degrading significantly because THERM is asserting more frequently on an hourly basis.

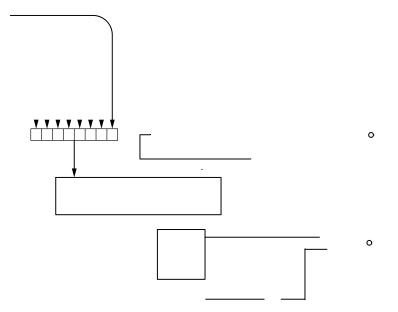


Figure 34. Functional Block Diagram of THERM Monitoring Circuitry

Enabling and Disabling THERM

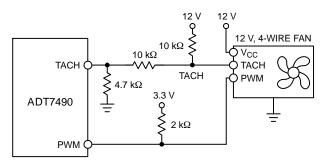


Figure 38. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7490 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is being used in the system, it should be driven from the PWM3 output in parallel with the third fan.

Figure 39 shows how to drive two fans in parallel using low cost NPN transistors. Figure 40 shows the equivalent circuit using a MOSFET.

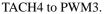
Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure the PWM outputs are not required to source current, and that they sink less than the 5 mA maximum current specified in the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 39 and Figure 40. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4-wire fans.

SYNC, Enhanced Acoustics Register 1 (Register 0x62) Bit 4 (SYNC) = 1, synchronizes TACH2, TACH3, and



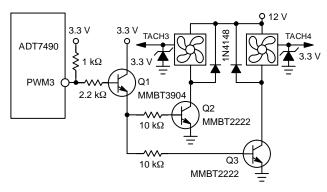


Figure 39. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

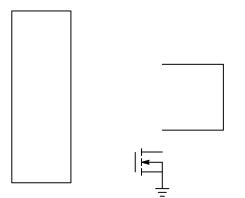


Figure 40. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-channel MOSFET

If the fan output has a resistive pullup to 12 V, or other voltage greater than 3.6 V, the fan output can be clamped with a Zener diode, as shown in Figure 43. The Zener diode voltage should be chosen so that it is greater than $V_{\rm IH}$ of the TACH input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value of between 3.0 V and 3.6 V is suitable.

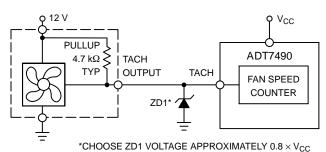


Figure 43. Fan with Strong TACH Pullup to > 3.6 V,

(for Example, 12 V) Clamped with Zener Diode

If the fan has a strong pullup (less than $1 \text{ k}\Omega$) to 12 V or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 44.

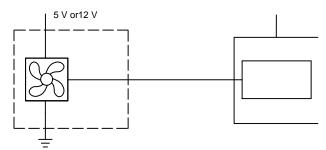


Figure 44. Fan with Strong TACH. Pullup to > V_{CC} or Totem-Pole Output, Clamped with Zener Diode and Resistor

0xFFFF indicates that either the fan has stalled or is running very slowly (<100 RPM).

High Limit > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an <u>SMBALERT</u>.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Table 31. FAN TACH LIMIT REGISTERS

Register

Description

Disabling Fan Startup Timeout

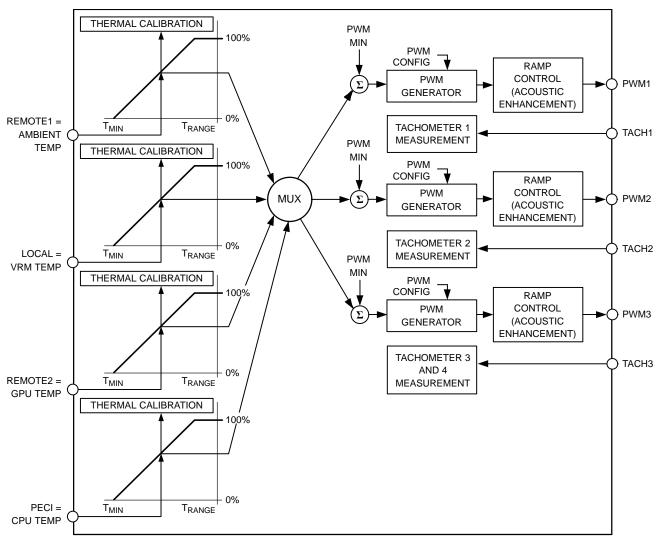


Figure 48. Automatic Fan Control Block Diagram

Step 1: Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

- What ADT7490 functionality is used?
- PWM2 or <u>SMBALERT</u>?
- TACH4 fan speed measurement or overtemperature THERM function?
- 2.5 V_{IN} voltage monitoring or overtemperature THERM function?

The ADT7490 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.

• How many fans are supported in the system, three or four? This influences the choice of whether to use the TACH4 pin or to reconfigure it for the THERM function.

• Is the CPU fan to be controlled using the ADT7490, or will the CPU fan run at full speed 100% of the time?

If run at 100%, it frees up a PWM output, but the system is louder.

• Where is the ADT7490 going to be physically located in the system?

This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7490 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

Step 2: Configuring the Muxtiplexer

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, can be run manually (under software control), or can be run at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits [7:5] (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs, respectively. The values selected for these bits determine how the multiplexer connects a temperature measurement channel to a PWM output.

Automatic Fan Control Multiplexer Options

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) cleared to 0.

000 = Remote 1 temperature controls PWMx

001 = Local temperature controls PWMx

010 = Remote 2 temperature controls PWMx

101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx

110 = Fastest speed calculated by all three temperature channels controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when the Remote 1 temperature exceeds 60° C or if the local temperature exceeds 45° C.

Setting the ALT bit in Register 0x5C, Register 0x5D, and Register 0x5E gives alternative behavior settings for Bits [7:5] of the PWM configuration registers.

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E, with the ALT bit (Bit 3) set to 1.

000 = PECI0 reading controls PWMx

001 = PECI1 reading controls PWMx

010 = PECI2 reading controls PWMx

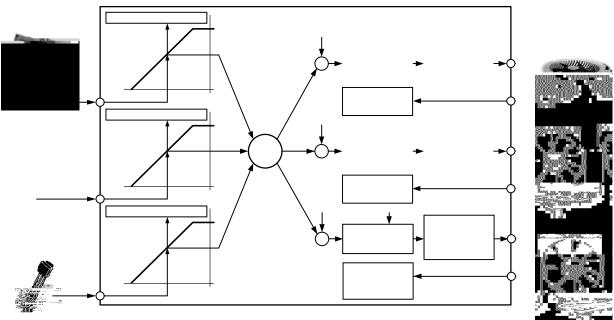
011 = PECI3 reading controls PWMx

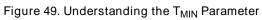
101 = Fastest speed calculated by all four PECI readings controls PWMx

111 = Fastest speed calculated by all thermal zones (Local, Rem1, Rem2 and PECI) controls PWMx

Other Mux Options

Bits [7:5] (BHVR),





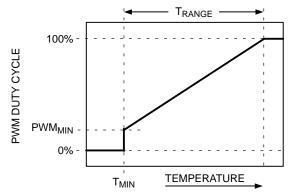


Figure 53. $T_{\mbox{RANGE}}$ Parameter Affects Cooling Slope The T

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, it is also necessary to note that the enhanced acoustics registers (0x62, 0x63, and 0x3C) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means that if T_{RANGE} is programmed with an AFC slope that is quite steep, a relatively small change in temperature could cause a large change in PWM output and possibly an audible change in fan speed, which can be noticeable/annoying to end users.

Decreasing the speed of the PWM output changes by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63) changes how fast the fan speed increases/decreases in the event of a temperature spike. Slowly the PWM duty cycle increases until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 57 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. Figure 57B shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

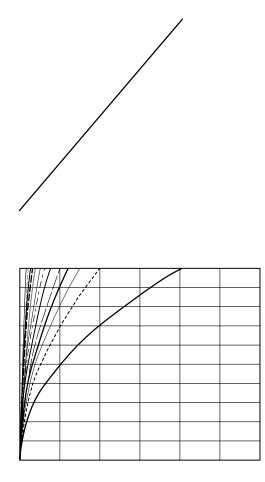


Figure 57. T_{RANGE} vs. Actual Fan Speed (Not PWM Drive) Profile

The T_{THERM} limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any T_{THERM} limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and one should ensure that it is not exceeded under normal system operating conditions.

Note that $T_{\overline{THERM}}$ limits are non-maskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C), can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

Table 43. THERM REGISTERS

Register	Description	Default
0x6A	Remote 1 THERM Limit	0x64 (100°C)
0x6B	Local THERM Limit	0x64 (100°C)
0x6C	Remote 2 THERM Limit	0x64 (100°C)
0x3D	PECI T _{CONTROL} Limit	0x00 (0°C)

THERM Hysteresis

THERM hysteresis on a particular channel is configured via the hysteresis settings in the following section (0x6D and 0x6E). For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 THERM.

Hysteresis Registers

Register 0x6D, Remote 1, Local Hysteresis Register

Bits [7:4], Remote 1 Temperature Hysteresis (4°C default) Bits [3:0], Local Temperature Hysteresis (4°C default)

Register 0x6E, Remote 2, PECI Temperature Hysteresis Register

Bits [7:4], Remote 2 Temperature Hysteresis (4°C default) Bits [3:0], PECI Temperature Hysteresis (4°C default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C, because this disables hysteresis. In effect, this causes the fans to cycle (during a THERM event) between normal speed and 100% speed, or, while operating close to T_{MIN} , between normal speed and off, creating unsettling acoustic noise.

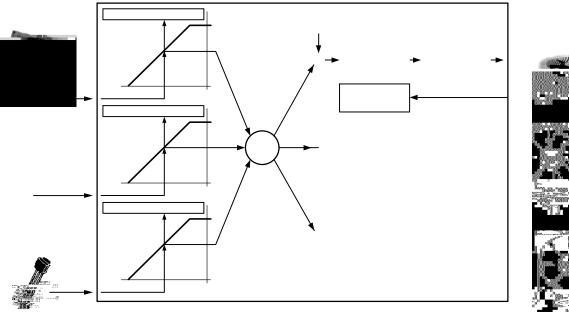


Figure 59. How T_{THERM} Relates to Automatic Fan Control

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (Register 0x10)

Bit 0 (SLOW) = 1, slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4.

Bit 1 (SLOW) = 1, slows the ramp rate for PWM changes associated with the local temperature channel by 4.

Bit 2 (SLOW) = 1, slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Bit 7 (ExtraSlow) = 1, slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp-up times when the SLOW bit is set for each temperature monitoring channel.

Enhanced Acoustics Register 1 (Register 0x62) Bits [2:0] ACOU, selec

Table 44. ADT7490 REGISTERS (continued)

Addr

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	Lock- able
0x4C	R/W	+12V _{IN} Low Limit	7	6	5	4	3	2	1	0	0x00	-
0x4D	R/W	+12V _{IN} High Limit	7	6	5	4	3	2	1	0	0xFF	-
0x4E	R/W	Remote 1 Temp Low Limit	7									

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	Lock- able
0x62	R/W	Enhanced Acoustics Reg. 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0x00	Yes
0x63	R/W	Enhanced Acoustics Reg. 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 Temp. T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x68	R/W	Local Temp. T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x69	R/W	Remote 2 Temp. T _{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x6A	R/W	Remote 1 THERM Temp. Limit	7	6	5	4	3	2	1	0	0x64	Yes

0x6B R/W

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	Lock- able
0x76	R	Extended Resolution 1	+5V _{IN}	+5V _{IN}	V _{CC}	V _{CC}	V _{CCP}	V _{CCP}	+2.5V _{IN}	+2.5V _{IN}	0x00	_

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De- fault	Lock- able
0x8F	R/W	Dynamic T _{MIN} Control Reg. 2	CYR2	CYR2	CYL	CYL	CYL	CYR1	CYR1	CYR1	0x00	Yes
0x90	R/W	Dynamic T _{MIN} Control Reg. 3	PECI	PHTP	CYP	CYP	CYP	RES	RES	RES	0x00	Yes
0x94	R/W	PECI0 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x95	R/W	PECI1 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x96	R/W	PECI2 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x97	R/W	PECI3 Temp. Offset	7	6	5	4	3	2	1	0	0x00	Yes
-	0x41	-	-	0x74	OOL	R2T	LT	R1T	+5V _{IN}			

Table 46. REGISTER 0x11 - CONFIGURATION REGISTER 7 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	THERMHys	R/W	THERM hysteresis is enabled by default. Setting this bit to 1 disables THERM hysteresis.
[1]	FSPD	R/W	When set to 1, this bit runs all fans at maximum speed as programmed in the maximum PWM duty cycle registers (0x38 to 0x3A). Power-on default = 0. This bit is not locked at any time.
[2]	Vx1	R/W	BIOS should set this bit to 1 when the ADT7490 is configured to measure current from an ADOPT VRM controller and to measure the CPU core voltage. This bit allows monitoring software to display CPU watts usage. (Lockable.)
[3]	FSPDIS	R/W	Logic 1 disables fan spin-up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin-up timeout selected.
[4]	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. In this state, if at any point during an SMBus transaction involving the ADT7490 activity ceases for more than 35 ms, the ADT7490 assumes the bus is locked and releases the bus. This allows the ADT7490 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable.)
[7:5]	RES	N/A	Reserved. Do not write to these bits.

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 51. TEMPERATURE READING REGISTERS (POWER-ON DEFAULT = 0x80) (Note 1 and 2)

Register Address	R/W	Description
0x25	Read-only	Remote 1 Temperature Reading (Note 3 and 4) (8 MSBs of Reading)
0x26	Read-only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read-only	Remote 2 Temperature Reading (Note 3 and 4) (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (Register 0x76, Register 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.

 These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).

3. In twos complement mode, a temperature reading of -128°C (0x80) indicates a diode fault (open or short) on that channel.

4. In Offset 64 mode, a temperature reading of -64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 52. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0x00) (Note 1)

Register Address	R/W	Description
0x28	Read-only	TACH1 Low Byte
0x29	Read-only	TACH1 High Byte
0x2A	Read-only	TACH2 Low Byte
0x2B	Read-only	TACH2 High Byte
0x2C	Read-only	TACH3 Low Byte
0x2D	Read-only	TACH3 High Byte
0x2E	Read-only	TACH4 Low Byte
0x2F	Read-only	TACH4 High Byte

 These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH Pulses per Revolution register (Register 0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte must

Table 56. REGISTER 0x36 – PECI CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[2:0]	AVG[2:0]	R/W	$\begin{array}{l} PECI Smoothing Interval. These bits set the duration over which smoothing is carried out on the PECI data read. Note that the PECI smoothing interval is equal to the PECI register update interval. The smoothing interval is calculated using the following formula: $
			Bit Code Number of PECI Readings 000 16 001 2048 010 4096 011 8192 100 16384 101 32768 110 65536 111 Reserved
[3]	DOM0	R/W	CPU Domain Count information. Set to 0 indicates that CPU 1 associated with the PECI0 reading has a single domain (default). Set to 1 indicates that the system CPU 1 contains two domains.
[4]	REPLACE	R/W	If this bit is set to 0, it indicates that the ADT7490 is operating in standard mode. If this bit is set to 1, the Remote 1 Temperature register (Register 0x25) is overwritten by PECI0 information (Register 0x33) and vice versa. Note that in this mode, all associated user programmable limit and fan control registers are also swapped and should be programmed in the appropriate PECI or absolute temperature format.
[7:5]	RES		

Table 60. T_{CONTROL} LIMIT REGISTER (POWER-ON DEFAULT = 0x00) (Note 1)

Register Address	R/W (Note 2)	Description
0x3D	R/W	PECI T _{CONTROL} Limit

 If any PECI reading exceeds the T_{CONTROL} limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below T_{CONTROL} limit – hysteresis.

 This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 61. REGISTER 0x3F - VERSION REGISTER

Bit No.	Mnemonic	R/W	Description
[1:0]	REV[1:0]	Read-only	These two bits indicate the ADT7490 silicon revision number. 0x00 indicates Revision 0, 0x01 indicates Revision 1, and so on. 0x11 indicates that further revision information can be found in the "Extended Revision" register (0x12). The revision number is then found by adding 0x11 to the contents of the extended revision register.
[2]	PECI	Read-only	This bit is set to 1 indicating that the ADT7490 supports the PECI interface.
[3]	4-wire	Read-only	This bit is set to 1 indicating that the ADT7490 may be configured to drive 4-wire fans using high frequency PWM.
[7:4]	VER[3:0]	Read-only	These bits indicate the version number of the device. This is set to 6, indicating that the ADT7490 is part of the Heceta 6 ASIC family.

Table 62. REGISTER 0x40 – CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0x04)

Table 63. REGISTER 0x41 – INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W		Description
[0]	+2.5 V _{IN} / THERM	Read-only	+2.5 V_{IN} = 1 indicates that the 2.5 V_{IN}	

Table 65. REGISTER 0x43 - INTERRUPT STATUS REGISTER 3 (POWER-ON DEFAULT = 0x00)

Table 68. FAN TACHOMETER LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x34	R/W	PECI Low Limit	0x81
0x54	R/W	TACH1 Minimum Low Byte	0xFF
0x55	R/W	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	R/W	TACH2 Minimum Low Byte	0xFF
0x57	R/W	TACH2 Minimum High Byte	0xFF
0x58	R/W	TACH3 Minimum Low Byte	0xFF
0x59	R/W	TACH3 Minimum High Byte	0xFF
0x5A	R/W	TACH4 Minimum Low Byte	0xFF
0x5B	R/W	TACH4 Minimum High Byte	0xFF

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 (0x42) to indicate fan failure. Setting the Configuration Register 1 (0x40) Lock bit has no effect on these registers.

Table 69. REGISTER 0x55 – TACH1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0xFF)

Bit No.	Mnemonic	R/W	Description
[3:0]	Reserved	Read-only	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are reserved. Otherwise, these bits represent Bits [3:0] of the TACH1 minimum high byte.
[7:4]	SCADC	R/W	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits

Table 73. REGISTER 0x5F, REGISTER 0x60, AND REGISTER 0x61 – REMOTE 1 T _{RANGE} /PWM1 FREQUENCY,
LOCAL T _{RANGE} /PWM2 FREQUENCY, AND REMOTE 2 T _{RANGE} /PWM3 FREQUENCY (POWER-ON DEFAULT = 0xC4)

Bit No.	Mnemonic	R/W (Note 1)		Description
[2:0]	FREQ	R/W	These bits control mode).	the PWMx frequency (only apply when PWM channel is in low frequency
			Bit Code	Frequency
			000 001 010 011 100 101 110 111	11.0 Hz 14.7 Hz 22.1 Hz 29.4 Hz 35.3 Hz (Default) 44.1 Hz 58.8 Hz 88.2 Hz
[3]	HF/LF	R/W		equency PWM mode is enabled for PWMx. quency PWM mode is enabled for PWMx.
[7:4]	RANGE	R/W	These bits determin control. Bit Code 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1011 1010 1011 1110 1111	Temperature 2°C 2.5°C 3.33°C 4°C 5°C 6.67°C 8°C 10°C 13.33°C 16°C 20°C 26.67°C 32°C (Default) 40°C 53.33°C

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set. Any further attempts to write to this register have

Table 74. REGISTER 0x62 – ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0x00)

R/W Bit No. Mnemonic

Table 75. REGISTER 0x63 – ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[2:0]	ACOU2	R/W	Assuming that PWMx is associated with the local temperature channel, these bits define the maximum rate of change of the PWMx output for local temperature-related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.
			When Bit 7 of Configuration Register 6 (0x10) is 0
			Bit Code Time for 0% to 100%
			$000 = 1$ $37.5 \sec$ $001 = 2$ $18.8 \sec$ $010 = 3$ $12.5 \sec$ $011 = 4$ $7.5 \sec$ $100 = 8$ $4.7 \sec$ $101 = 12$ $3.1 \sec$ $110 = 24$ $1.6 \sec$ $111 = 48$ $0.8 \sec$
			When Bit 7 of Configuration Register 6 (0x10) is 1
			Bit Code Time for 0% to 100%
			$000 = 1$ $52.2 \sec$ $001 = 2$ $26.1 \sec$ $010 = 3$ $17.4 \sec$ $011 = 4$ $10.4 \sec$ $100 = 8$ $6.5 \sec$ $101 = 12$ $4.4 \sec$ $110 = 24$ $2.2 \sec$ $111 = 48$ $1.1 \sec$
[3]	EN2	R/W	When this bit is 1, smoothing is enabled on the local temperature channel.
[6:4]	ACOU3	R/W	Assuming that PWMx is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 2 Temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.
[7]	EN3	R/W	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 76. PWM MINIMUM Db1G.e5422YCLEISTERhaverature735.395 0 0 8 21fl.

Table 78. T_{MIN} REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x67	R/W	Remote 1 Temperature T _{MIN}	0x5A (90°C)
0x68	R/W	Local Temperature T _{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 Temperature T _{MIN}	0x5A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at

minimum speed and increases with temperature according to T_{RANGE}. These registers become read-only when the Configuration Register 1 (0x40) Lock bit is set. Any further attempts to write to these registers 2. have no effect.

Table 79. THERM LIMIT REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x6A	R/W	Remote 1 THERM Temperature Limit	0x64 (100°C)
0x6B	R/W	Local THERM Temperature Limit	0x64 (100°C)
0x6C	R/W	Remote 2 THERM Temperature Limit	0x64 (100°C)

1. If any temperature measured exceeds its THERM limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical over temperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below THERM limit – hysteresis. If the THERM pin is programmed as an output, exceeding these limits by 0.25°C can cause the THERM pin to assert low as an output.

2. These registers become read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to these registers have no effect.

Table 82. REGISTER 0x6E – REMOTE 2 AND PECI TEMPERATURE/T_{MIN} HYSTERESIS (POWER-ON DEFAULT = 0x44)

Bit No. (Note 1)	Mnemonic	R/W (Note 2)	Description
[3:0]	HYSP	R/W	PECI temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the PECI AFC control loops.
[7:4]	HYSR2	R/W	Remote 2 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC control loops.

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} – hysteresis. Up to <u>15°C of</u> hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its <u>THERM</u> limit is exceeded. The PWM output being controlled goes to 100%, if the <u>THERM</u> limit is exceeded and remains at 100% until the temperature drops below <u>THERM</u> – hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.

2. These registers become read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to these registers have no effect.www.

Table 87. REGISTER 0x73 - CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description	
0	FanPresDT	R/W	When FanPresDT = 1, the state of Bits [3:1] of this register reflects the presence of a 4-wire fan on the appropriate TACH channel.	
1	Fan1Detect	Read-only	Fan1Detect = 1 indicates that a 4-wire fan is connected to the PWM1 input.	
2	Fan2Detect	Read-only	Fan2Detect = 1 indicates that a 4-wire fan is connected to the PWM2 input.	
3	Fan3Detect	Read-only	Fan3Detect = 1 indicates that a 4-wire fan is connected to the PWM3 input.	
4	AVG	R/W	AVG = 1 indicates that averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster (x16).	
5	ATTN	R/W	ATTN = 1 indicates that the ADT7490 removes the attenuators from the +2.5 V_{IN} , V_{CCP} , +5 V_{IN} , and +12 V_{IN} inputs. These inputs can be used for other functions such as connecting up external sensors. It is also possible to remove attenuators from individual channels using Bits [7:4] of Configuration Register 4 (0x7D).	
6	CONV	R/W	CONV = 1 indicates that the ADT7490 is put into a single-channel ADC conversion mode. In this mode, the ADT7490 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits [7:4] of TACH1 minimum high byte register (0x55).When CONV = 1, Bits [7:4], Register 0x55Bit CodeADC Channel Selected0000+2.5 V _{IN} 0001V _{CCP} 0010V _{CCC} 0011+5 V _{IN}	
			0100 +12 V _{IN} 0101 Remote 1 Temperature 0110 Local Temperature 0111 Remote 2 Temperature CCP CCP	

Table 89. REGISTER 0x75 - INTERRUPT MASK REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	+12 V _{IN}	R/W	When Pin 21 is configured as a +12 V_{IN} input, +12 V_{IN} = 1 masks SMBALERT for out-of-limit conditions on the +12 V_{IN} channel.
[1]	OOL	R/W	OOL = 1 masks SMBALERT assertions when the OOL status bit is set. Note that the OOL mask bit is independent of the individual mask bits in Interrupt Mask Register 3 (0x82). Therefore, if the intention is to mask SMBALERT assertions for any of the Interrupt Status Register 4 bits, OOL must also be masked.
[2]	FAN1	R/W	FAN1 = 1 masks SMBALERT for a Fan 1 fault.
[3]	FAN2	R/W	FAN2 = 1 masks SMBALERT for a Fan 2 fault.
[4]	FAN3	R/W	FAN3 = 1 masks SMBALERT for a Fan 3 fault.
[5]	Fan4/ THERM	R/W	If Pin 14 is configured as TACH4, Fan4/THERM = 1 masks SMBALERT for a Fan 4 fault. If Pin 14 is configured as THERM, Fan4/THERM = 1 masks SMBALERT for an exceeded THERM timer limit.
[6]	D1 FAULT	R/W	D1 = 1 masks SMBALERT for a diode open or short on a Remote 1 channel.
[7]	D2 FAULT	V31763467.5	D2 = 10 masks SMBALERT for a 60.55 de open or shoet 2 chaotnel. 519.5.452

Tm.0

Table 90. REGISTER 0x76 - EXTENDED RESOLUTION REGISTER 1 (POWER-ON DEFAULT = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[1:0]	+2.5 V _{IN}	Read-onlyR/	N

Table 92. REGISTER 0x78 - CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description			
[0]	ALERT Enable	R/W	ALERT = 1, Pin 10 (PWM2/SMBALERT) is configured as an SMBALERT interrupt output to indicate out-of-limit error conditions. ALERT = 0, Pin 10 (PWM2/SMBALERT) is configured as the PWM2 output.			
[1]	THERM/ +2.5V _{IN}	R/W	ALERT = 1, Pin 10 (PWM2/SMBALERT) is configured as an SI indicate out-of-limit error conditions. ALERT = 0, Pin 10 (PWM2/SMBALERT) is configured as the PTHERM = 1 enables THERM functionality on Pin 22 and Pin 14 THERM, determined by Bit 0 and Bit 1 (Pin 14 Func) of Config When THERM is asserted, if the fans are running and the BOC at full speed. Alternatively, THERM can be programmed so that how long THERM has been asserted.THERM = 0 enables $\pm 2.5V_{IN}$ measurement on Pin 22 and disat Configuration Register 5 (0x7C) are set, THERM is bidirectional. timer input only.Pin 14 Func (0x7D)THERM/ $\pm 2.5V_{IN}$ (0x78)Pin 22 Pin 22 		of Configuration Re d the BOOST bit is s ned so that a timer is and disables THER	gister 4 (0x7D). set, then the fans run s triggered to time M. If Bits [5:7] of
[2]	BOOST	R/W			of THERM causes a	all fans to run at the

Table 95. REGISTER 0x7B - TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0x55)

Bit No.	Mnemonic	R/W	Description
[1:0]	FAN1	R/W	Sets number of pulses to be counted when measuring Fan 1 speed. Can be used to

Table 97. REGISTER 0x7D - CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[1:0]	Pin 14 Func	R/W	These bits set the functionality of Pin 14. 00 = TACH4 (Default) 01 = THERM 10 = SMBALERT 11 = Reserved	
[2]	THERM Disable	R/W	THERM Disable = 0 enables THERM overtemperature output assuming THERM is correctly configured (0x78, 0x7C, and 0x7D). THERM Disable = 1 disables THERM overtemperature output on all channels. THERM can also be disabled on any channel by:	

Table 101. REGISTER 0x81 – INTERRUPT STATUS REGISTER 4 (POWER-ON DEFAULT = 0x00)

Bit No. Mnemonic R/W

Description

Table 105. REGISTER 0x88 – PECI CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No. Mnemonic R/W

Table 108. REGISTER 0x8F – DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description		
[2:0]	CYR1	R/W	3-bit Remote 1 Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel in terms of number of monitoring cycles. The system has associated thermal time constants that be found to optimize the response of fans and the control loop.		or the Remote 1 channel in terms of ociated thermal time constants that need to
			Bit Code	Decrease Cycle	Increase Cycle
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[5:3]	CYL	R/W	3-bit Local Temperature Cycle Value. These three bits define the subsequent T_{MIN} adjustments in the control loop for the local tem number of monitoring cycles. The system has associated thermal be found to optimize the response of fans and the control loop.		or the local temperature channel in terms of ociated thermal time constants that need to
			Bit Code	Decrease Cycle	Increase Cycle
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[7:6]	CYR2	R/W	2 LSBs of 3-bit Remote 2 Cycle Value. The MSB of the 3-bit code resides T _{MIN} Control Register 1 (Register 0x8E). These three bits define the dela making subsequent T _{MIN} adjustments in the control loop for the Remote of number of monitoring cycles. The system has associated thermal time to be found to optimize the response of fans and the control loop.		ree bits define the delay time between bloop for the Remote 2 channel in terms ssociated thermal time constants that need
			Bit Code	Decrease Cycle	Increase Cycle
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 109. REGISTER 0x90 – DYNAMIC T_{MIN} CONTROL REGISTER 3 (POWER-ON DEFAULT = 0x00)

Bit No.	Mnemonic	R/W (Note 1)		Descriptio	n
[2:0]	RES	Reserved	Reserved		
[5:3]	CYP	R/W	3-bit PECI Temperature Cycle Value. These three bits define the delay time between making subsequent T_{MIN} adjustments in the control loop for the PECI temperature channels in terms of number of monitoring cycles. The system has associated thermal time constants that need to be found to optimize the response of fans and the control loop.		
			Bit Code	Decrease Cycle	Increase Cycle
			000 001 010 011 100 101 110 111	8 cycles (1 sec) 16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec)	16 cycles (2 sec) 32 cycles (4 sec) 64 cycles (8 sec) 128 cycles (16 sec) 256 cycles (32 sec) 512 cycles (64 sec) 1024 cycles (128 sec) 2048 cycles (256 sec)
[6]	PHTP	R/W	PHTR1 = 1 copies the PECI0 current reading to the PECI operating point register is asserted. The operating point contains the temperature at which THERM is ass allowing the system to run as quietly as possible without affecting system perform PHTR1 = 0 ignores any THERM assertions on the THERM pin. The PECI operatin register reflects its programmed value. PECI = 1 enables dynamic T _{MIN} control on the PECI temperature channel. The channel is dynamically adjusted based on the current temperature, operating point, a and low limits for this zone. PECI = 0 disables dynamic T _{MIN} control. The T _{MIN} value chosen is not adjusted a channel behaves as described in the Automatic Fan Control Overview section.		erature at which THERM is asserted, thout affecting system performance.
[7]	PECI	R/W			temperature, operating point, and high value chosen is not adjusted and the

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 110. REGISTER 0x94 - PECI0 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI0 channel measurements. The programmable offset range is from -63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 111. REGISTER 0x95 - PECI1 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0x00)

Bit No.	R/W (Note 1)	Description	
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI1 channel measurements. The programmable offset range is from -63° C to $+127^{\circ}$ C with 1° C resolution.	

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 112. REGISTER 0x96 – PECI2 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0x00)

Bit No.	R/W (Note 1)	Description	
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI2 channel measurements. The programmable offset range is from -63° C to $+127^{\circ}$ C with 1° C resolution.	

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 113. REGISTER 0x97 - PECI3 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0x00)

Bit No.	R/W (Note 1)	Description
[7:0]	R/W	Allows a temperature offset to be automatically applied to the PECI3 channel measurements. The programmable offset range is from –63°C to +127°C with 1°C resolution.

1. This register becomes read-only when the Configuration Register 1 (0x40) Lock bit is set to 1. Any further attempts to write to this register have no effect.

Table 114. ORDERING INFORMATION

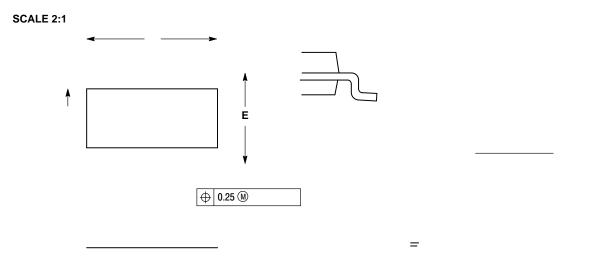
Device Order Number*	Package Type	Package Option	Shipping [†]
ADT7490ARQZ-REEL	24-lead QSOP	RQ-24	2,500 Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. *This is a Pb-Free package.

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