Mic o-S e ing S e e Mo o B idge Con olle

Introduction

The AMIS 30422 is a micro-stepping stepper motor bridge controller for large current range bipolar applications. The chip interfaces via a SPI interface with an external controller in order to control two external power NMOS H bridges. It has an on-chip voltage regulator, current sensing, self adapting PWM controller and pre-driver with smart slope control switching allowing the part to be EMC compliant with industrial and automotive applications. It uses a proprietary PWM algorithm for reliable current control.

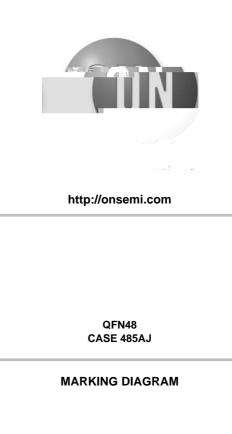
The AMIS 30422 contains a current translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (direction) register or input pin. The chip provides a so-called "Speed and Load Angle" output. This allows the creation of stall detection algorithms and control loops based on load angle to adjust torque and speed.

The AMIS 30422 is implemented in a mature technology, enabling fast high voltage analog circuitry and multiple digital functionalities on the same chip. The chip is fully compatible with automotive voltage requirements.

The AMIS 30422 is easy to use and ideally suited for large current stepper motor applications in the automotive, industrial, medical and marine environment. With the on chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

Key Features

- Dual H Bridge Pre Drivers for 2 Phase Stepper Motors
- Programmable Current via SPI
- On chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- 9 Step Modes from Full Step up to 128 Micro Steps
- Current Sense via Two External Sense Resistors
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 3.3 V Microcontrollers
- Integrated 3.3 V Regulator to Supply External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- Integrated Watchdog Function
- These Devices are Pb Free and are RoHS Compliant



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 44 of this data sheet.

BLOCK DIAGRAM

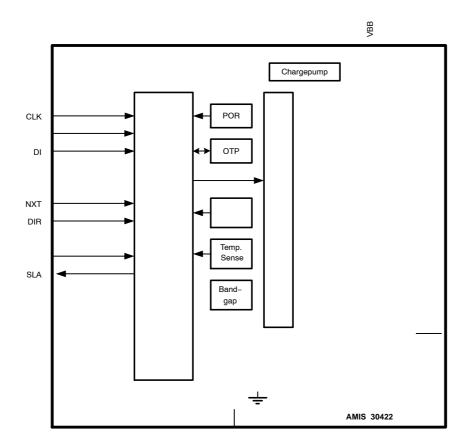
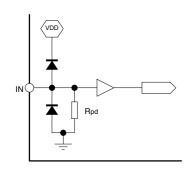
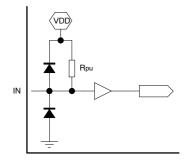


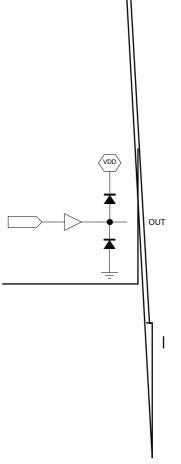
Figure 1. Block Diagram AMIS 30422

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.







ELECTRICAL SPECIFICATION

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Parameter	Min	Max	Unit
V _{BB}	Analog DC supply voltage (Note 3)	-0.3	+40	V
I _{load}	Logic supply external load current, Normal Mode	0	-10	mA
	Logic supply external load current, Sleep Mode	0	-1	mA

V_{RSENS}

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Тур	Мах	Unit
SUPPLY & V	OLTAGE R	EGULATOR					
V _{BB}	VBB	Nominal operating supply range		6		30	V
I _{BB}		Total internal current consumption	Unloaded outputs, internal consumption included, H-bridge disabled			20	mA
I _{SLEEP}		Sleep mode current consumption	Unloaded outputs, CSb = V_{DD}			150	μΑ
V _{DD}	VDD	Regulated Output Voltage	–10 mA ≤ I _{load} ≤ 0 mA	3.1	3.3	3.5	V
V_{DD_SLEEP}		Regulated Output Voltage in Sleep	$-1 \text{ mA} \le I_{\text{load}} \le 0 \text{ mA}$	2.1	2.95	3.63	V

Table 4. DC PARAMETERS

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Symbol

Remark/Test Conditions Min Typ Max Unit

Table 5. AC PARAMETER The AC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.

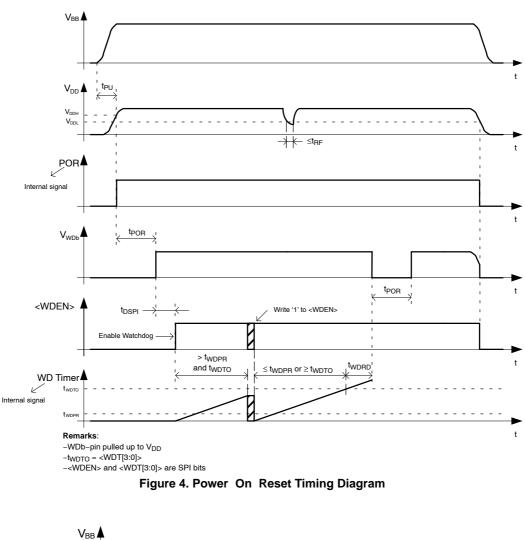
Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Тур	Max	Unit
DIGITAL INP	UTS						
t _{NXT_HI}		NXT Minimum, high pulse width		625			ns
t _{NXT_LO}		NXT Minimum, low pulse width		625			ns
t _{DIR_SET}		NXT set up time, following change of DIR or <dirctrl></dirctrl>		1.28			μs
t _{DIR_HOLD}		NXT hold time, before change of DIR or <dirctrl></dirctrl>		1.28			μs
t _{SLP_SET}		<slp> set up time</slp>	See Figure 6	300			μs
t _{SLP_HOLD}				1			μs
t _{MOTEN_SET}				1			μs
^t мотел_но LD	+O <moten> hold time</moten>			1.28			μs
t _{MSP}		<msp[7:0]> update delay</msp[7:0]>				1.28	μs
CLEAR FUN	CTION			•	•	•	

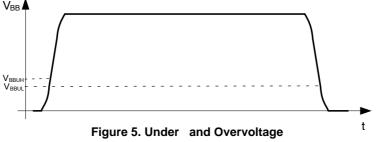
t _{CLR_SE}		Clear set up time	See Figure 7	40		μs
t _{CLR}	ULN	Clear duration time	See Figure 7	20	90	μs

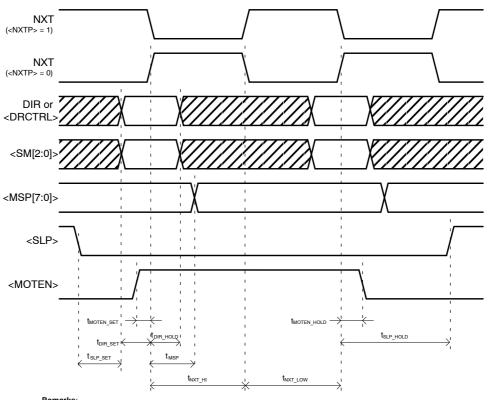
DIGITAL OUTPUTS

 t_{H2L}

AMIS 30422



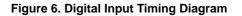




Remarks:

-CDIRCTRL>, <SM[2:0]>, <MSP[7:0]>, <SLP>, <MOTEN> and <NXTP> are SPI bits -Timing for SPI bits starts after CS is high

-T_{SLP_SET} only relates to the digital inputs pins DIR and NXT



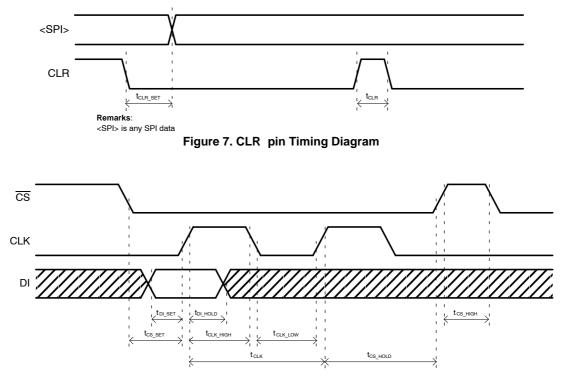


Figure 8. SPI Bus Timing Diagram

TYPICAL APPLICATION SCHEMATIC

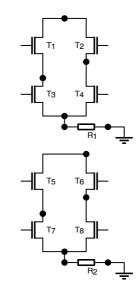


Figure 9. Typical Application Schematic AMIS 30422

FUNCTIONAL DESCRIPTION

H Bridge Pre Drivers The H bridge pre drivers for external N type MOSFETs

PWM Current Control

A PWM comparator compares continuously the actual winding current (measured over the external sense resistor) with the requested

Programmable Peak Current

The amplitude of the current waveform in the motor coils (I_{max}) can be programmed through SPI bits <CUR[2:0]>. The coil current can be calculated as next:

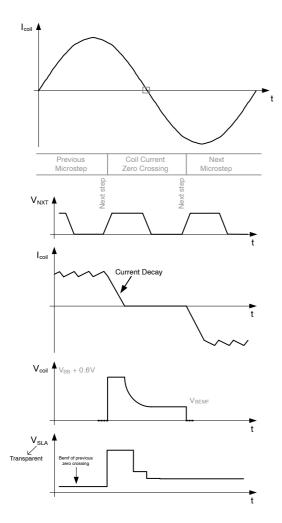
$$I_{max} = \langle CUR[2:0] \rangle / R_{SENSE}$$

R_{SENSE} is resistor R₁ and R₂ as given in Figure 9, <CUR[2:0]> is dependant on the REF pin voltage. This makes it possible to set the coil current by means of SPI commands or by adjusting the REF pin voltage. See also page 35.

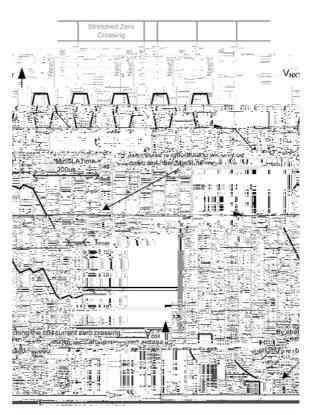
A change in the coil current (<CUR[2:0]>) will be updated at the next PWM cycle.

Hold Current Setting

A second coil current value can be programmed which is called the Hold Current (<HOLD_CUR[2:0]>). By enabling this functionality (<EN_HOLD> = 1), AMIS 30422 will automatically change the coil current to the programmed Hold Current value when no NXT pulse is detected for a time longer than the specified <HOLD_TIME[1:0]>. From the moment a NXT pulse is detected, AMIS







2 Demostry Munic Selfer Asian the anti-mercial contractor second

Figure 20. BEMF sampling without (left) and with (right) zero crossing stretching

....

Sleep Mode

AMIS 30422 can be placed in Sleep Mode by means of SPI bit <SLP>. This mode allows reduction of current consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low power mode
- All SPI registers maintain their logic content
- SPI communication is still possible (slightly current increase during SPI communication).
- ٠

WARNING, ERROR DETECTION AND DIAGNOSTICS FEEDBACK

Thermal Warning and Shutdown

AMIS 30422 has 4 thermal ranges which can be read out through SPI bits <TR[1:0]> and <TSD>. Thermal Range 1 goes from 40°C up to T₁. Thermal Range 2 goes from T₁ to T₂ and Thermal Range 3 goes from T₂ up to T₃ (T₁, T₂ and T₃ can be found in Table 4). Once above T₃ the 4th thermal level is reached which is the thermal warning range.

When junction temperature rises above T_{TW} (= T_3), the ERRb pin will be activated. If junction temperature increases above thermal shutdown level (T_{TSD}), then the circuit goes in Thermal Shutdown Mode and all driver transistors are disabled (high impedance). The condition to get out of the Thermal Shutdown Mode is to be at a temperature lower than T_{TW} and by clearing the <TSD> SPI bit.

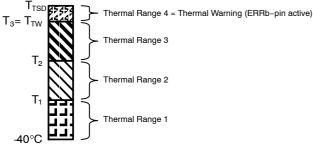


Figure 21. Thermal Ranges

Over Current Detection

The over current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over current detection threshold, the ERRb pin will be activated and the drivers are switched off (motor driver disabled) to reduce the power dissipation and to protect the H bridge. Each driver has an individual detection bit (see Status Register 1 and 2). The error condition is latched and the microcontroller needs to read out the error to reset the error and to be able to re enable the motor driver again. Note: Successive resetting the motor driver in case of a short circuit condition may damage the drivers.

Open Coil/Current Not Reached Detection

Open coil detection is based on the observation of 100% duty cycle of the PWM regulator. If in a coil 100% duty cycle is detected for a certain time, an open coil will be latched (see Status Register 1 and 2) and the ERRb pin will be activated (drivers are disabled). The time this 100% duty cycle needs to be present is adjustable with SPI bits <OPEN_COIL[1:0]>. A short time will result in fast detection of an open coil but could also trigger unwanted open coil errors. Increase the timing if this is the case.

When the resistance of a motor coil is very large and the supply voltage is low, it can happen that the motor driver is not able to deliver the requested current to the motor. Under these conditions the PWM controller duty cycle will be 100% and the ERRb pin will flag this situation. This feature can be used to test if the operating conditions (supply voltage, motor coil resistance) still allow reaching the requested coil current or else the coil current should be reduced.

Note: A short circuit could trigger an open coil.

Charge Pump Failure

The charge pump is an important circuit that guarantees low $R_{DS(on)}$ for all external MOSFET's, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee a low $R_{DS(on)}$ of the drivers, a charge pump failure is latched (<CPFAIL>), the ERRb pin is activated and the driver is disabled (<MOTEN> = '0'). One needs to read Status Register 1 to clear the charge pump failure.

After power on reset (POR) the charge pump voltage will need some time to exceed the required threshold. During that time the ERRb pin will be active but not latched for 250 μ s. If the slope of the power supply V_{BB} is slow during power up (charge pump not started after 250 μ s), a charge pump failure will be latched and the ERRb pin is activated (see also Figure 22).

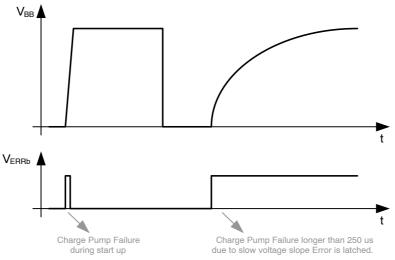


Figure 22. Charge Pump Failure

Watchdog

When V_{BB} is applied, the WDb pin is kept low for t_{por} (Table 5). This can for instance be used to reset an external microcontroller at power up.

The WDb pin also has a second function, a Watchdog function. When the watchdog is enabled ($\langle WDEN \rangle = '1'$), a timer will start counting up. When the counter reaches a certain value ($\langle WDT[3:0] \rangle$), the $\langle WD \rangle$ SPI bit will be set and the WDb pin will be pulled low for a time equal to t_{POR} to reset the external microcontroller. To avoid that the microcontroller gets reset, the microcontroller needs to re enable the watchdog before the count value is reached (= write '1' to $\langle WDEN \rangle$ before $\langle WDT[3:0] \rangle$ is reached). This functionality can be used to reset a "stuck" microcontroller.

The SPI bit <WD> can be used to detect a cold or warm boot. When powering the application (cold boot), <WD> will be zero. If the microcontroller has been reset by the WDb pin (warm boot), <WD> bit will be '1'. The microcontroller can use this information to detect a cold or warm boot.

It's forbidden to re enable the watchdog too fast (minimum time between re enabling must be above t_{WDPR} (see Figure 4)). One may also not enable the watchdog too fast after power up (see t_{DSPI} , Figure 4).

A small analogue filter avoids resetting due to spikes or noise on the VDD supply $(t_{\text{rf}}).$

During and after power up the WDb pin is an open drain output. One can change this to a push pull output by using SPI bit <IO_OT>.

Error Output

The error output (ERRb pin) will be activated if an error is reported. Next errors will be reported:

- Thermal Warning
- Thermal Shutdown
- Overcurrent
- Open Coil
- Charge Pump Failure
- All errors except a Thermal Warning will disable the H bridge drivers to protect the motor driver (<MOTEN> = '0'). To reset the error one needs to read out the error. Only when all errors are reset it will be possible to re enable the motor driver (<MOTEN> = '1').

Keep in mind that during power up a charge pump failure will be reported during the first 250us but will not be latched (see also Charge Pump Failure).

During and after power up the ERRb pin is an open drain output. One can change this to a push pull output with SPI bit <IO_OT>.

POWER SUPPLY AND THERMAL CALCULATION

Logic Supply Regulator

AMIS 30422 has an on chip 3.3 V low drop regulator to supply the digital part of the chip itself, some low voltage analog blocks and external circuitry. See Table 4 for the limitations.

Undervoltage

AMIS 30422 has undervoltage detection. If V_{BB} drops below V_{BBUL}

SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS 30422. The implemented SPI block is designed to interface directly with numerous microcontrollers from several manufacturers. AMIS 30422 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS 30422), and DI signal is the output from the Master. A chip select line (CSb) allows individual selection of a Slave SPI device in a multiple slave system. The CSb line is active low. If AMIS 30422 is not selected, DO is in HiZ and does not interfere with SPI bus activity. The output type of DO can be set in SPI (<IO_OT>). Since AMIS 30422 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

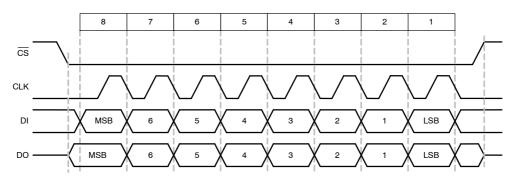


Figure 23. Timing Diagram of a SPI Transfer

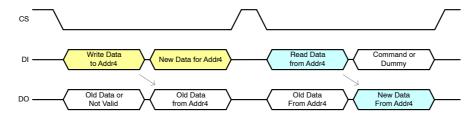
Transfer Packet

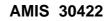
Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS 30422 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS 30422 in a READ operation.

After a WRITE operation the Master could initiate a READ command in order to verify the data correctly written as illustrated in Figure 28. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is

transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when CSb line is high, the first read out byte might represent old status information (Figure 29).





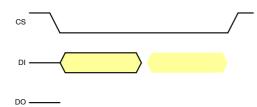


Table 8. SPI REGISTER OVERVIEW

SPI Register	Address	Access	Abbreviation
Status Register 4	0x09	R	SR4
Predriver Register 0	0x0A	R/W	PDRV0
Predriver Register 1	0x0B	R/W	PDRV1
Predriver Register 2	0x0C	R/W	PDRV2
Predriver Register 3	0x0D	R/W	PDRV3

Where: R/W = read and write access, R = read access only

Watchdog Register (WR)

The Watchdog Register is located at address 0x00 and can be used to enable the watchdog and set the watchdog time out. It can also be used to set the short circuit and open coil detection time

Control Register 0 (CR0)

Control Register 0 is located at address 0x01 and is used to set the maximum coil current and stepping mode.

Table 11. CONTRO	Table 11. CONTROL REGISTER 0								
	Control F								
Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0x01	Reset	0	0	0	0	0	1	1	1
	Data		S	M[3:0]		_		CUR[2:0]	

Table 12. CONTROL REGISTER 0 PARAMETERS

$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Parameter	Value	Value	Description	Info
0010 32 nd 0011 16 th		0000	128 th		
0011 16 th		0001	64 th		
		0010	32 nd		
0100 8th		0011	16 th		
		0100	8 th		
SM[3:0] Defines the 8 stepping modes for the PWM regulator.	SM[3:0]	0101	4 th	Defines the 8 stepping modes for the PWM regulator.	p23

Parameter	Value	Value	Description	Info
DIRCTRL	0	CW	Defines the direction of rotation. <u>Remark:</u> CW and CCW is relative. Direction of rotation will	202
DINCINE	1	CCW	be defined by the status of the DIR-pin and connection of the stepper motor!	p23
NXTP	0	Positive Edge	Defines the active edge on the NVT him	-00
NATP	1	Negative Edge	Defines the active edge on the NXT-pin.	p23
	0	Push Pull	Defines the extent time of WDb ain	-00
WDb_OD	1	Open Drain	Defines the output type of WDb-pin	p28
ERRb_OD -	0	Push Pull		-00
	1	Open Drain	 Defines the output type of ERRb-pin 	p28
	0	Disabled		-14
PWMJ	1	Enabled	Enables or disables PWM jitter	p14
	00	40 μs		
	01	120 μs		-01
MINSLATIME[1:0]	10	200 μs	Defines the time coil current zero-crossing extension time.	p21
	11	360 μs]	

Table 14. CONTROL REGISTER 1 PARAMETERS

Remark: Bit 5 of Control Register 1 should always be '0' (zero)!

Control Register 2 (CR2) Control

Parameter	Value	Value	Description	Info
	000	1		
	001	0.5		
	010	0.25		
	011	0.125	Defines the motor terminal voltage division factor for the	-04
SLAG[2:0]	100	0.0625	SLA-pin.	p24
	101	0.0625		
	110	0.0625		
	111	0.0625		
	0	No additional offset		
SLA_OFFS	1	Additional offset of 0.6 V	To enable an additional offset on the SLA-pin of 0.6V.	p24

Table 16. CONTROL REGISTER 2 PARAMETERS

Remark: Bit 5 of Control Register 2 should always be '0' (zero)!

Control Register 3 (CR3)

Control Register 3 is located at address 0x04 and is used to set the hold coil current functionality.

Table 17. CONTROL REGISTER 3

		Contro	ol Register	3 (CR3)						
Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1		
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0x04			-	-	-	•	-	-	-	•

Status Register 0 (SR0)

Status Register 0 is located at address 0x05 and can only be read. Status Register 0 is a non latched register meaning that the value of the register can change without the need of reading out the register. The register can be used to retrieve the temperature range or to verify a watchdog event.

Notice that bit 7 is the parity bit (see READ operation p30).

Table 19. STATUS REGISTER 0

	Status Register 0 (SR0)											
Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0			
	Access	R	R	R	R	R	R	R	R			
0x05	Reset	0	0	0	0	0	1	0	0			
	Data	PAR	TR[1:0]	WD	-	-	-	-			

Table 20. STATUS REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
	00	–40°C to 15°C	Motor driver thermal range.	
	01	15°C to 72°C	Remark: TR[1:0] = 11 and TSD = 0 => Thermal Warning	
TR[1:0]	10	73°C to 150°C	TR[1:0] = 11 and TSD = 1 => Thermal Shutdown TSD is located in Status Register 2	p27
	11	TSD = 0: 150°C to 170°C TSD = 1: >170°C		
WD	0	No watchdog event	If WDEN = 1 and watchdog not acknowledged before the Watchdog Time-out (WDT[3:0]), WDb-pin will be pulled low for 100ms to reset an external microcontroller and WD	p28
WD	1	Watchdog event occurred	bit will be set to '1' to indicate this event. The external mi- crocontroller can use this bit to verify a cold (WD = 0) or warm boot (WD = 1).	μΖο

Status Register 1 (SR1)

Status Register 1 is located at address 0x06 and can only be read. Status Register 1 is a latched register. If an error occurs the bit will be set and can only be cleared by reading out this bit¹. The register is used to report an overcurrent or open coil in the X coil, or to report a charge pump failure.

Notice that bit 7 is the parity bit (see READ operation p30).

Table 21. STATUS REGISTER 1

	Status Register 1 (SR1)									
Address	Address Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0									
	Access	R	R	R	R	R	R	R	R	
0x06	Reset	0	0	0	0	0	0	0	0	
	Data	PAR	OVCXPT	OVCXPB	OVCXNT	OVCXNB	CPFAIL	OPEN_X	-	

1. In Sleep mode the register can be read out but will not be cleared!

Parameter	Value	Value	Description	Info	
OVCXPT	0	No overcurrent		~ 07	
OVCAPT	1	Overcurrent	Overcurrent detection in top transistor XP-terminal	p27	
OVCYDR	0	No overcurrent	Our answerst detection in bottom transistor VD, terminal	~07	
OVCXPB	OVCXPB 1	Overcurrent	Overcurrent detection in bottom transistor XP-terminal	p27	
OVCXNT	0	No overcurrent		- 07	
OVCANT	1	Overcurrent	Overcurrent detection in top transistor XN-terminal	p27	
	0	No overcurrent		. 07	
OVCXNB	1	Overcurrent	Overcurrent detection in bottom transistor XN-terminal	p27	
	0	No charge pump failure		. 07	
CPFAIL	1	Charge pump failure	Charge pump failure detection	p27	
	0	No open coil detected	Open coil detection for X–coil	p27	
OPEN_X	1	Open coil detected	Note: a short circuit could trigger an open coil		

Table 22. STATUS REGISTER 1 PARAMETERS

Status Register 2 (SR2)

Status Register 3 (SR3)

Status Register 3 is located at address 0x08 and can only be read. Status Register 3 contains the highest 8 bits of the microstepping position and can be used to retrieve the position in the translator table (see Table 7). It is a non latched register meaning that the microstepping position can be updated by the motor driver at any moment. Status Register 3 does not contain a parity bit.

Table 25. STATUS REGISTER 3

	Status Register 3 (SR3)									
Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
0x08	Access	R	R	R	R	R	R	R	R	
	Reset	0	0	0	0	0	0	0	0	
	Data				MSP	[8:1]				

Table 26. STATUS REGISTER 3 PARAMETERS

Parameter	Value	Value	Description	Info
MSP[8:1]	XXXX XXXX	Microstepping position	Indicates the position within the translator table	p23

Status Register 4 (SR4)

Status Register 4 is located at address 0x09 and can only be read. Status Register 4 contains the lowest 8 bits of the microstepping position and can be used to retrieve the position in the translator table (see Table 7). It is a non-latched register meaning that the microstepping position can be updated by the motor driver at any moment. Status Register 4 does not contain a parity bit.

Table 27. STATUS REGISTER 4

	Status Register 4 (SR4)								
Address	Dess Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0								
0x09	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data				MSP	[7:0]			

Table 28. STATUS REGISTER 4 PARAMETERS

Parameter	Value	Value	Description	Info
MSP[7:0]	XXXX XXXX	Microstepping position	Indicates the position within the translator table	p23

Table 32. PREDRIVER REGISTER 1 PARAMETERS

Parameter	Value	Value	Description	Info		
	000	1.25 μs				
	001 1.75 μs 010 2.25 μs					
		2.25 μs				
	011	2.75 μs				
BOT_t2[2 :0]	100	3.25 μs	Defines the switch on duration t_2 for the external bottom MOSFET's.	p13		
	101	3.75 μs				
	110	4.25 μs]			
	111	4.75 μs	1			

 $\begin{array}{l} \mbox{Predriver Register 2 (PDRV2)} \\ \mbox{Predriver Register 2 is located at address 0x0C and can be used to set t_{off} (see Figure 11). \\ \end{array}$

Table 33. PREDRIVER REGISTER 2

Predriver Register 2 (PDRV2)									
Address	s Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0								
0x0C	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	1	0	0	0	1
	Data	-	TOP_toff[2:0]			-	BOT_toff[2:0]		

Table 34. PREDRIVER REGISTER 2 PARAMETERS

Parameter	Value	Value	Description	Info		
	000	1.25 μs				
	001	1.75 μs				
	010	2.25 μs				
	011	2.75 μs	Defines the switch off duration to far the subgraph ten MOSEET's	n10		
TOP_toff[2:0]	100	3.25 μs	Defines the switch off duration t _{off} for the external top MOSFET's.	p13		
	101	3.75 μs				
	110	4.25 μs				
	111	4.75 μs				
	000	1.25 μs				
	001	1.75 μs				
	010	2.25 μs				
	011	2.75 μs	Defines the switch off duration to far the outgrad better MOSEET's	n10		
BOT_toff[2 :0]	100	3.25 μs	Defines the switch off duration t _{off} for the external bottom MOSFET's.	p13		
	101	3.75 μs	1			
	110	4.25 μs				
	111	4.75 μs				

Predriver Register 3 (PDRV3)

Predriver Register 3 is located at address 0x0D and can be used to set t_1 (see Figure 11).

Table 35. PREDRIVER REGISTER 3

	Predriver Register 3 (PDRV3)									
Address		Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 0								
	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0x0D	Reset	0	0	0	1	0	0	0	1	
	Data	-		TOP_t1[2:0]		-	BOT_t1[2:0]			

Table 36. PREDRIVER REGISTER 3 PARAMETERS

Parameter	Value	Value	Description	Info		
	000	375 ns				
	001	500 ns				
	010	625 ns				
	011	750 ns	Defines the switch on duration to for the subscription MCCCCC			
TOP_t1[2:0]	100	825 ns	Defines the switch on duration t ₁ for the external top MOSFET's.	p13		
	101	1000 ns				
	110	1125 ns				
	111	1250 ns				
	000	375 ns				
	001	500 ns				
	010	625 ns				
DOT +1 [0 -0]	011	750 ns	Defines the suitch on duration to far the external better MOSEET's	n10		
BOT_t1[2 :0]	100	825 ns	Defines the switch on duration t_1 for the external bottom MOSFET's.	p13		
	101	1000 ns	-			
	110	1125 ns				
	111	1250 ns				

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