AMIS-30422

Mic o-S e ing S e e Mo o B idge Con olle

Introduction

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QFN48
CASE 485AJ

MARKING DIAGRAM

Key Features

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ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 44 of this data sheet.

BLOCK DIAGRAM

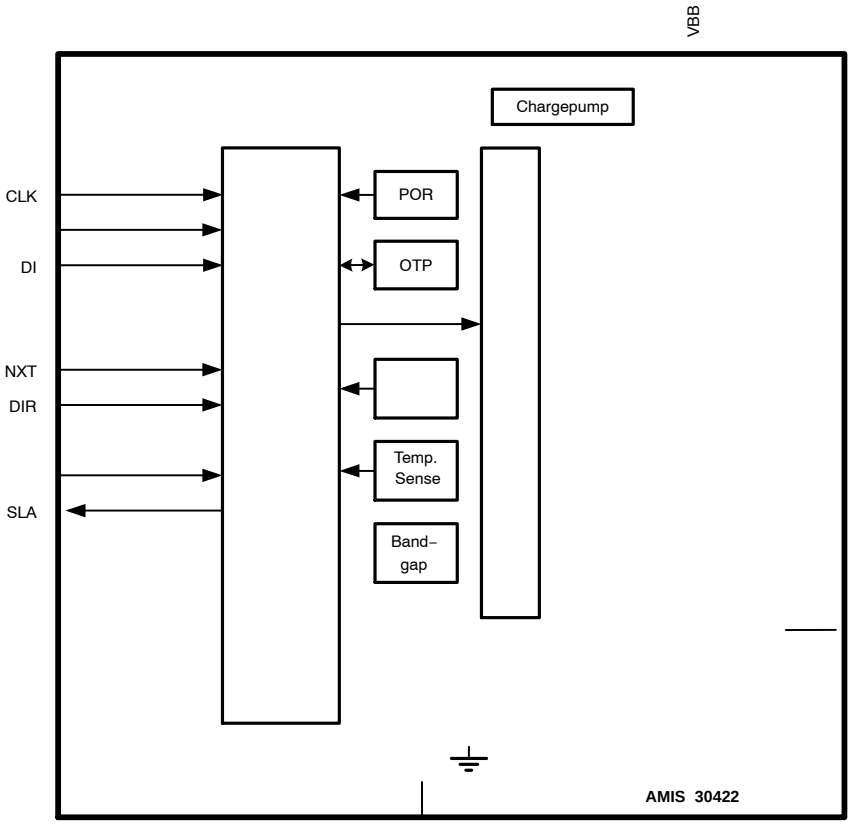
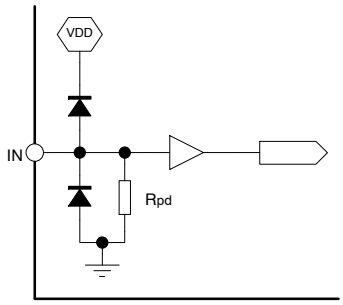
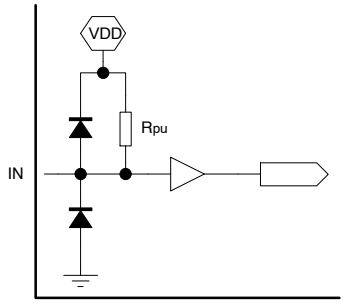
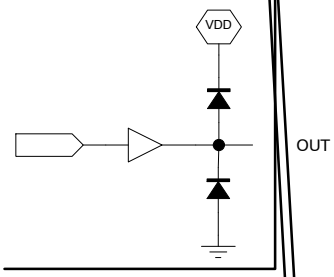


Figure 1. Block Diagram AMIS 30422

EQUIVALENT SCHEMATICS







ELECTRICAL SPECIFICATION

Table 2. ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

Symbol	Parameter	Min	Max	Unit
V_{BB}	Analog DC supply voltage (Note 3)	−0.3	+40	V
I_{load}	Logic supply external load current, Normal Mode	0	−10	mA
	Logic supply external load current, Sleep Mode	0	−1	mA
V_{RSENS}				

Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
SUPPLY & VOLTAGE REGULATOR							
V_{BB}	VBB	Nominal operating supply range		6		30	V
I_{BB}		Total internal current consumption	Unloaded outputs, internal consumption included, H−bridge disabled			20	mA
I_{SLEEP}		Sleep mode current consumption	Unloaded outputs, CSb = V_{DD}			150	μA
V_{DD}	VDD	Regulated Output Voltage	$-10\ mA \le I_{load} \le 0\ mA$	3.1	3.3	3.5	V
V_{DD_SLEEP}		Regulated Output Voltage in Sleep	$-1\ mA \le I_{load} \le 0\ mA$	2.1	2.95	3.63	V

Table 4. DC PARAMETERS

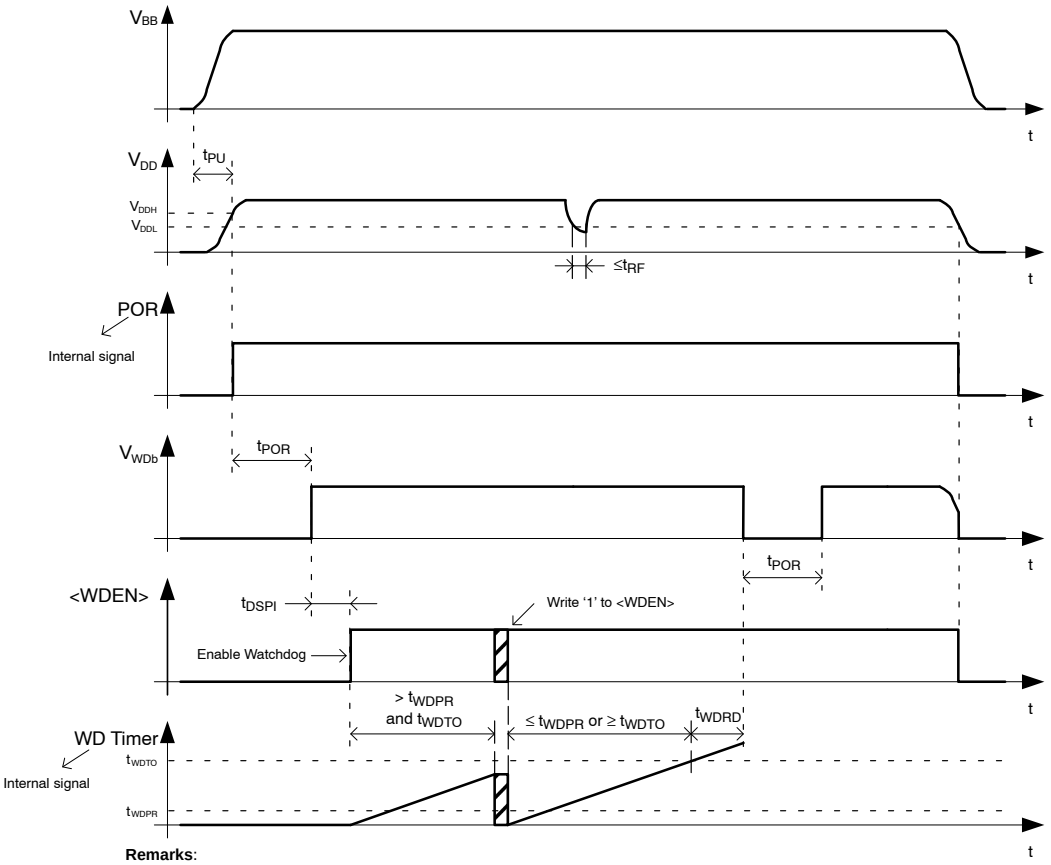
Table 4. DC PARAMETERS

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.
Convention: currents flowing in the circuit are defined as positive.

Symbol	Remark/Test Conditions	Min	Typ	Max	Unit

Table 5. AC PARAMETER The AC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
DIGITAL INPUTS							
t_{NXT_HI}		NXT Minimum, high pulse width	See Figure 6	625			ns
t_{NXT_LO}		NXT Minimum, low pulse width		625			ns
t_{DIR_SET}		NXT set up time, following change of DIR or <DIRCTRL>		1.28			µs
t_{DIR_HOLD}		NXT hold time, before change of DIR or <DIRCTRL>		1.28			µs
t_{SLP_SET}		<SLP> set up time		300			µs
t_{SLP_HOLD}		<SLP> hold time		1			µs
t_{MOTEN_SET}		<MOTEN> set up time		1			µs
t_{MOTEN_HOLD}		<MOTEN> hold time		1.28			µs
t_{MSP}		<MSP[7:0]> update delay				1.28	µs
CLEAR FUNCTION							
t_{CLR_SET}	CLR	Clear set up time	See Figure 7	40			µs
t_{CLR}		Clear duration time	See Figure 7	20		90	µs
DIGITAL OUTPUTS							
t_{H2L}							



Remarks:
−WDb−pin pulled up to V_{DD}
−t_{WDTO} = <WDT[3:0]>
−<WDEN> and <WDT[3:0]> are SPI bits

Figure 4. Power On Reset Timing Diagram

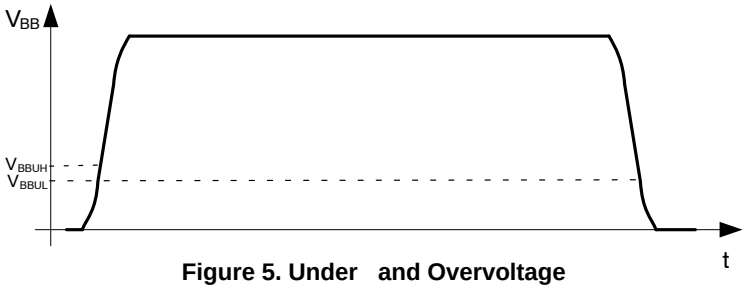
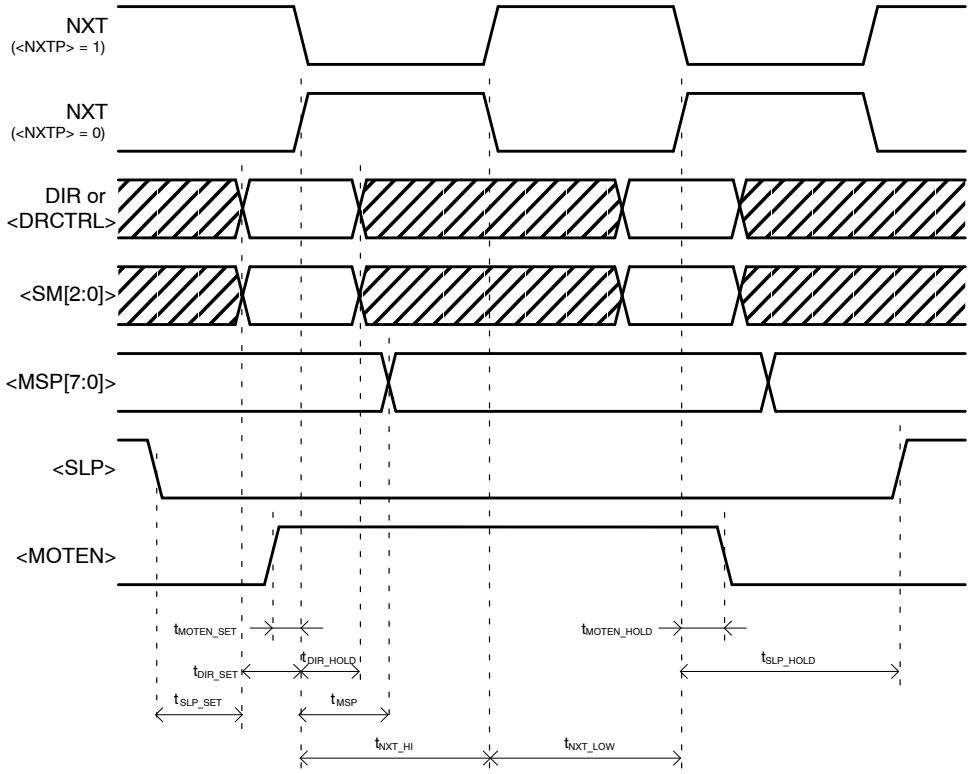
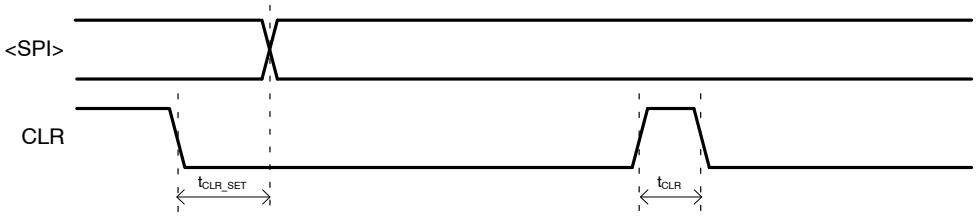


Figure 5. Under and Overvoltage



Remarks:
–<DIRCTRL>, <SM[2:0]>, <MSP[7:0]>, <SLP>, <MOTEN> and <NXTP> are SPI bits
–Timing for SPI bits starts after CS is high
–T_{SLP_SET} only relates to the digital inputs pins DIR and NXT

Figure 6. Digital Input Timing Diagram



Remarks:
<SPI> is any SPI data

Figure 7. CLR pin Timing Diagram

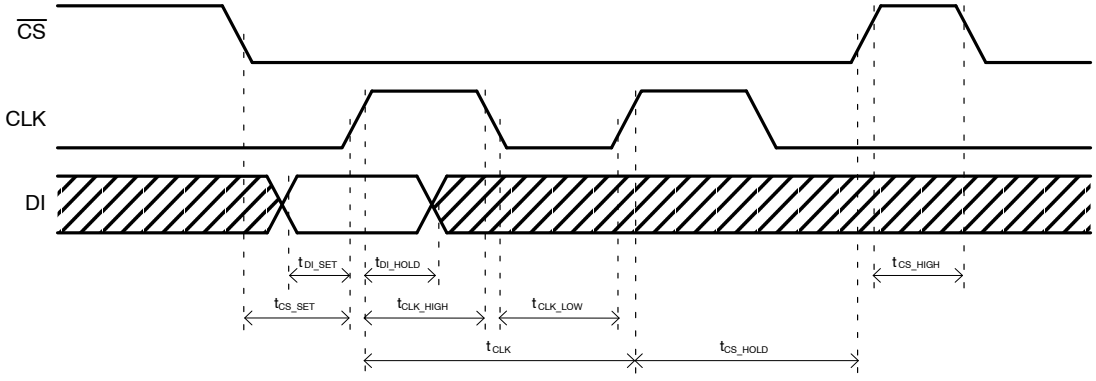


Figure 8. SPI Bus Timing Diagram

TYPICAL APPLICATION SCHEMATIC

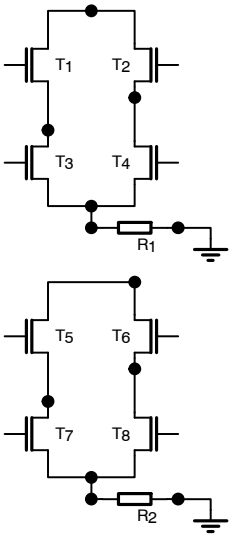


Figure 9. Typical Application Schematic AMIS 30422

FUNCTIONAL DESCRIPTION

H Bridge Pre Drivers

PWM Current Control

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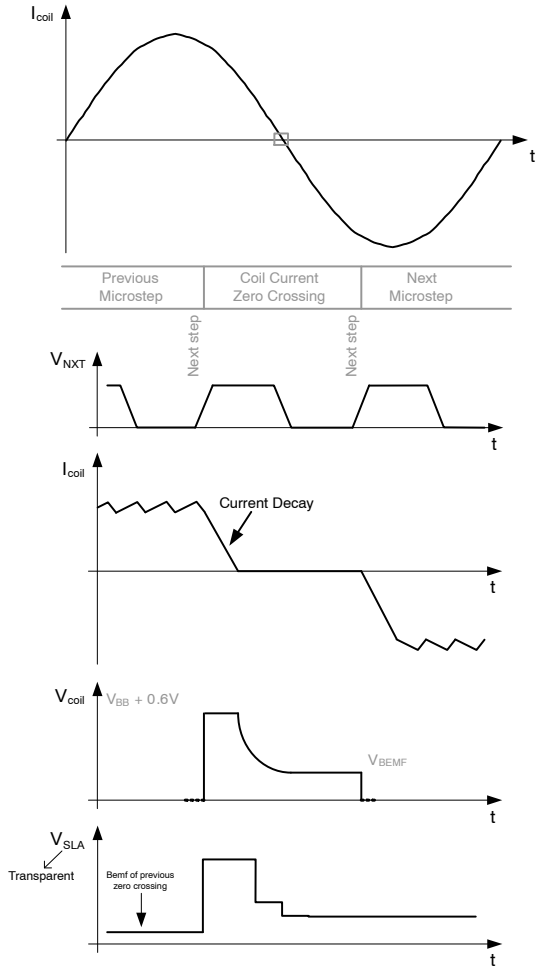
Programmable Peak Current

$$I_{max} = \text{<CUR[2:0]>} / R_{SENSE}$$

Hold Current Setting


I_{coil}
t
Previous Microstep
Coil Current Zero Crossing
Next Microstep
Next step
Next step
V_{NXT}
t
I_{coil}
Current Decay
t
V_{coil}
V_{BB} + 0.6V
V_{BEMF}
t
V_{SLA}
Transparent
Bemf of previous zero crossing
t

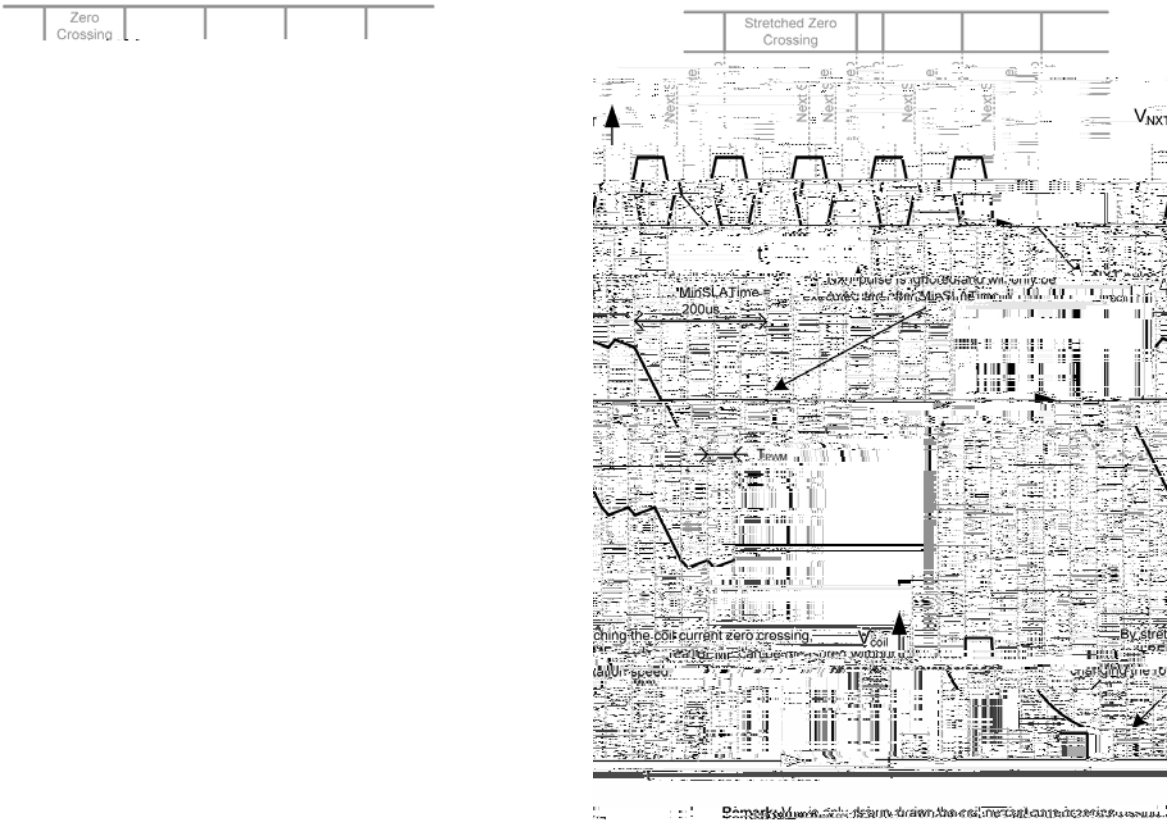


Figure 20. BEMF sampling without (left) and with (right) zero crossing stretching

Sleep Mode

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WARNING, ERROR DETECTION AND DIAGNOSTICS FEEDBACK

Thermal Warning and Shutdown

Open Coil/Current Not Reached Detection

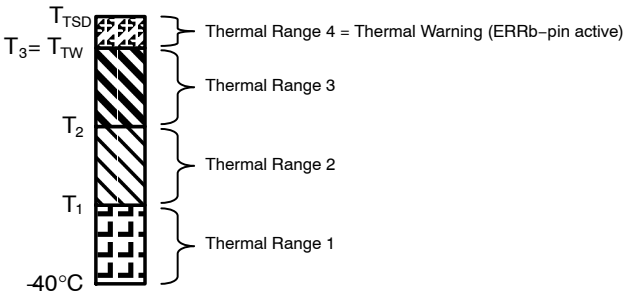

Figure 21. Thermal Ranges

Charge Pump Failure

Over Current Detection

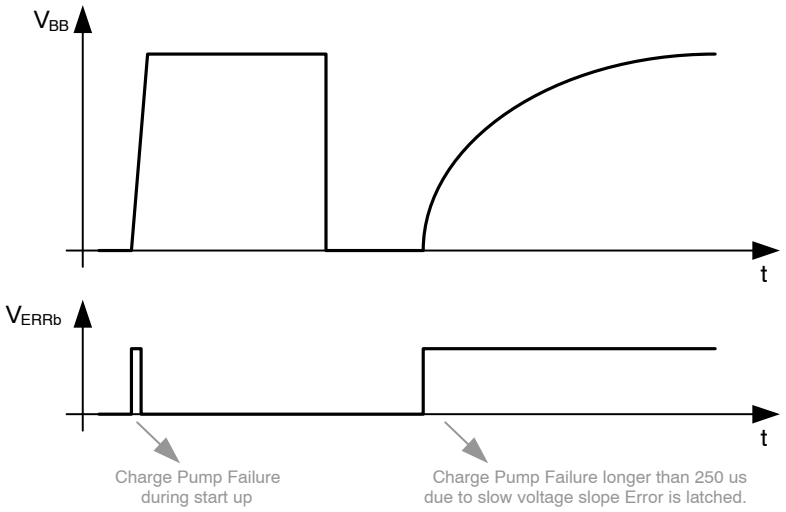

Figure 22. Charge Pump Failure

Watchdog

Error Output

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POWER SUPPLY AND THERMAL CALCULATION

Logic Supply Regulator

Undervoltage

SPI INTERFACE

SPI Transfer Format and Pin Signals

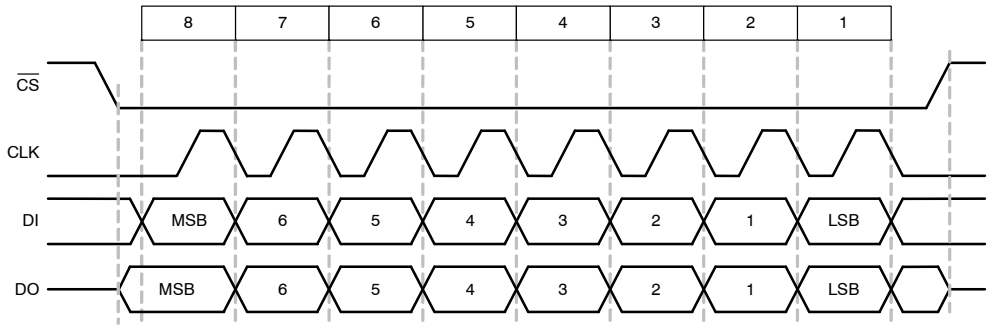

Figure 23. Timing Diagram of a SPI Transfer

Transfer Packet

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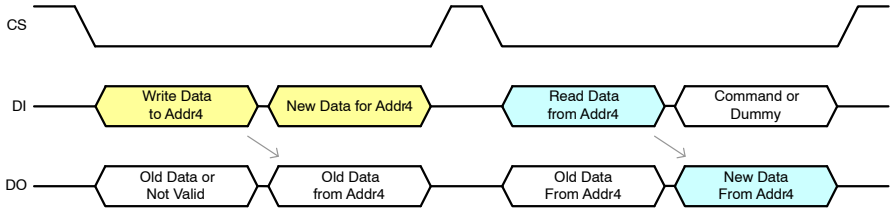
CS
DI
Write Data to Addr4
New Data for Addr4
Read Data from Addr4
Command or Dummy
DO
Old Data or Not Valid
Old Data from Addr4
Old Data From Addr4
New Data From Addr4

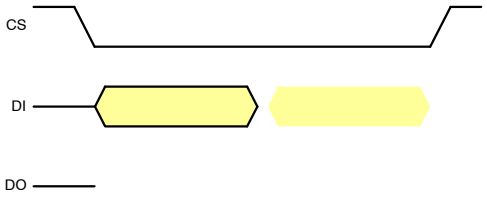
CS
DI
DO

Table 8. SPI REGISTER OVERVIEW

SPI Register	Address	Access	Abbreviation
Status Register 4	0x09	R	SR4
Predriver Register 0	0x0A	R/W	PDRV0
Predriver Register 1	0x0B	R/W	PDRV1
Predriver Register 2	0x0C	R/W	PDRV2
Predriver Register 3	0x0D	R/W	PDRV3

Watchdog Register (WR)

Control Register 0 (CR0)

Table 11. CONTROL REGISTER 0

Control Register 0 (CR0)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x01	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	1	1	1
	Data	SM[3:0]				–	CUR[2:0]		

Table 12. CONTROL REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
SM[3:0]	0000	128th	Defines the 8 stepping modes for the PWM regulator.	p23
	0001	64th		
	0010	32nd		
	0011	16th		
	0100	8th		
	0101	4th		

Table 14. CONTROL REGISTER 1 PARAMETERS

Parameter	Value	Value	Description	Info
DIRCTRL	0	CW	Defines the direction of rotation. Remark: CW and CCW is relative. Direction of rotation will be defined by the status of the DIR−pin and connection of the stepper motor!	p23
	1	CCW		
NXTP	0	Positive Edge	Defines the active edge on the NXT−pin.	p23
	1	Negative Edge		
WDb_OD	0	Push Pull	Defines the output type of WDb−pin	p28
	1	Open Drain		
ERRb_OD	0	Push Pull	Defines the output type of ERRb−pin	p28
	1	Open Drain		
PWMJ	0	Disabled	Enables or disables PWM jitter	p14
	1	Enabled		
MINSLATIME[1:0]	00	40 μs	Defines the time coil current zero−crossing extension time.	p21
	01	120 μs		
	10	200 μs		
	11	360 μs		

Control Register 2 (CR2)

Table 16. CONTROL REGISTER 2 PARAMETERS

Parameter	Value	Value	Description	Info
SLAG[2:0]	000	1	Defines the motor terminal voltage division factor for the SLA−pin.	p24
	001	0.5		
	010	0.25		
	011	0.125		
	100	0.0625		
	101	0.0625		
	110	0.0625		
	111	0.0625		
SLA_OFFS	0	No additional offset	To enable an additional offset on the SLA−pin of 0.6V.	p24
	1	Additional offset of 0.6 V		

Control Register 3 (CR3)

Table 17. CONTROL REGISTER 3

Control Register 3 (CR3)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	
0x04	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Status Register 0 (SR0)

Table 19. STATUS REGISTER 0

Status Register 0 (SR0)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x05	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	1	0	0
	Data	PAR	TR[1:0]		WD	–	–	–	–

Table 20. STATUS REGISTER 0 PARAMETERS

Parameter	Value	Value	Description	Info
TR[1:0]	00	−40°C to 15°C	Motor driver thermal range. Remark: TR[1:0] = 11 and TSD = 0 => Thermal Warning TR[1:0] = 11 and TSD = 1 => Thermal Shutdown TSD is located in Status Register 2	p27
	01	15°C to 72°C		
	10	73°C to 150°C		
	11	TSD = 0: 150°C to 170°C TSD = 1: >170°C		
WD	0	No watchdog event	If WDEN = 1 and watchdog not acknowledged before the Watchdog Time−out (WDT[3:0]), WDb−pin will be pulled low for 100ms to reset an external microcontroller and WD bit will be set to ‘1’ to indicate this event. The external microcontroller can use this bit to verify a cold (WD = 0) or warm boot (WD = 1).	p28
	1	Watchdog event occurred		

Status Register 1 (SR1)

Table 21. STATUS REGISTER 1

Status Register 1 (SR1)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x06	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	OVCXPT	OVCXPB	OVCXNT	OVCXNB	CPFAIL	OPEN_X	–

1. In Sleep mode the register can be read out but will not be cleared!

Table 22. STATUS REGISTER 1 PARAMETERS

Parameter	Value	Value	Description	Info
OVCXPT	0	No overcurrent	Overcurrent detection in top transistor XP−terminal	p27
	1	Overcurrent		
OVCXPB	0	No overcurrent	Overcurrent detection in bottom transistor XP−terminal	p27
	1	Overcurrent		
OVCXNT	0	No overcurrent	Overcurrent detection in top transistor XN−terminal	p27
	1	Overcurrent		
OVCXNB	0	No overcurrent	Overcurrent detection in bottom transistor XN−terminal	p27
	1	Overcurrent		
CPFAIL	0	No charge pump failure	Charge pump failure detection	p27
	1	Charge pump failure		
OPEN_X	0	No open coil detected	Open coil detection for X−coil Note: a short circuit could trigger an open coil	p27
	1	Open coil detected		

Status Register 2 (SR2)

Status Register 3 (SR3)

Table 25. STATUS REGISTER 3

Status Register 3 (SR3)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x08	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	MSP[8:1]							

Table 26. STATUS REGISTER 3 PARAMETERS

Parameter	Value	Value	Description	Info
MSP[8:1]	xxxx xxxx	Microstepping position	Indicates the position within the translator table	p23

Status Register 4 (SR4)

Table 27. STATUS REGISTER 4

Status Register 4 (SR4)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x09	**Access**	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	MSP[7:0]							

Table 28. STATUS REGISTER 4 PARAMETERS

Parameter	Value	Value	Description	Info
MSP[7:0]	xxxx xxxx	Microstepping position	Indicates the position within the translator table	p23

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Table 32. PREDRIVER REGISTER 1 PARAMETERS

Parameter	Value	Value	Description	Info
BOT_t2[2 :0]	000	1.25 μs	Defines the switch on duration t_2 for the external bottom MOSFET's.	p13
	001	1.75 μs		
	010	2.25 μs		
	011	2.75 μs		
	100	3.25 μs		
	101	3.75 μs		
	110	4.25 μs		
	111	4.75 μs		

Predriver Register 2 (PDRV2)

Table 33. PREDRIVER REGISTER 2

Predriver Register 2 (PDRV2)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x0C	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	1	0	0	0	1
	Data	-	TOP_toff[2:0]			-	BOT_toff[2:0]		

Table 34. PREDRIVER REGISTER 2 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_toff[2:0]	000	1.25 μs	Defines the switch off duration t_{off} for the external top MOSFET's.	p13
	001	1.75 μs		
	010	2.25 μs		
	011	2.75 μs		
	100	3.25 μs		
	101	3.75 μs		
	110	4.25 μs		
	111	4.75 μs		
BOT_toff[2 :0]	000	1.25 μs	Defines the switch off duration t_{off} for the external bottom MOSFET's.	p13
	001	1.75 μs		
	010	2.25 μs		
	011	2.75 μs		
	100	3.25 μs		
	101	3.75 μs		
	110	4.25 μs		
	111	4.75 μs		

Predriver Register 3 (PDRV3)

Table 35. PREDRIVER REGISTER 3

Predriver Register 3 (PDRV3)									
Address		**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
0x0D	**Access**	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	1	0	0	0	1
	Data	-	TOP_t1[2:0]			-	BOT_t1[2:0]		

Table 36. PREDRIVER REGISTER 3 PARAMETERS

Parameter	Value	Value	Description	Info
TOP_t1[2:0]	000	375 ns	Defines the switch on duration t_1 for the external top MOSFET's.	p13
	001	500 ns		
	010	625 ns		
	011	750 ns		
	100	825 ns		
	101	1000 ns		
	110	1125 ns		
	111	1250 ns		
BOT_t1[2 :0]	000	375 ns	Defines the switch on duration t_1 for the external bottom MOSFET's.	p13
	001	500 ns		
	010	625 ns		
	011	750 ns		
	100	825 ns		
	101	1000 ns		
	110	1125 ns		
	111	1250 ns		