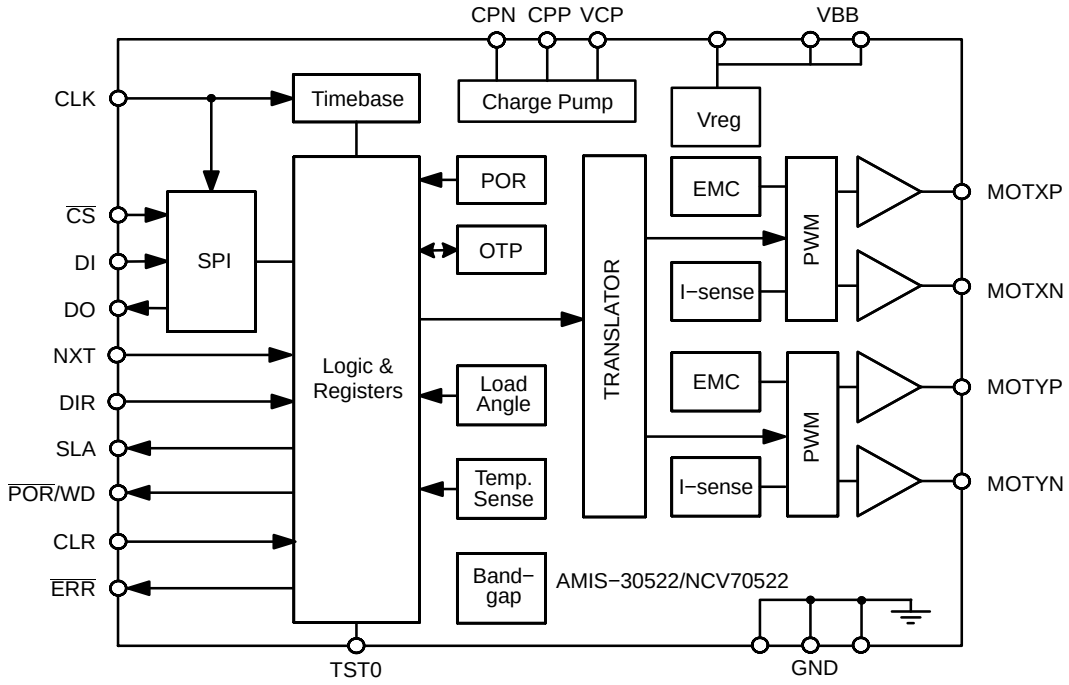
AMIS-30522, NCV70522

Micro-Stepping Motor Driver

The AMIS 30522/NCV70522 is a micro stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. The AMIS

Publication Order Number:


CPN
CPP
VCP
VBB
CLK
Timebase
Charge Pump
Vreg
POR
EMC
MOTXP
CS
SPI
OTP
PWM
DI
I−sense
MOTXN
DO
NXT
Logic &
Registers
TRANSLATOR
Load
Angle
EMC
MOTYP
DIR
SLA
PWM
POR/WD
Temp.
Sense
I−sense
MOTYN
CLR
Band−
gap
AMIS−30522/NCV70522
ERR
TST0
GND

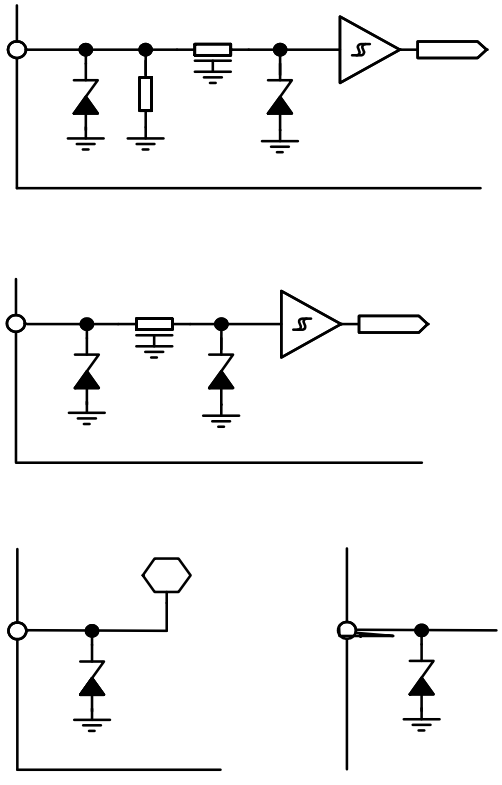
V_{BB}	Analog DC Supply Voltage (Note 1)	−0.3	+40	V
T_{ST}	Storage Temperature	−55	+160	°C
T_J	Junction Temperature (Note 2)	−50	+175	°C
V_{ESD}	Electrostatic Discharges on Component Level, All Pins (Note 3)	−2	+2	kV
V_{ESD}	Electrostatic Discharges on Component Level, HiV Pins (Note 4)	−8	+8	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. For limited time < 0.5 s
2. Circuit functionality not guaranteed.
3. Human Body Model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B)
4. HiV = High Voltage Pins MOTxx, V_{BB}, GND; Human Body Model (100 pF via 1.5 kΩ, according to JEDEC EIA−JESD22−A114−B)

NQFP−32	0.95	60	30	K/W

The following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



The 522 is available in a NQFP32 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground

(The AC Parameters are Given for V_{BB} and Temperature in Their Operating Ranges)

f_{osc}		Frequency of Internal Oscillator		3.6	4.0	4.4	MHz
f_{PWM}	MOTxx	PWM Frequency	Frequency Depends Only on Internal Oscillator	20.8	22.8	24.8	kHz
		Double PWM Frequency		41.6	45.6	49.6	kHz
f_d		PWM Jitter Depth (Note 13)			10		% f_{PWM}
tb_{rise}	MOTxx	Turn−On Voltage Slope, 10% to 90% (Note 13)	EMC[1:0] = 00		150		V/μs
			EMC[1:0] = 01		100		V/μs
			EMC[1:0] = 10		50		V/μs
			EMC[1:0] = 11		25		V/μs
tb_{fall}	MOTxx	Turn−off Voltage Slope, 90% to 10% (Note 13)	EMC[1:0] = 00		150		V/μs
			EMC[1:0] = 01		100		V/μs
			EMC[1:0] = 10		50		V/μs
			EMC[1:0] = 11		25		V/μs
t_{H2L}	$\overline{DO}$ $\overline{ERR}$	Output Falltime from V_{inH} to V_{inL}	Capacitive Load 400 pF and Pullup Resistor of 1.5 kΩ			50	ns
f_{CP}	CPN CPP	Charge Pump Frequency			250		kHz
t_{CPU}	MOTxx	Startup Time of Charge Pump (Note 14)	Spec External Components			5.0	ms
t_{CLR}	CLR	Minimum Time for Hard Reset		100			μs
t_{NXT_HI}	NXT	NXT Minimum, High Pulse Width	See Figure 4	2.0			μs
t_{NXT_LO}		NXT Minimum, Low Pulse Width	See Figure 4	2.0			μs
t_{DIR_SET}		NXT Hold Time, Following Change of DIR	See Figure 4		2.0		μs
t_{DIR_HOLD}		NXT Hold Time, Before Change of DIR	See Figure 4		2.0		μs
t_{PU}	PORB/ WD	Power−Up Time	V_{BB} = 12 V, I_{LOAD} = 50 mA, C_{LOAD} = 220 nF			110	μs
t_{PD}		Power−Down Time	external conditions				ms
t_{POR}		Reset Duration			100		ms
t_{RF}		Reset Filter Time			1.0		μs
t_{WDTO}		Watchdog Time Out Interval		32		512	ms
t_{WDPR}		Prohibited Watchdog Acknowledge Delay			2.0		ms

13. Characterization Data Only
14. Guaranteed by design.

A full H bridge is integrated for each of the two stator windings. Each H bridge consists of two low side and two high side N type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (High Impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H bridge switches, it is guaranteed that the top and bottom switches of the same half bridge are never conductive simultaneously (interlock delay).

A two stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

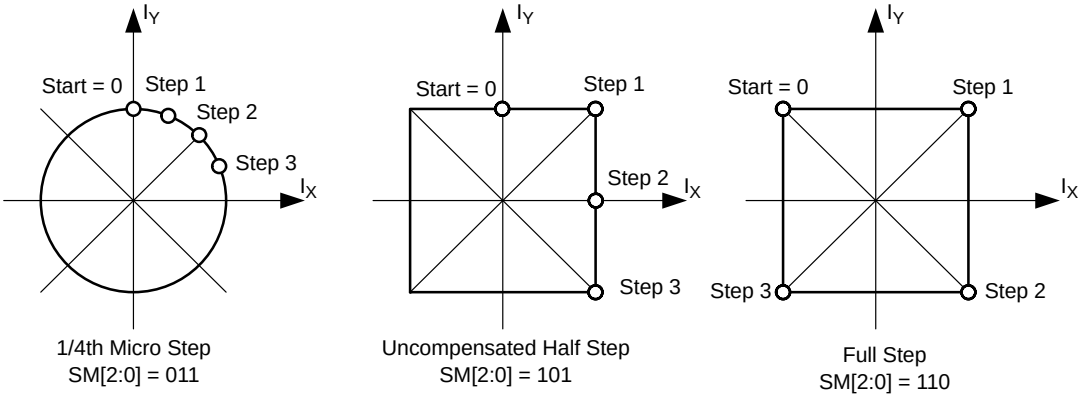
In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (See Table 12 SPI Control Parameter Overview EMC[1:0]).

The power transistors are equipped with so called “active diodes”: when a current is forced through the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain bulk diode of the transistor.

Depending on the desired current range and the micro step position at hand, the $R_{DS(on)}$ of the low side transistors

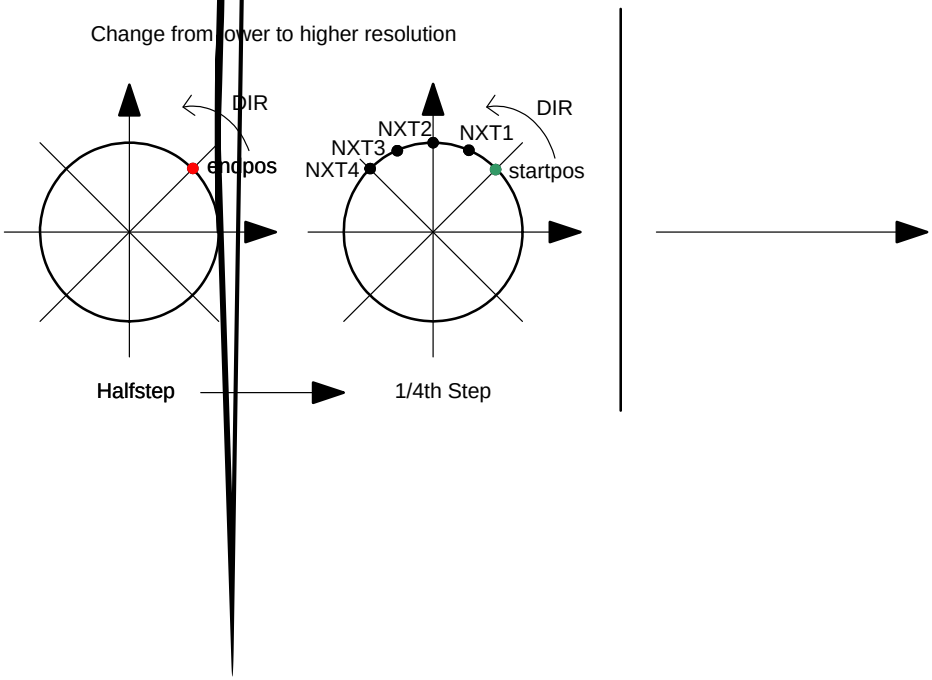
000 0000	'0'	0*	0*	0*	0*	0	100

011 1111	63	–	–	–	–	3.5	−98.8
100 0000	64	32	16	8	4	0	−100
100 0001	65	–	–	–	–	−3.5	−98.8
100 0010	66	33	–	–	–	−8.1	−97.7
100 0011	67	–	–	–	–	−12.7	−96.5
100 0100	68	34	17	–	–	−17.4	−95.3
100 0101	69	–	–	–	–	–	

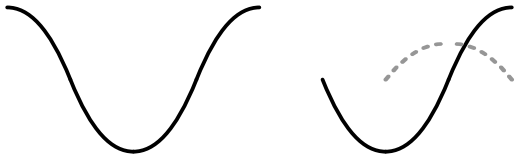


The direction of rotation is selected by means of following combination of the DIR input pin and the SPI controlled direction bit <DIRCTRL> as illustrated in Table 12.

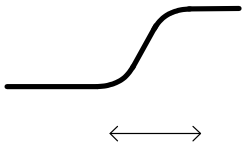
Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled). Depending on the NXT polarity bit <NXTP>

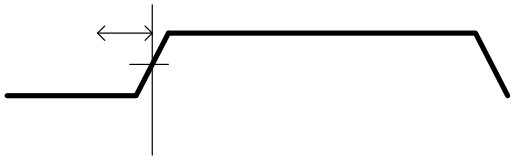

Change from lower to higher resolution
DIR
encpos
DIR
NXT2
NXT1
NXT3
NXT4
startpos
Halfstep
1/4th Step

exist per electrical period, yielding in total 4 zero current observation points per electrical period.



VBB

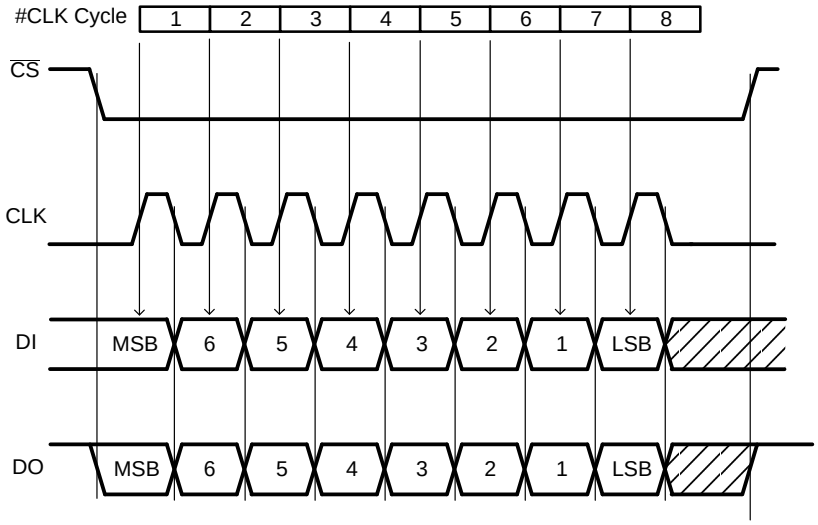




The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with the 522. The implemented SPI block is designed to interface directly with numerous micro controllers from several manufacturers. The 522 acts always as a Slave and cannot initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (522), and DI signal is the output from the Master. A chip select line ($\overline{CS}$) allows individual selection of a Slave SPI device in a multiple slave system. The $\overline{CS}$ line is active low. If the 522 is not selected, DO is pulled up with the external pullup resistor. Since 522 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.



NOTE: At the falling edge of the eighth clock pulse the data−out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the 522 system clock when $\overline{CS}$ = High.

CPFail	Charge Pump Failure	1	Status Register 0	‘0’ = no failure ‘1’ = failure: indicates that the charge pump does not reach the required voltage level.	‘0’
WD	Watchdog event	1	Status Register 0	This bit indicates the watchdog timer has not been cleared properly in time. If the master reads that WD is set to “1” after reset, it means that a watchdog re-set occurred (warm boot) instead of power−on−reset (cold boot). WD bit will be cleared only when the master writes “0” to WDEN bit.	‘0’
MSP[6:0]	Micro Step Position	7	Status Register 3	Translator micro step position	‘0000000’
OPENX	OPEN Coil X	1	Status Register 0	‘1’ = Open coil detected	‘0’
OPENY	OPEN Coil Y	1	Status Register 0	‘1’ = Open coil detected	‘0’
OVCXNB	Overcurrent at MOT Terminal; ottom Transistor	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at bottom transistor XN−terminal	‘0’
OVCXNT	Overcurrent at MOT Terminal; op Transistor	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at top transistor XN−terminal	‘0’
OVCXPB	Overcurrent at MOT Terminal; ottom Transistor	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at bottom transistor XP−terminal	‘0’
OVCXPT	Overcurrent at MOT Terminal; op Transistor	1	Status Register 1	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at top transistor XP−terminal	‘0’
OVCYNB	Overcurrent at MOT Terminal; ottom Transistor	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at bottom transistor YN−terminal	‘0’
OVCYNT	Overcurrent at MOT Terminal; op Transistor	1	Status Register 2	‘0’ = no failure ‘1’ = failure: indicates that overcurrent is detected at top transistor YN−terminal	‘0’
OVCYPB	Overcurrent at MOT Terminal; ottom Transistor	1	Status Register 2		

				†
AMIS30522C5222RG	−40°C to +125°C	NQFP−32 (Pb−Free)	1500 mA	Tape & Reel
AMIS30522C5222G	−40°C to +125°C	NQFP−32 (Pb−Free)	1500 mA	Tube / Tray
NCV70522MN003R2G*	−40°C to +125°C	NQFP−32 (Pb−Free)	1500 mA	Tape & Reel
NCV70522MN003G*	−40°C to +125°C	NQFP−32 (Pb−Free)	1500 mA	Tube / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Qualified for automotive applications.

QFN32, 7x7
CASE 560AA
ISSUE A

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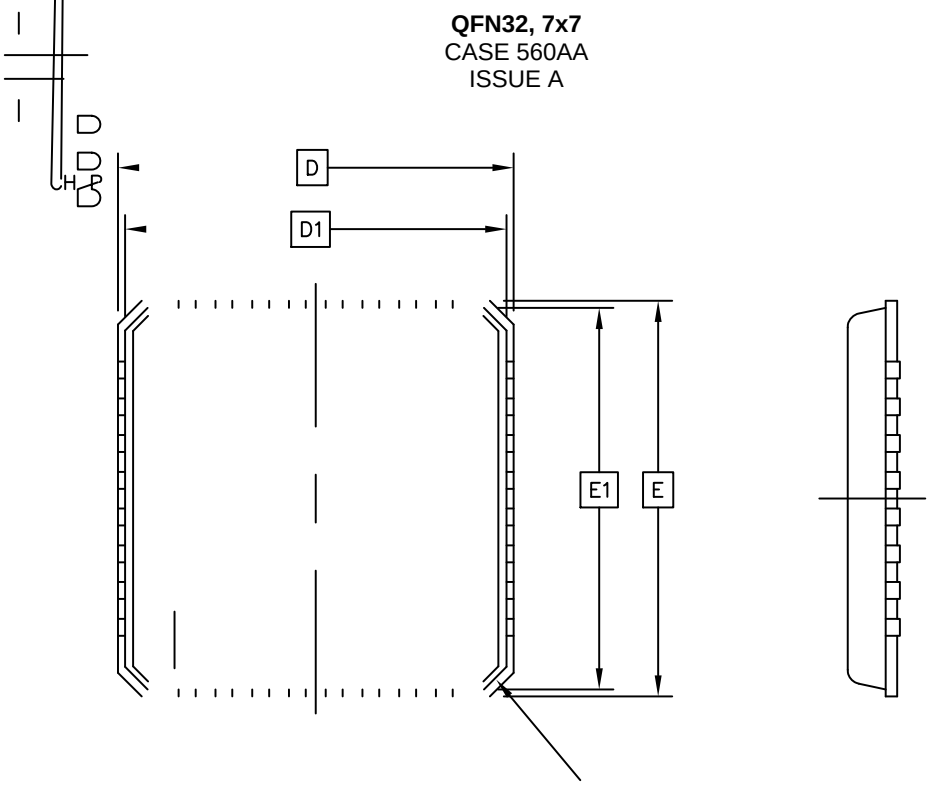

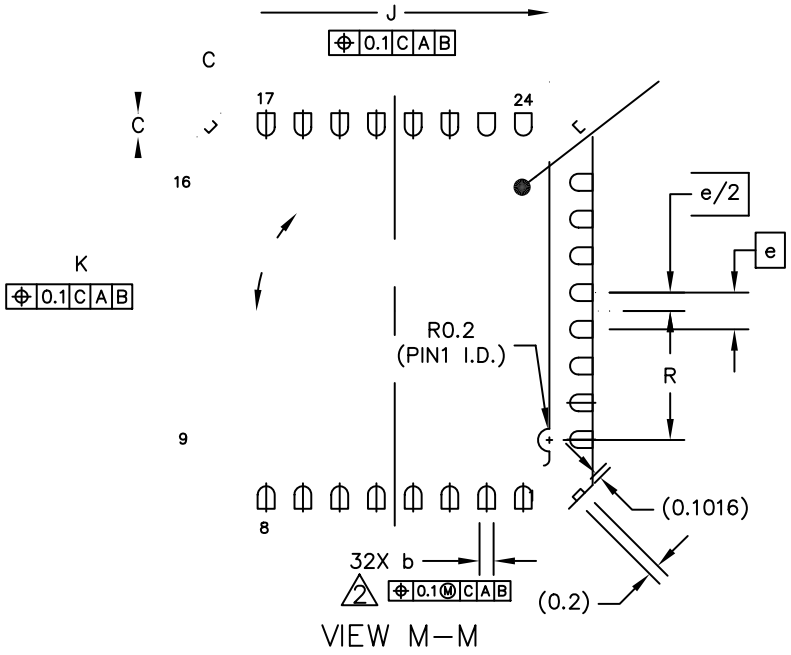

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DESCRIPTION:		