

Introduction

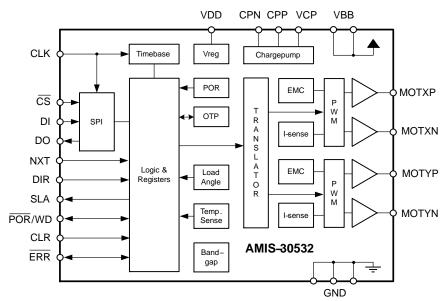
The AMIS-30532 is a micro-stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and an SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. The AMIS-30532 contains a current-translation table and takes the next micro-step depending on the clock signal on the "NXT" input pin and the status of the "DIR" (=direction) register or input pin. The chip provides a so-called "speed and load angle" output. This allows the creation of stall detection algorithms and control loops based on load-angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS-30532 is implemented in I2T100 technology, enabling both high-voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS-30532 is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on-

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Block DIAGRAM



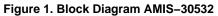
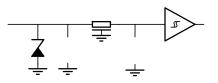


Table 1. PIN LIST AND DESCRIPTION

Name	Pin	Description	Туре	Equivalent Schematic
GND	1	Groun[re6891		

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



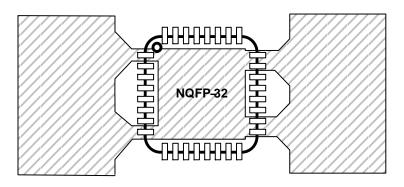


Figure 4. Example of NQFP-32 PCB Ground Plane Layout in Top View (Preferred Layout at Top and Bottom)

ELECTRICAL SPECIFICATION

Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating

ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 5. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Тур	Max	Unit
DIGITAL OUTPUTS							

V_{OL} DO, ERR

Table 6. AC PARAMETERS (The AC parameters are given for V_{BB} and temperature in their operating ranges)

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Тур	Max	Unit
INTERNAL OSCILLATOR							
f _{osc}		Frequency of internal oscillator		3.6	4.0	4.4	MHz
NOTODDD							

MOTORDRIVER

f_{PWM}

TYPICAL APPLICATION SCHEMATIC

Figure 7. Typical Application Schematic AMIS-30532

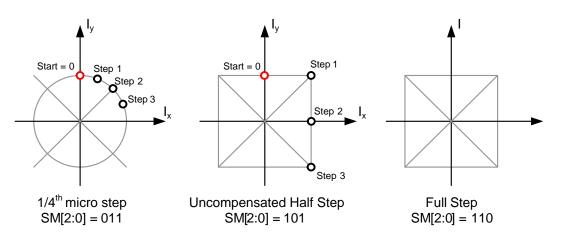
FUNCTIONAL DESCRIPTION

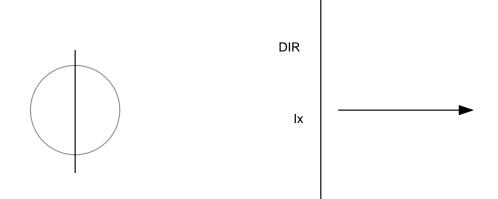
H–Bridge Drivers

A full H-bridge is integrated for each of the two stator windings. Each H-bridge consists of two low-side and two high-side N-type MOSFET switches. Writing logic '0' in bit <MOTEN> disables all drivers (high-impedance). Writing logic '1' in this bit enables both bridges and current can flow in the motor stator windings.

Table 11. CIRCULAR TRANSLATOR TABLE (CONTINUED)

MSP[6:0]





Speed and Load Angle Output

The SLA-pin provides an output voltage that indicates the level of the Back-e.m.f. voltage of the motor. This Back-e.m.f. voltage is sampled during every so-called "coil

current zero crossings". Per coil, two zero-current positions exist per electrical period, yielding in total four zero-current observation points per electrical period.

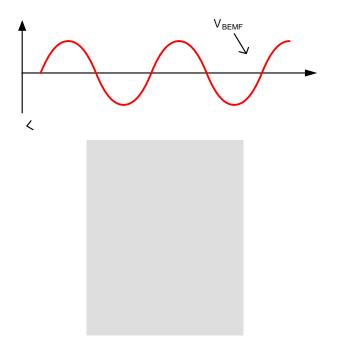
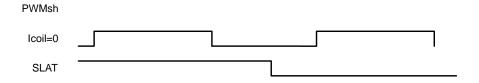


Figure 14. Principle of Bemf Measurement



voltages. If supply voltage is too low or external components are not properly connected to guarantee $R_{DS(on)}$ of the drivers, then the bit <CPFAIL> is set (Table 16). Also after POR the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to "1".

Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

Logic Supply Regulator

AMIS-30532 has an on-chip 5 V low-drop regulator with external capacitor to supply the digital part of the chip,

some low-voltage analog blocks and external circuitry. The voltage is derived from an internal bandgap reference. To calculate the available drive-current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 5 DC Parameters.

Power-On Reset (POR) Function

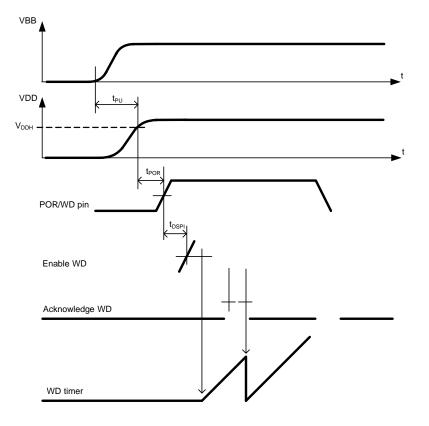
The open drain output pin POR

• Oscillator and digital clocks are silent, except during SPI communication

The voltage regulator remains active but with reduced current–output capability (I_{LOADSLP}). The watchdog timer stops running and it's value is kept in the counter. Upon

leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic '0' to bit <SLP>. A start-up time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.



SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS–30532. The implemented SPI block is designed to interface directly with numerous micro–controllers from several manufacturers. AMIS–30532 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS-30532), and DI signal is the output from the Master. A chip select line (\overline{CS})

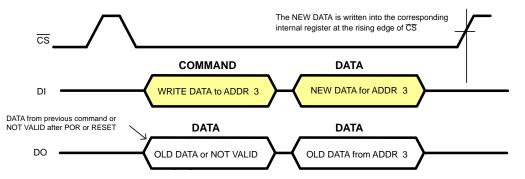


Figure 21. Single WRITE Operation where DATA from the Master is written in SPI register with Address 3

Examples of Combined READ and WRITE Operations

In the following examples successive READ and WRITE operations are combined. In Figure 22 the Master first reads the status from Register at ADDR4 and at ADDR5 followed

by writing a control byte in Control Register at ADDR2. Note that during the write command the old data of the pointed register is returned at the moment the new data is shifted in.

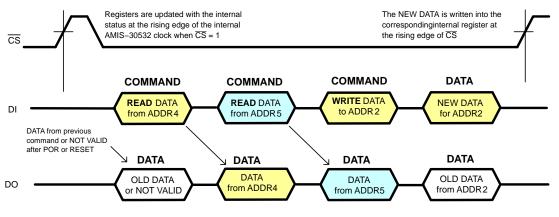


Figure 22. 2 Successive READ Commands Followed by a WRITE Command

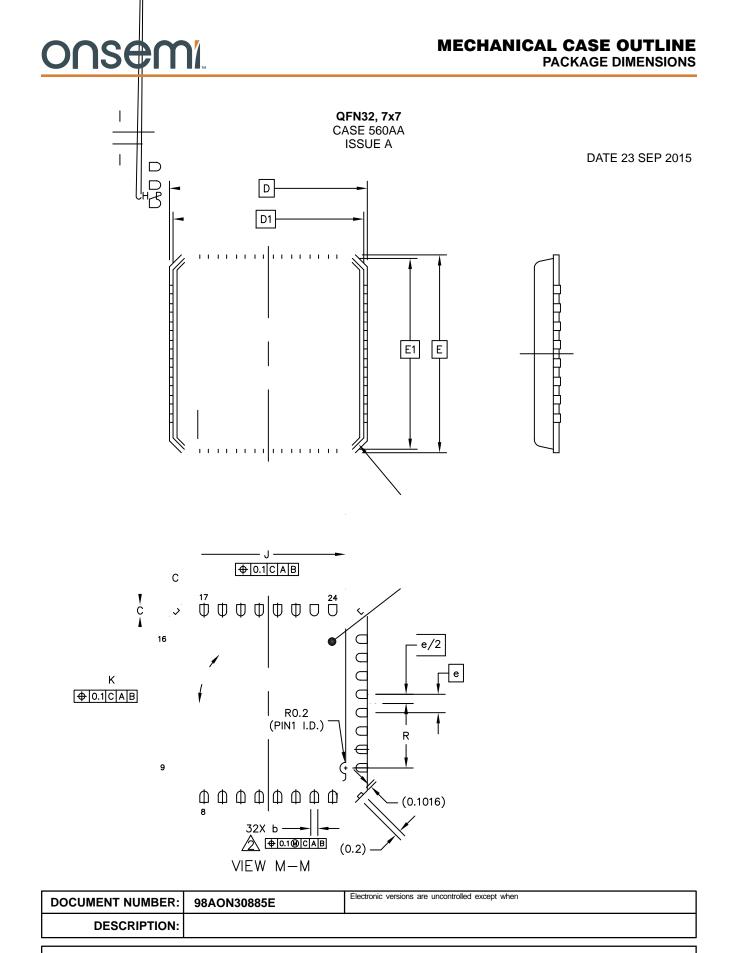
After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 23. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when \overline{CS} line is high, the first read out byte might represent old status information.

Table 14. SPI CONTROL PARAMETER OVERVIEW

CUR[4:0] Selects IMCmax

Mnemonic	Flag	Length (bit) Related SPI Register		Comment	Reset State
CPFail	Charge pump failure	1	<u>Status Register 0</u>	'0' = no failure '1' = failure: indicates that the charge pump does not reach the required voltage level. Note 1	ʻ0'
MSP[6:0]	Micro-step position	7	Status Register 3	Translator micro step position	'0000000'
OPENX	OPEN Coil X	1	Status Register 0	'1' = Open coil detected	

Table 17. SPI STATUS FLAGS OVERVIEW



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