Key Features

- Dual H−Bridge for 2−Phase Stepper Motors
- Programmable Peak−Current Up to 3 A
- On−Chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- Eleven Step Modes from Full Step Up to 128 Micro−Steps
- Fully Integrated Current−Sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly−Back Diodes
- Full Output Protection and Diagnosis
- Thermal Warning and Shutdown
- Compatible with 5 V and 3.3 V Microcontrollers
- Integrated 5 V Regulator to Supply External Microcontroller
- Integrated Reset Function to Reset External Microcontroller
- Integrated Watchdog Function
- These Devices are Pb−Free and are RoHS Compliant

See detailed ordering and shipping information in the package dimensions section on

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April, 2019 −

BLOCK DIAGRAM

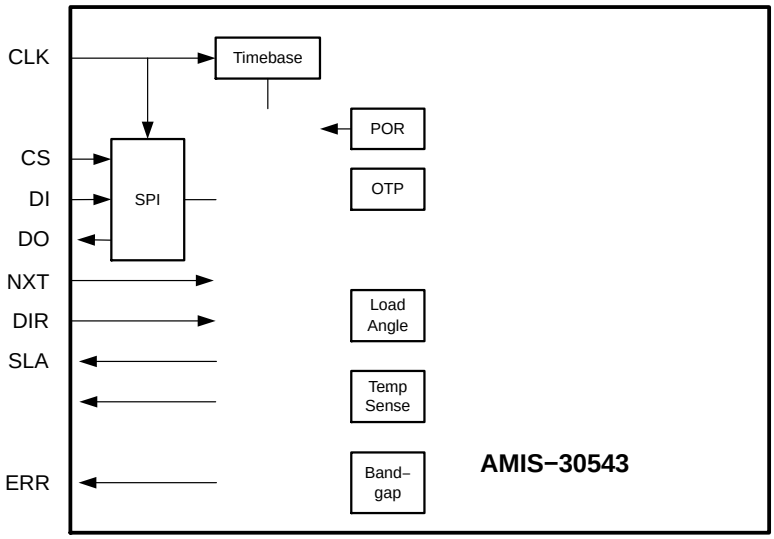
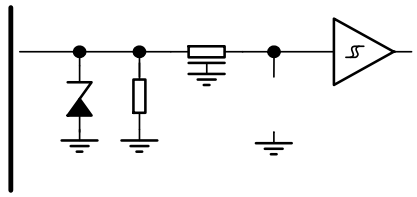


Table 1. PIN LIST AND DESCRIPTION

Name	Pin	Description	Type	Equivalent Schematic
GND	1	Ground	Supply	
DI	2	SPI Data In	Digital Input	Type 2
CLK	3	SPI Clock Input	Digital Input	Type 2
NXT	4	Next micro−step input	Digital Input	Type 2
DIR	5	Direction input	Digital Input	Type 2
$\overline{\text{ERR}}$	6	Error output (open drain)	Digital Output	Type 4
SLA	7	Speed load angle output	Analog Output	Type 5
/	8	No function (to be left open in normal operation)		
CPN	9	Negative connection of charge pump capacitor		

EQUIVALENT SCHEMATICS

Following figure gives the equivalent schematics of the user relevant inputs and outputs. The diagrams are simplified representations of the circuits used.



PACKAGE THERMAL CHARACTERISTICS

The AMIS−30543 is available in a NQFP32 package. For cooling optimizations, the NQFP has an exposed thermal pad which has to be soldered to the PCB ground plane. The ground plane needs thermal vias to conduct the heat to the bottom layer. Figure 4 gives an example for good power distribution solutions.

For precise thermal cooling calculations the major thermal resistances of the device are given in Table 5. The thermal media to which the power of the devices has to be given are:

- Static environmental air (via the case)
- PCB board copper area (via the exposed pad)

The major thermal resistances of the device are the Rth from the junction to the ambient (Rthja) and the overall Rth from the junction to exposed pad (Rthjp). In Table 4 below one can find the values for the Rthja and Rthjp, simulated according to JESD−51.

The Rthja for 2S2P is simulated conform JEDEC JESD−51 as follows:

- A 4−layer printed circuit board with inner power planes and outer (top and bottom) signal layers is used
- Board thickness is 1.46 mm (FR4 PCB material)
- The 2 signal layers: 70 μm thick copper with an area of 5500 mm^2 copper and 20% conductivity
- The 2 power internal planes: 36 μm thick copper with an area of 5500 mm^2 copper and 90% conductivity

The Rthja for 1S0P is simulated conform to JEDEC JESD−51 as follows:

- A 1−layer printed circuit board with only 1 layer
- Board thickness is 1.46 mm (FR4 PCB material)
- The layer has a thickness of 70 μm copper with an area of 5500 mm^2 copper and 20% conductivity

Unit
V
mA

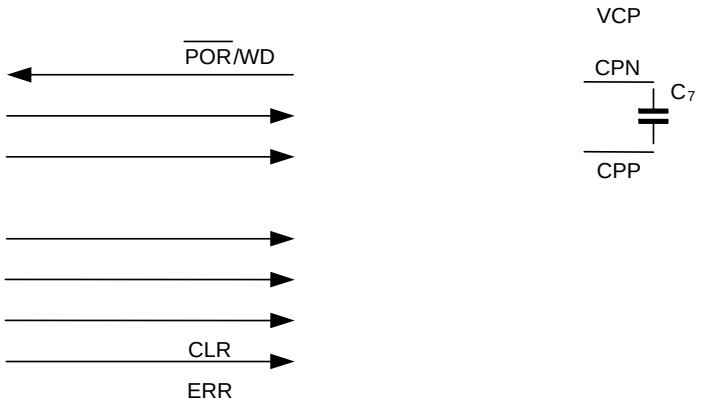
Table 4. DC PARAMETERS (The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified) Convention: currents flowing in the circuit are defined as positive.

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUTS							
V_{OL}	DO, $\overline{ERR}$, $\overline{POR}$/WD	Logic Low level open drain	I_{OL} = 5 mA			0.5	V
THERMAL WARNING AND SHUTDOWN							
T_{tw}		Thermal Warning		150	160	170	°C
T_{tsd}		Thermal shutdown (Notes 9 and 10)			T_{tw} + 20		°C
CHARGE PUMP							
V_{cp}	VCP	Output voltage	6 V< V_{BB} < 15 V		2 * V_{BB} – 2		V
			15 V < V_{BB} < 30 V	V_{BB} + 9	V_{BB} + 12.5	V_{BB}+16	V
C_{buffer}		External buffer capacitor		180	220	470	nF
C_{pump}	CPP CPN	External pump capacitor		180	220	470	nF
PACKAGE THERMAL RESISTANCE VALUE							
Rth_{ja}	NQFP	Thermal Resistance Junction−to−Ambient	Simulated Conform JEDEC JESD−51, 2S2P		30		K/W
			Simulated Conform JEDEC JESD−51, 1S0P		60		K/W
Rth_{jp}	NQFP	Thermal Resistance Junction−to−Exposed Pad			0.95		K/W
SPEED AND LOAD ANGLE OUTPUT							
V_{out}	SLA	Output Voltage Range		0.2		V_{DD} − 0.2	V
V_{off}		Output Offset SLA pin		−50		50	mV
G_{sla}		Gain of SLA Pin = V_{BEMF} / V_{COIL}	SLAG = 0		0.5		
			SLAG = 1		0.25		
R_{out}		Output Resistance SLA pin				1	kΩ

9. No more than 100 cumulated hours in life time above T_{tw}.
10. Thermal shutdown is derived from thermal warning. Characterization Data Only.

Table 5. AC PARAMETERS

TYPICAL APPLICATION SCHEMATIC



FUNCTIONAL DESCRIPTION

H−Bridge Drivers

A full H−bridge is integrated for each of the two stator windings. Each H−bridge consists of two low−side and two high−side N−type MOSFET switches. Writing logic ‘0’ in bit <MOTEN> disables all drivers (high−impedance). Writing logic ‘1’ in this bit enables both bridges and current can flow in the motor stator windings.

Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to > 50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over−all current−ripple is divided by two if PWM frequency is doubled (see Table 12 SPI Control Parameter Overview PWMF)

Table 9. CIRCULAR TRANSLATOR TABLE

MSP[8:0]

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

			SM[2:0]								
	xxx	xxx	000	001	010	011	100	xxx			
	ESM[2:0]										
	001	010	000	000	000	000	000	011		% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph		Coil X	Coil Y
000101011	43									50	86
000101100	44	22	11							51	86
000101101	45									52	85
000101110	46	23								53	84
000101111	47									55	84
000110000	48	24	12	6	3					56	83
000110001	49									57	82
000110010	50	25								58	82
000110011	51									59	81
000110100	52	26	13							60	80
000110101	53									61	80
000110110	54	27								62	79
000110111	55									62	78
000111000	56	28	14	7						63	77
000111001	57										

1205.512 441.184 .9070713.096 7 440.277 4BT6 0 0 6 186.5764 432.68(0m( )Tj.9356 0 0 6 45.8364 Tm27..754jET173.795 480.529 .90709 13.153 r

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
010101100	172	86	43							86	−51
010101101	173									85	−52
010101110	174	87								84	−53
010101111	175									84	−55
010110000	176	88	44	22	11					83	−56
010110001	177									82	−57
010110010	178	89								82	−58
010110011	179									81	−59
010110100	180	90	45							80	−60
010110101	181									80	−61
010110110	182	91								79	−62
010110111	183									78	−62
010111000	184	92	46	23						77	−63
010111001	185									77	−64
010111010	186	93								76	

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]									
	xxx	xxx	000	001	010	011	100	xxx	xxx	
	ESM[2:0]									
	001	010	000	000	000	000	000	011	100	% of I_{max}
MSP[8:0]										Coil X Coil Y

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
	ESM[2:0]										
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]	1/128	1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y
100000010	258	129								−2	−100
100000011	259									−4	−100
100000100	260	130	65							−5	−100
100000101	261									−6	−100
100000110	262	131								−7	−100
100000111	263									−9	−100
100001000	264	132	66	33						−10	−100
100001001	265									−11	−99
100001010	266	133								−12	−99
100001011	267										

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]										
	xxx	xxx	000	001	010	011	100	xxx	xxx		
		ESM[2:0]									
	001	010	000	000	000	000	000	011	100	% of I_{max}	
MSP[8:0]		1/64	1/32	1/16	1/8	1/4	Comp 1/2	Comp full 2ph	Comp full 1ph	Coil X	Coil Y

Table 9. CIRCULAR TRANSLATOR TABLE (continued)

	SM[2:0]									
	xxx	xxx	000	001	010	011	100	xxx	xxx	
	ESM[2:0]									
	001	010	000	000	000	000	000	011	100	% of I_{max}

MSP[8:0]

AMIS

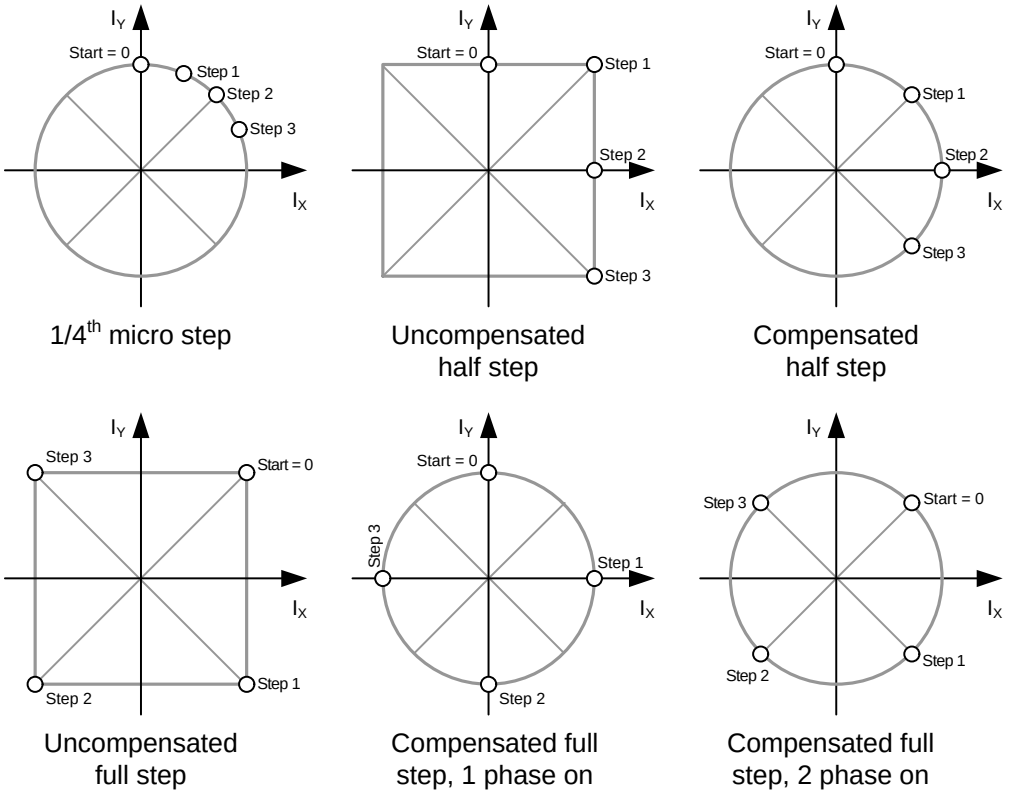


Figure 10. Translator Table: Circular and Square

Direction

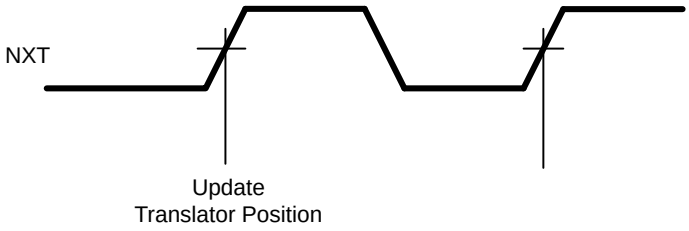
The direction of rotation is selected by means of following combination of the DIR input pin and the SPI−controlled direction bit <DIRCTRL>. (see Table 12 SPI Control Parameter Overview)

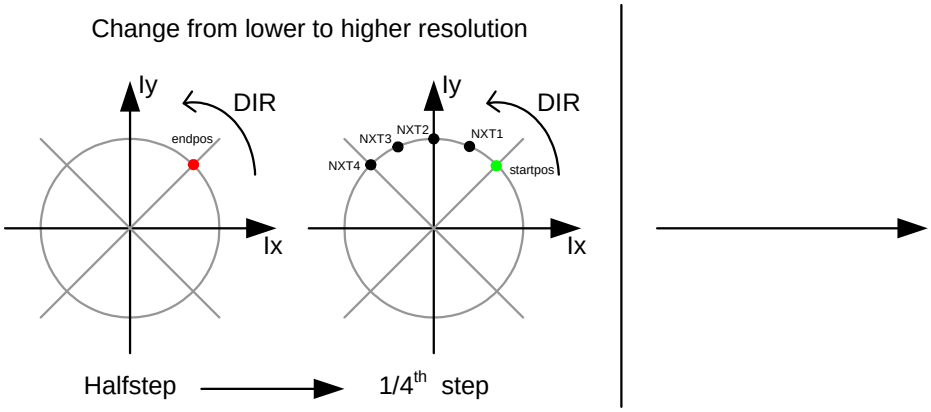
NXT Input

Changes on the NXT input will move the motor current one step up/down in the translator table (even when the motor is disabled: <MOTEN> = 0). Depending on the NXT−polarity bit <NXTP> (see Table 12 SPI Control Parameter Overview), the next step is initiated either on the rising edge or the falling edge of the NXT input.

Translator Position

The translator position MSP[8:0] can be read in SPI Status Register 3 and Status Register 4 (See Table 14 SR3 and SR4). This is a 9−bit number equivalent to the 1/128th micro−step (see Table 9 “Circular Translator Table”). The translator position is updated immediately following a NXT trigger.




Change from lower to higher resolution
Iy
DIR
endpos
Ix
Iy
DIR
NXT3
NXT2
NXT1
NXT4
startpos
Ix
Halfstep
1/4th step

Speed and Load Angle Output

The SLA−pin provides an output voltage that indicates the level of the Back−

Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

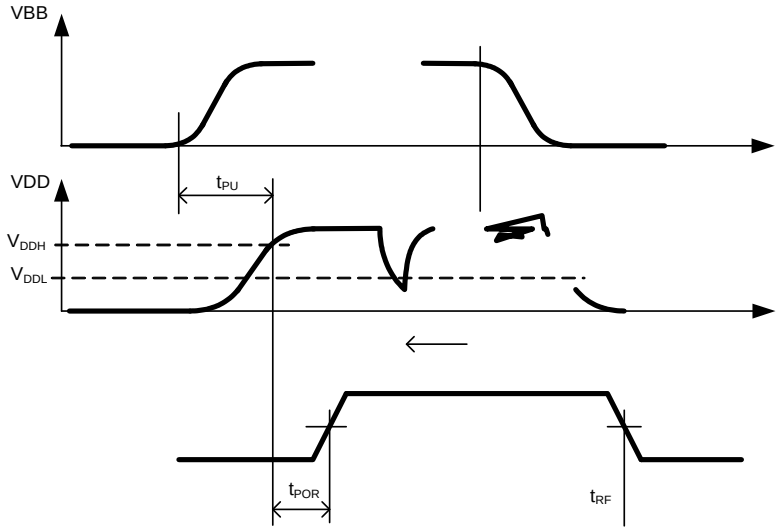
NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

Logic Supply Regulator

AMIS−30543 has an on−chip 5 V low−drop regulator with external capacitor to supply the digital part of the chip, some low−voltage analog blocks and external circuitry. The voltage level is derived from an internal bandgap reference. To calculate the available drive−current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See Table 4. DC parameters

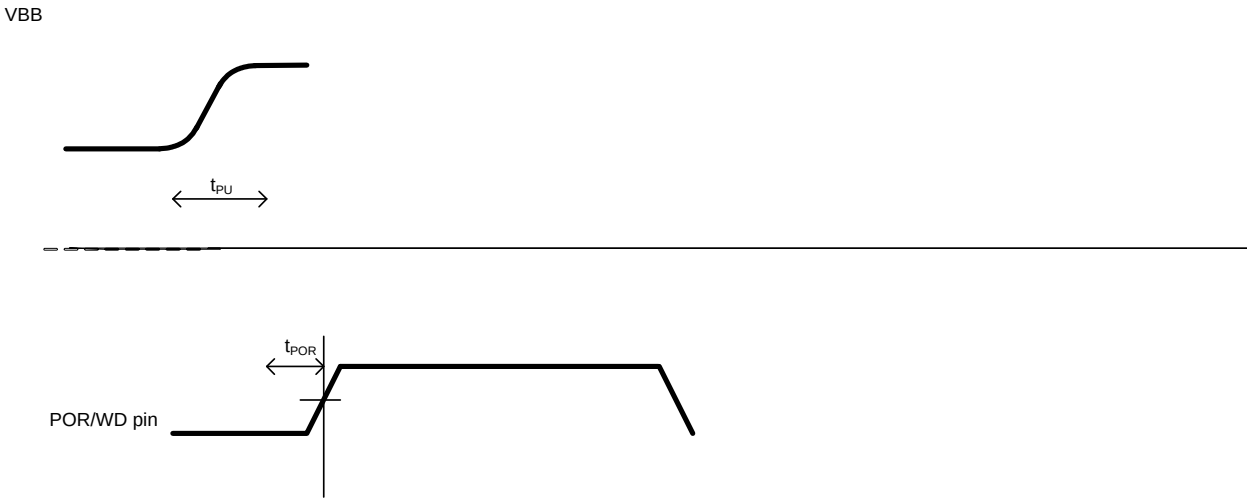
Power−On Reset (POR) Function

The open drain output pin $\overline{POR}$/WD provides an “active low” reset for external purposes. At powerup of AMIS−30543, this pin will be kept low for some time to reset for example an external microcontroller. A small analogue filter avoids resetting due to spikes or noise on the V_{DD} supply.



The voltage regulator remains active but with reduced current−output capability ($I_{LOADSLP}$). The watchdog timer stops running and it's value is kept in the counter. Upon leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic '0' to bit <SLP>. A startup time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.



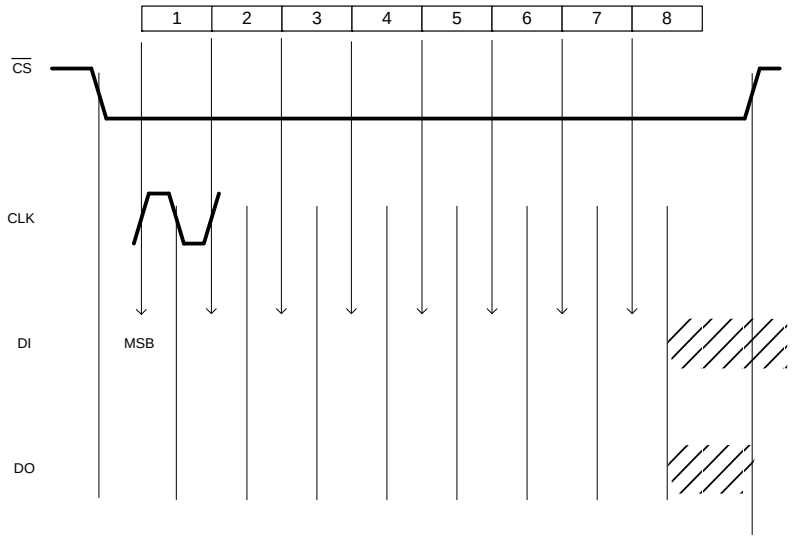
SPI INTERFACE

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS−30543. The implemented SPI block is designed to interface directly with numerous micro−controllers from several manufacturers. AMIS−30543 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

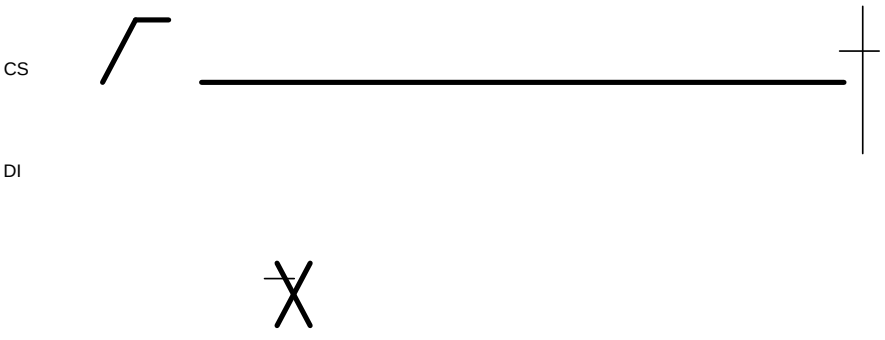
During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS−30543), and DI signal is the output from the Master. A chip select line ($\overline{CS}$) allows individual selection of a Slave SPI device in a multiple−slave system. The $\overline{CS}$ line is active low. If AMIS−30543 is not selected, DO is pulled up with the external pull up resistor. Since AMIS−30543 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.



Two command types can be distinguished in the communication between master and AMIS−30543:

- READ **from** SPI Register with address ADDR[4:0]:


CS
DI

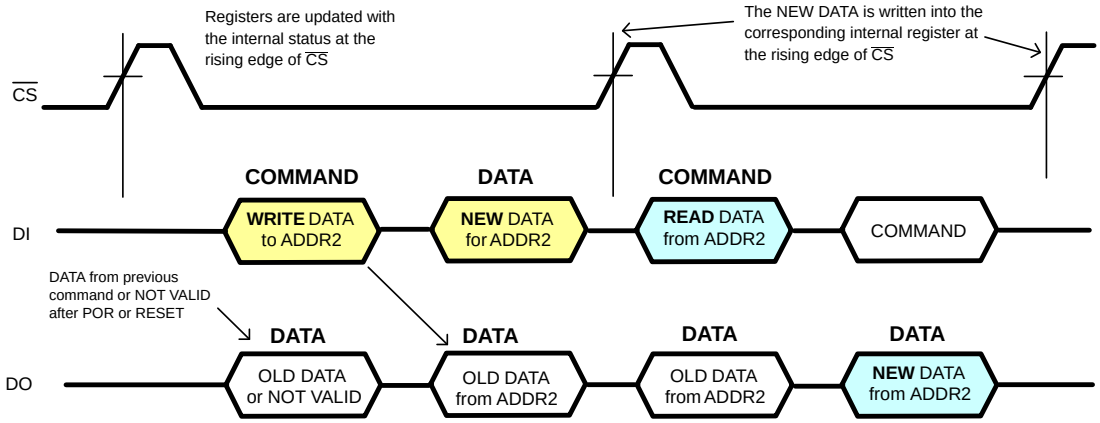


Figure 23. A WRITE Operation Where DATA from the Master is Written in SPI Register with Address 2 Followed by a READ Back Operation to Confirm a Correct WRITE Operation

NOTE: The internal data−out shift buffer of AMIS−30543 is updated with the content of the selected SPI register only at the last (every eight) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

Table 11. SPI CONTROL REGISTERS (All SPI control registers have Read/Write Access and default to “0” after power−on or hard reset)

		Structure							
	Content	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
	Access	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**	**R/W**
Address	**Reset**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
WR (00h)	Data	WDEN	WDT[3:0]				–	–	–
CR0 (01h)	Data	SM[2:0]			CUR[4:0]				
CR1 (02h)	Data	DIRCTRL	NXTP	–	–	PWMF	PWMJ	EMC[1:0]	
CR2 (03h)	Data	MOTEN	SLP	SLAG	SLAT	–	–	–	–
CR3 (09h)	Data	–	–	–	–	–	ESM[2:0]		

Where:
R/W Read and Write access
Reset: Status after power−On or hard reset

Table 12. SPI CONTROL PARAMETER OVERVIEW

Symbol	Description	Status		Value
DIRCTRL	Controls the direction of rotation (in combination with logic level on input DIR)	<DIR> = 0	<DIRCTRL> = 0	CW motion (Note 15)
			<DIRCTRL> = 1	CCW motion (Note 15)
		<DIR> = 1	<DIRCTRL> = 0	CCW motion (Note 15)
			<DIRCTRL> = 1	CW motion (Note 15)
NXTP	Selects if NXT triggers on rising or falling edge	<NXTP> = 0	Trigger on rising edge	
		<NXTP> = 1	Trigger on falling edge	
EMC[1:0]	Turn On – Turn−off Slopes of motor driver (Note 14)	00	Very Fast	
		01	Fast	
		10	Slow	
		11	Very Slow	
SLAT	Speed load angle transparency bit	<SLAT> = 0	SLA is not transparent	
		<SLAT> = 1	SLA is transparent	
SLAG	Speed load angle gain setting	<SLAG> = 0	Gain = 0.5	
		<SLAG> = 1	Gain = 0.25	
PWMF	Enables doubling of the PWM frequency (Note 14)	<PWMF> = 0	Default Frequency	
		<PWMF> = 1	Double Frequency	
PWMJ	Enables jittery PWM	<PWMJ> = 0	Jitter disabled	
		<PWMJ> = 1	Jitter enabled	
SM[2:0]	Stepmode (only valid if ESM[2:0] = 000)	000	1/32 Micro – Step	
		001	1/16 Micro – Step	
		010	1/8 Micro – Step	
		011	1/4 Micro – Step	
		100	Compensated Half Step	
		101	Uncompensated Half Step	
		110	Uncompensated full step	
		111	Uncompensated full step	
ESM[2:0]	Stepmode	001	1/128 Micro−Step	
		010	1/64 Micro−Step	
		011	Compensated full step, 2 phase on	
		100	Compensated full step, 1 phase on	
		Other	Stepping mode defined by SM[2:0]	
SLP	Enables sleep mode (if V_{BB} > 9 V)	<SLP> = 0	Active mode	
		<SLP> = 1	Sleep mode	
MOTEN	Activates the motor driver outputs	<MOTEN> = 0	Drivers disabled	
		<MOTEN> = 1	Drivers enabled	

14. The typical values can be found in Table 4: DC Parameters and in Table 5: AC parameters
15. Depending on the wiring of the motor connections

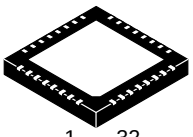
CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

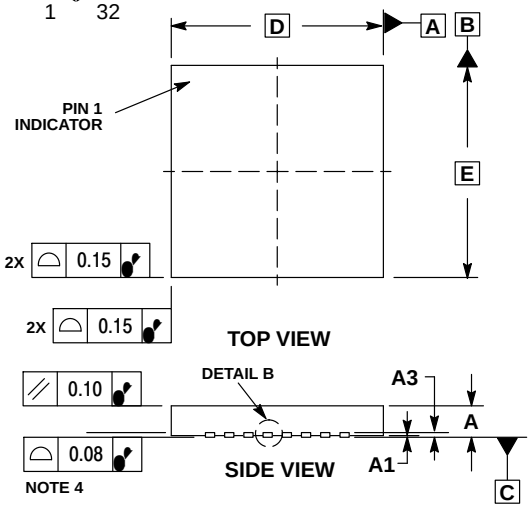
Table 13. SPI CONTROL PARAMETER OVERVIEW CUR[4:0]

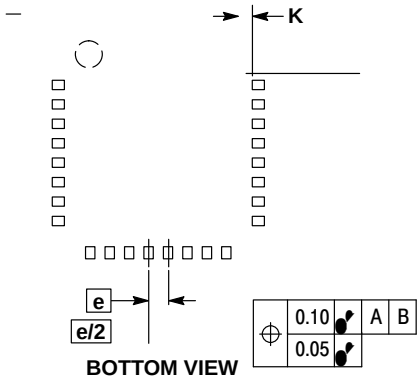
Current Range (Note 17)	Index CUR[4:0]		Current (mA) (Note 16)	Current Range (Note 17)	Index CUR[4:0]		Current (mA) (Note 16)
0	0	00000	132	3	16	10000	1405
	1	00001	245		17	10001	1520
	2	00010	355		18	10010	1695
1	3	00011	395		19	10011	1850
	4	00100	445		20	10100	2070
	5	00101	485		21	10101	2240
	6	00110	540		22	10110	2440
	7	00111	585		23	10111	2700
	8	01000	640		24	11000	2845
	9	01001	715		25	11001	3000
2	10	01010	780		26	11010	3000
	11	01011	870		27	11011	3000
	12	01100	955		28	11100	3000
	13	01101	1060		29	11101	3000
	14	01110	1150		30	11110	3000
	15						

Table 15. SPI STATUS FLAGS OVERVIEW

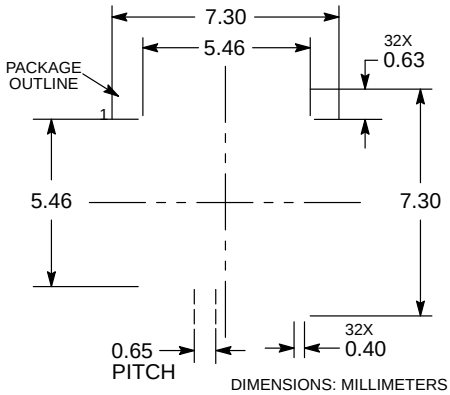
Mnemonic	Flag	Length (bit)	Related SPI Register	Comment	Reset State
CPFail	Charge pump failure	1	Status Register 0	‘0’ = no failure ‘1’ = failure: indicates that the charge pump does not reach the required voltage level. Note 1	‘0’
MSP[8:0]	Micro−step position	9	Status Register 3 and Status Register 4	Translator micro step position	‘000000000’
OPENX	OPEN Coil X	1	Status Register 0	‘1’ = Open coil detected	







RECOMMENDED MOUNTING FOOTPRINT

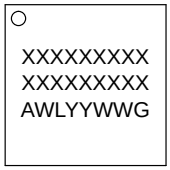


DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	7.00 BSC	
D2	5.16	5.36
E	7.00 BSC	
E2	5.16	5.36
e	0.65 BSC	
K	0.20	−−−
L	0.30	0.50

GENERIC MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**QFN32 7X7, 0.65MM PITCH**	**PAGE 1 OF 1**

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