AMIS-42665

High-Speed Low Power CAN Transceiver

http://onsemi.com

(Top View)

Description

The AMIS−42665 CAN transceiver is the interface between a controller area network (CAN) protocol controller and the physical bus and may be used in both 12 V and 24 V systems. The transceiver provides differential transmit capability to the bus and differential receive capability to the CAN controller.

Due to the wide common−mode voltage range of the receiver inputs, the AMIS−42665 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

The AMIS−42665 is a new addition to the CAN high−speed transceiver family and offers the following additional features:

Features

- Wake−up (WU) Over Bus
- Voltage Source via V_{SPLIT} Pin for Stabilizing the Recessive Bus Level (Further EMC Improvement)
- Ideal Passive Behavior when Supply Voltage is Removed
- Extremely Low Current Standby Mode
- Compatible with the ISO 11898 Standard (ISO 11898−2, ISO 11898−5 and SAE J2284)
- High Speed (up to 1 Mbps)
- Ideally Suited for 12 V and 24 V Industrial and Automotive Applications
- Extremely Low Current Standby Mode with Wake−up via the Bus
- Low EME Common−Mode Choke is No Longer Required
- Differential Receiver with Wide Common−Mode Range (± 35 V) for High EMS
- Transmit Data (TxD) Dominant Time−out Function
- Thermal Protection
- Bus Pins Protected against Transients in an Automotive Environment
- Power Down Mode in which the Transmitter is Disabled
- Bus and V_{SPLIT} Pins Short Circuit Proof to Supply Voltage and Ground
- Logic Level Inputs Compatible with 3.3 V Devices
- These are Pb−Free Devices

[redacted]

TYPICAL APPLICATION

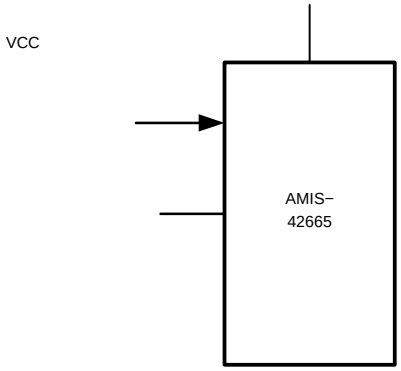


Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{CC}	Supply Voltage		−0.3	+7	V
V_{CANH}	DC Voltage at Pin CANH	$0 < V_{CC} < 5.25$ V; No Time Limit	−50	+50	V
V_{CANL}	DC Voltage at Pin CANL	$0 < V_{CC} < 5.25$ V; No Time Limit	−50	+50	V
V_{SPLIT}	DC Voltage at Pin V_{SPLIT}	$0 < V_{CC} < 5.25$ V; No Time Limit	−50	+50	V
V_{TxD}	DC Voltage at Pin TxD		−0.3	V_{CC} + 0.3	V
V_{RxD}	DC Voltage at Pin RxD		−0.3	V_{CC} + 0.3	V
V_{STB}	DC Voltage at Pin STB		−0.3	V_{CC} + 0.3	V
$V_{tran(CANH)}$	Transient Voltage at Pin CANH	Note 1	−300	+300	V
$V_{tran(CANL)}$	Transient voltage at Pin CANL	Note 1	−300	+300	V
$V_{tran(VSPLIT)}$	Transient Voltage at Pin V_{SPLIT}	Note 1	−300	+300	V
$V_{esd(CANL/CANH/VSPLIT)}$	Electrostatic Discharge Voltage at CANH and CANL Pin	Note 2 Note 4	−8 −500	+8 +500	kV

detected by the low−power differential receiver, the signal is first filtered and then verified as a valid wake signal after a time period of t_{dbus}, the RxD pin is driven low by the transceiver to inform the controller of the wake−up request.

Split Circuit

The V_{SPLIT} Pin is operational only in normal mode. In standby mode this pin is floating. The V_{SPLIT} is connected as shown in Figure 2 and its purpose is to provide a stabilized DC voltage of 0.5 x V_{CC} to the bus avoiding possible steps in the common−mode signal therefore reducing EME. These unwanted steps could be caused by an unpowered node on the network with excessive leakage current from the bus that shifts the recessive voltage from its nominal 0.5 x V_{CC} voltage.

Wake−up

When a valid wake−up (dominant state longer than t_{dbus}) is received during the standby mode the RxD pin is driven low. Wake−up behavior in case of a permanent dominant – due to, for example, a bus short – represents the only difference between the circuit sub−versions listed in the Ordering Information table. It is depicted in Figures 3 and 4. When the standby mode is entered while a dominant is present on the bus, the “unconditioned bus wake−up” versions will signal a bus−wakeup immediately after the state transition (seen as a High−level glitch on RxD). The other version (differing purely by a metal−level modification in the digital part) will signal bus−wakeup only after the initial dominant is released. In this way it’s ensured, that a CAN bus can be put to a low−power mode even if the nodes have a level sensitivity to RxD pin and a permanent dominant is present on the bus.

Overtemperature Detection

A thermal protection circuit protects the IC from damage by switching off the transmitter if the junction temperature exceeds a value of approximately 160°C. Because the transmitter dissipates most of the power, the power dissipation and temperature of the IC are reduced. All other IC functions continue to operate. The transmitter off−state resets when Pin TxD goes high. The thermal protection circuit is particularly needed when a bus line short circuits.

TxD Dominant Time−out Function

A TxD dominant time−out timer circuit prevents the bus lines being driven to a permanent dominant state (blocking all network communication) if Pin TxD is forced permanently low by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TxD. If the duration of the low−level on Pin TxD exceeds the internal timer value $t_{dom(TxD)}$, the transmitter is disabled, driving the bus into a recessive state. The timer is reset by a positive edge on Pin TxD. See Figure 10.

This TxD dominant time−out time ($t_{dom(TxD)}$

ELECTRICAL CHARACTERISTICS

Definitions

All voltages are referenced to GND (Pin 2). Positive currents flow into the IC.

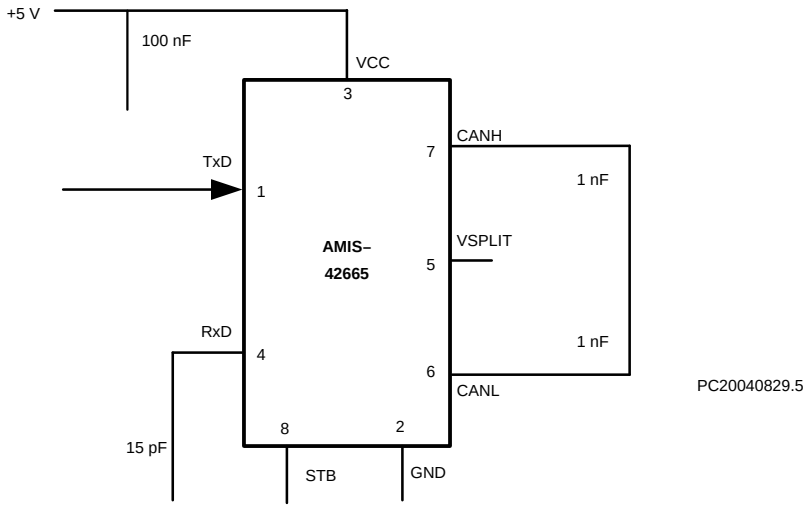
CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLY (PIN V_{CC})						
I_{CC}	Supply Current	Dominant; V_{TxD} = 0 V Recessive; V_{TxD} = V_{CC}		45 4	65 8	mA
I_{CCS}	Supply Current in Standby Mode	$T_{J,max}$ = 100°C		10	15	μA
TRANSMITTER DATA INPUT (PIN TxD)						
V_{IH}	High−Level Input Voltage	Output Recessive	2.0	−	V_{CC} + 0.3	V
V_{IL}	Low−Level Input Voltage	Output Dominant	−0.3	−	+0.8	V
I_{IH}	High−Level Input Current	V_{TxD} = V_{CC}	−5	0	+5	μA
I_{IL}	Low−Level Input Current	V_{TxD} = 0 V	−75	−200	−350	μA
C_i	Input Capacitance	Not Tested	−	5	10	pF
TRANSMITTER MODE SELECT (PIN STB)						
V_{IH}	High−Level Input Voltage	Standby Mode	2.0	−	V_{CC} + 0.3	V
V_{IL}	Low−Level Input Voltage	Normal Mode	−0.3	−	+0.8	V
I_{IH}	High−Level Input Current	V_{STB} = V_{CC}	−5	0	+5	μA
I_{IL}	Low−Level Input Current	V_{STB} = 0 V	−1	−4	−10	μA
C_i	Input Capacitance	Not Tested	−	5	10	pF
RECEIVER DATA OUTPUT (PIN RxD)						
I_{oh}	High−Level Output Current	V_o = 0.7 x V_{CC}	−5	−10	−15	mA
I_{ol}	Low−Level Output Current	V_o = 0.3 x V_{CC}	5	10	15	mA
BUS LINES (PINS CANH AND CANL)						
$V_{o(reces)\ (norm)}$	Recessive Bus Voltage Normal Mode	V_{TxD} = V_{CC}; No Load	2.0	2.5	3.0	V
$V_{o(reces)\ (stby)}$	Recessive Bus Voltage	V_{TxD} = V_{CC}; No Load Standby Mode	−100	0	100	mV
$I_{o(reces)\ (CANH)}$	Recessive Output Current at Pin CANH	−35 V < V_{CANH} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$I_{o(reces)\ (CANL)}$	Recessive Output Current at Pin CANL	−35 V < V_{CANL} < +35 V; 0 V < V_{CC} < 5.25 V	−2.5	−	+2.5	mA
$I_{LI(CANH)}$	Input Leakage Current to Pin CANH	V_{CC} = 0 V; V_{CANL} = V_{CANH} = 5 V	−10	−	+10	μA
$I_{LI(CANL)}$	Input Leakage Current to Pin CANL	V_{CC} = 0 V; V_{CANL} = V_{CANH} = 5 V	−10	−	+10	μA
$V_{o(dom)\ (CANH)}$	Dominant Output Voltage at Pin CANH	V_{TxD} = 0 V	3.0	3.6	4.25	V
$V_{o(dom)\ (CANL)}$	Dominant Output Voltage at Pin CANL	V_{TxD} = 0 V	0. 5	1.4	1.75	V
$V_{o(dif)\ (bus\_dom)}$	Differential Bus Output Voltage (V_{CANH} − V_{CANL})	V_{TxD} = 0 V; Dominant; 42.5 Ω < R_{LT} < 60 Ω	1.5	2.25	3.0	V
$V_{o(dif)\ (bus\_rec)}$	Differential Bus Output Voltage (V_{CANH} − V_{CANL})	V_{TxD} = V_{CC}; Recessive; No Load	−120	0	+50	mV
$I_{o(sc)\ (CANH)}$	Short Circuit Output Current at Pin CANH	V_{CANH} = 0 V; V_{TxD} = 0 V	−45	−70	−120	mA

CHARACTERISTICS V_{CC} = 4.75 V to 5.25 V; T_J = −40°C to +150°C; R_{LT} = 60 Ω unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BUS LINES (PINS CANH AND CANL)						
$I_{o(sc)\ (CANL)}$	Short Circuit Output Current at Pin CANL	V_{CANL} = 36 V; V_{TxD} = 0 V	45	70	120	mA
$V_{i(dif)\ (th)}$	Differential Receiver Threshold Voltage (see Figure 6)	−5 V < V_{CANL} < +12 V; −5 V < V_{CANH} < +12 V;	0.5	0.7	0.9	V
$V_{ihcm(dif)\ (th)}$	Differential Receiver Threshold Voltage for High Common−Mode (See Figure 6)	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V;	0.40	0.7	1.00	V
$V_{i(dif)\ (hys)}$	Differential Receiver Input Voltage Hysteresis (see Figure 6)	−35 V < V_{CANL} < +35 V; −35 V < V_{CANH} < +35 V;	50	70	100	mV
$R_{i(cm)\ (CANH)}$	Common−Mode Input Resistance at Pin CANH		15	26	37	kΩ
$R_{i(cm)\ (CANL)}$	Common−Mode Input Resistance at Pin CANL		15	26	37	kΩ
$R_{i(cm)\ (m)}$	Matching Between Pin CANH and Pin CANL Common Mode Input Resistance	V_{CANH} = V_{CANL}	−3	0	+3	%
$R_{i(dif)}$	Differential Input Resistance		25	50	75	kΩ
$C_{i(CANH)}$	Input Capacitance at Pin CANH	V_{TxD} = V_{CC}				

MEASUREMENT SETUPS AND DEFINITIONS



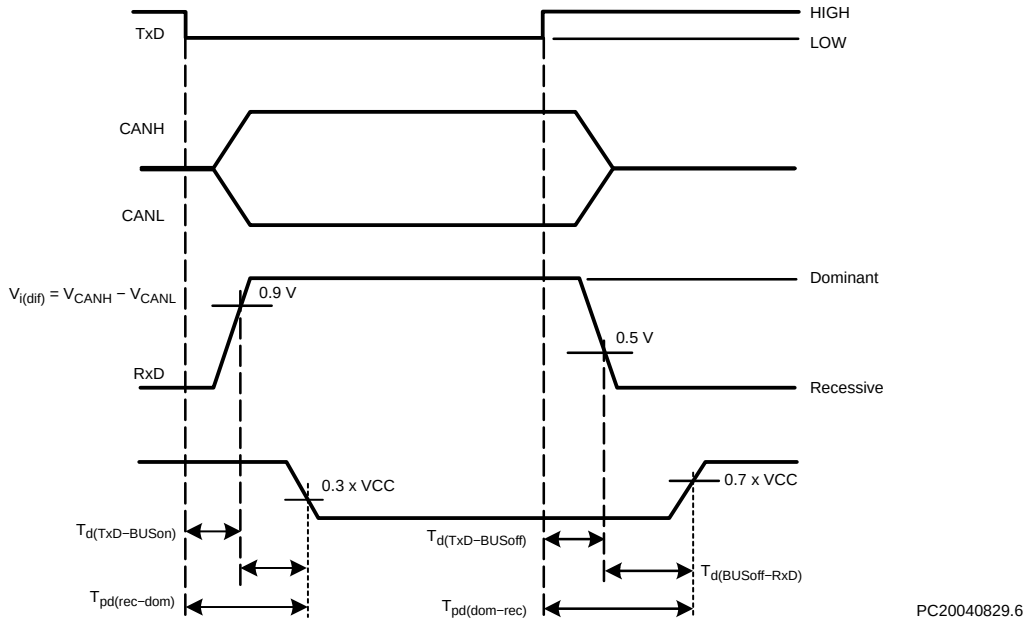


Figure 8. Timing Diagram for AC Characteristics

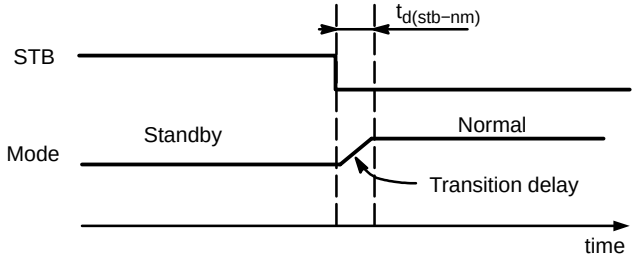
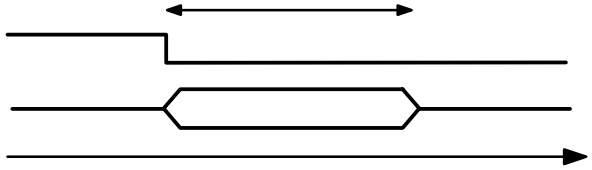


Figure 9. Transition from Standby to Normal



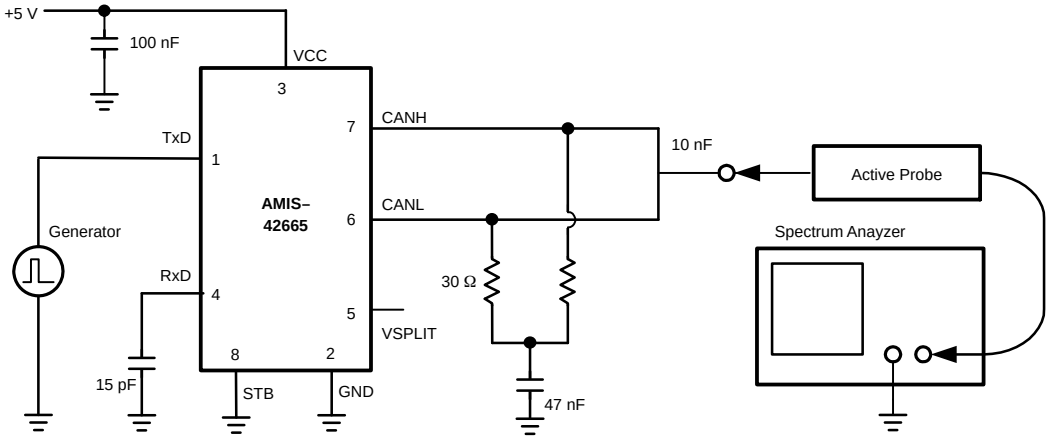
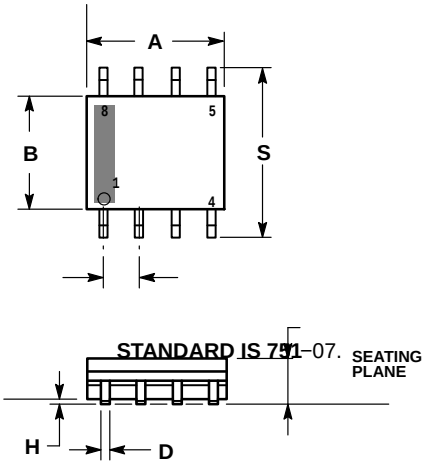


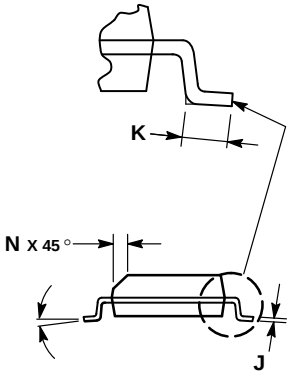
Figure 11. Basic Test Setup for Electromagnetic Measurement

PC20040829.9

PACKAGE DIMENSIONS

SOIC−8
CASE 751−07
ISSUE AK





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.