AMIS-30512

Micro-Stepping Motor Driver

Introduction

The AMIS 30512 is a micro stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. It has an on chip voltage regulator, reset output and watchdog reset, able to supply peripheral devices. The AMIS 30512 contains a current translation table and takes the next micro step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (=direction) register or input pin. The chip provides a so called “speed and load angle” output. This allows the creation of stall detection algorithms and control loops based on load angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS 30512 is implemented in I2T100 technology, enabling both high voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS 30512 is ideally suited for general purpose stepper motor applications in the automotive, industrial, medical, and marine environment.

Key Features

- Dual H Bridge for 2 phase Stepper Motors
- Programmable Peak current up to 800 mA Using a 5 bit Current DAC
- On chip Current Translator
- SPI Interface
- Speed and Load Angle Output
- Seven Step Modes from Full step up to 32 Micro steps
- Fully Integrated Current sense
- PWM Current Control with Automatic Selection of Fast and Slow Decay
- Low EMC PWM with Selectable Voltage Slopes
- Active Fly back Diodes
- Full Output Protection and Diagnosis
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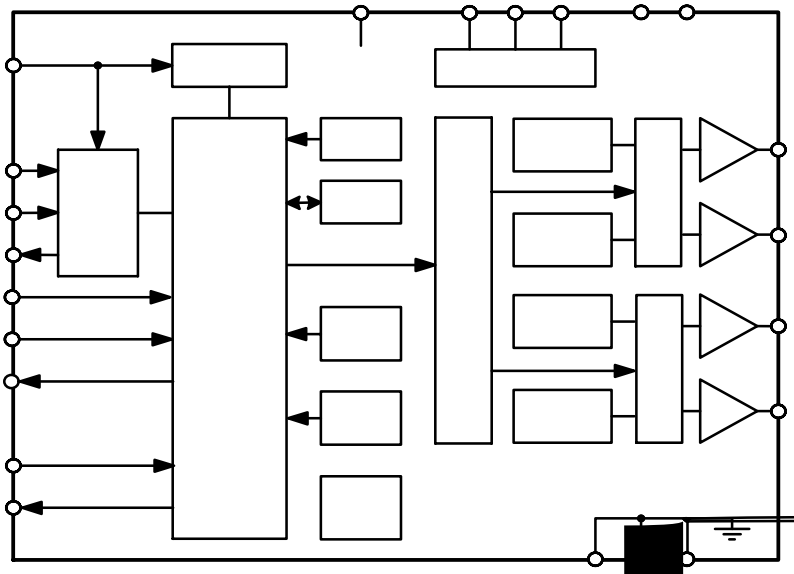

Figure 1. Block Diagram

Table 1. Pin List and Descriptions

Name	Pin	Description
DO	1	SPI data output (open drain)
VDD	2	Logic Supply Input (needs external decoupling capacitor)
GND	3	Ground
DI	4	SPI data in
CLK	5	SPI clock input
NXT	6	Next micro−step input
DIR	7	Direction input
$\overline{\text{ERR}}$	8	Error Output (open drain)
SLA	9	Speed Load Angle Output
CPN	10	Negative connection of charge pump capacitor
CPP	11	Positive connection of charge pump capacitor
VCP	12	Charge−pump filter−capacitor
CLR	13	“Clear” = Chip Reset input
$\overline{\text{CS}}$	14	SPI chip select input
VBB	15	High Voltage Supply Input
MOTYP	16	Negative end of phase Y coil output
GND	17	Ground
MOTYN	18	Positive end of phase Y coil output
MOTXN	19	Positive end of phase X coil output
GND	20	Ground
MOTXP	21	Negative end of phase X coil output
VBB	22	High Voltage Supply Input
$\overline{\text{POR}}$/WD	23	Power−on−reset (POR) and watchdog reset output (open drain)

Table 4. DC Parameters (The DC parameters are given for V_{BB}

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Table 5. AC Parameters (The AC parameters are given for V_{BB} and temperature in their operating ranges.)

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min.	Typ.	Max.	Unit
DIGITAL OUTPUTS							
t_{H2L}	DO ERRB	Output fall-time from V_{inH} to V_{inL}	Capacitive load 50 pF			50	ns
CHARGE PUMP							
f_{CP}	CPN CPP	Charge pump frequency			250		kHz
t_{CPU}	MOTxx	Start-up time of charge pump	For typ. value C_{buffer} and C_{pump}			2	ms
CLR FUNCTION							
t_{CLR}	CLR	Hard reset duration time		20		90	μs
NXT FUNCTION							
t_{NXT_HI}	NXT	NXT minimum, high pulse width	See Figure 2	2			μs
t_{NXT_LO}		NXT minimum, low pulse width	See Figure 2	2			μs
t_{DIR_SET}		NXT hold time, following change of DIR	See Figure 2	0.5			μs
t_{DIR_HOLD}		NXT hold time, before change of DIR	See Figure 2	0.5			

Table 6. SPI Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	SPI clock period	1			µs
t_{CLK_HIGH}	SPI clock high time	100			ns
t_{CLK_LOW}	SPI clock low time	100			ns
t_{SET_DI}	DI set up time, valid data before rising edge of CLK	50			ns
t_{HOLD_DI}	DI hold time, hold data after rising edge of CLK	50			ns
t_{CSB_HIGH}	CSB high time	2.5			µs
t_{SET_CSB}	CSB set up time, CSB low before rising edge of CLK	100			ns
t_{SET_CLK}	CLK set up time, CLK low before rising edge of CSB	100			ns

Figure 5. SPI Timing

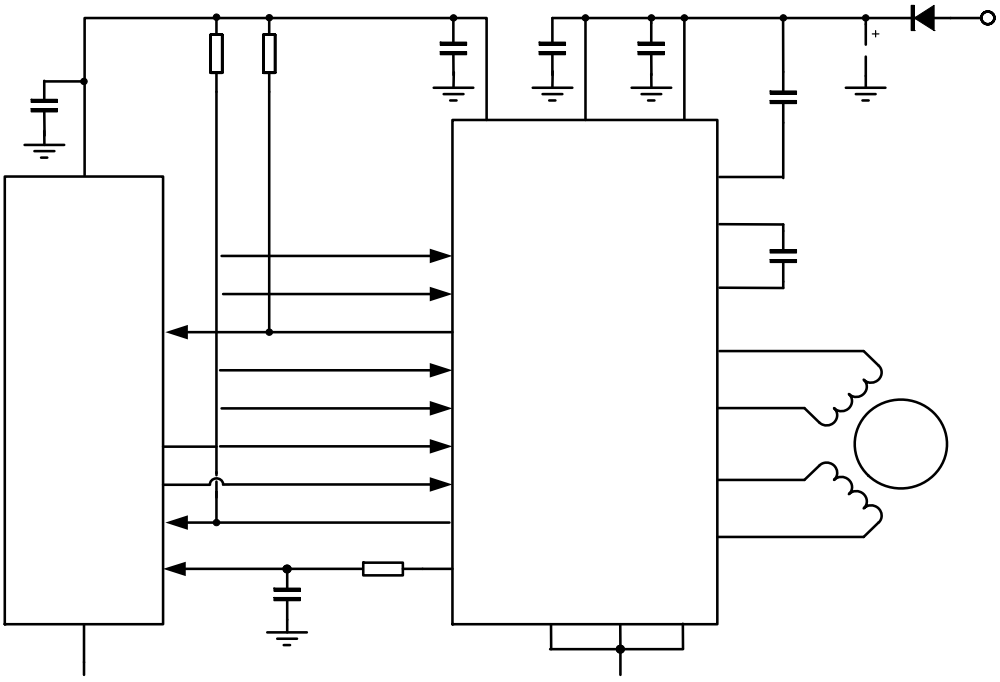


Figure 6. Typical Application Schematic

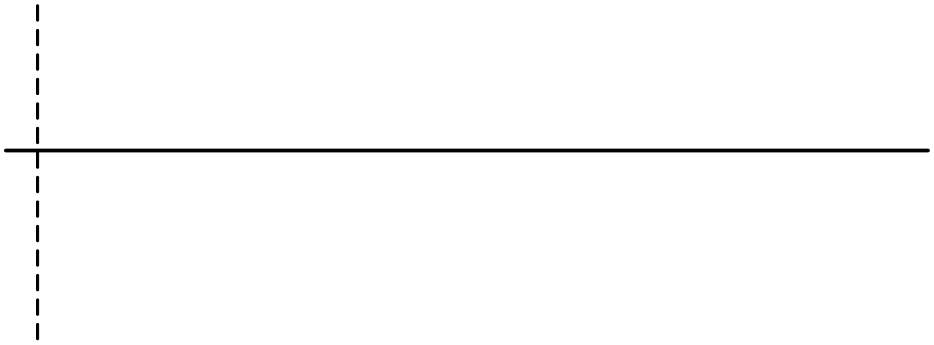


Figure 8. Automatic Duty Cycle Adaptation

Table 9. Circular Translator Table

	Stepmode (SM[2:0])	% of Imax	
MSP[6:0]		**Coil x**	**Coil y**

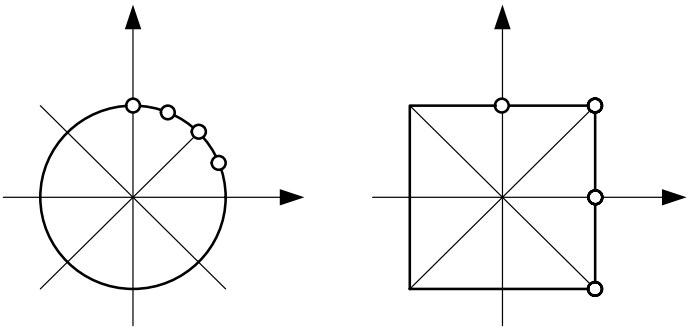


Figure 9. Translator Table: Circular and Square

Speed and Load Angle Output

The SLA pin provides an output voltage that indicates the level of the Back

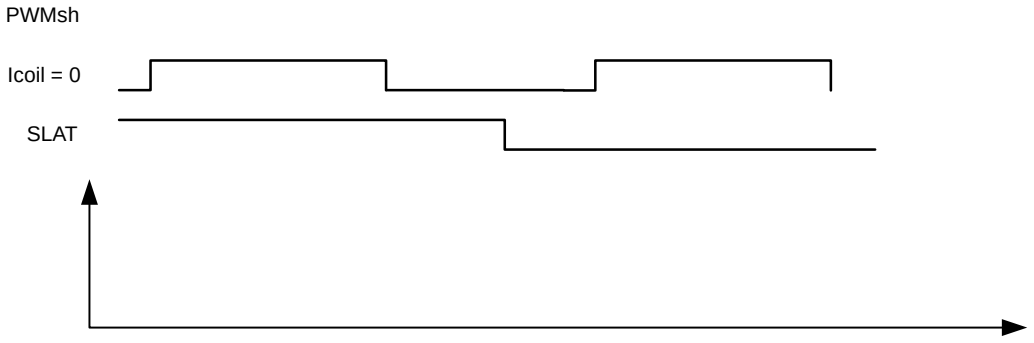


Figure 13. Timing Diagram of SLA−pin

not properly connected to guarantee sufficient low Rdson of the drivers, then the bit <CPFAIL> is set in Table 27: SPI Status Register 0. Also after power on reset the charge pump voltage will need the time t_{CPU} to exceed the required threshold. During that time <CPFAIL> will be set to “1”.

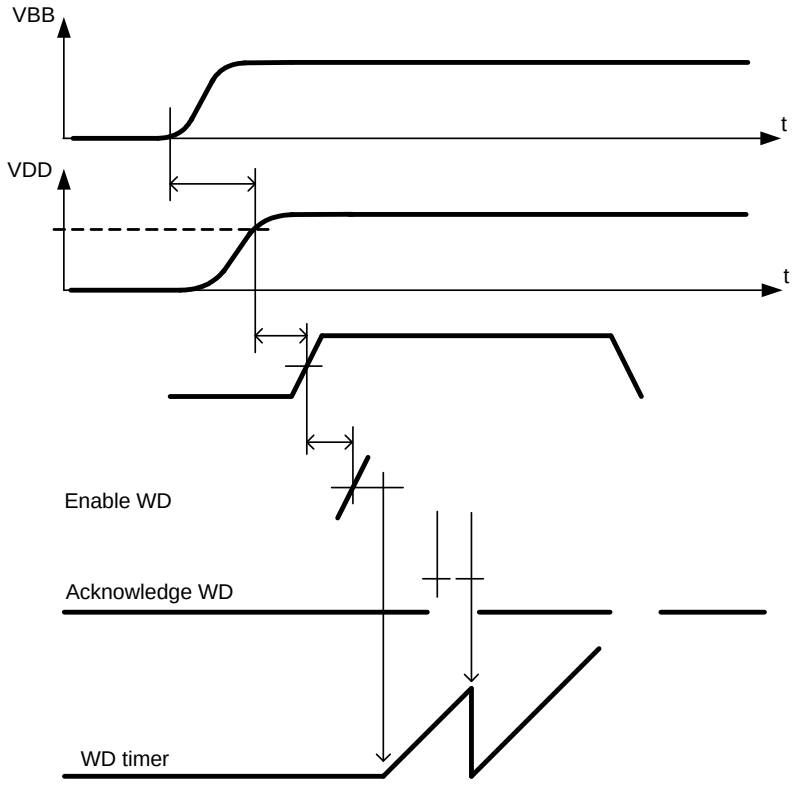
Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR <OVCYij> OR <OPENi> OR <CPFAIL>

Logic Supply Regulator

AMIS-30512 has an on-chip 5 V low-drop regulator with external decoupling capacitor to supply the digital part of the chip, some low-voltage analog blocks and external circuitry. The voltage is derived from an internal bandgap reference. To calculate the available drive-current for external circuitry, the specified $I_{load.14mo5.95341\ 47.792\ 2.81\ T9.81\ Tlon\ 5.953491.\ d1\ i\ q}$


VBB
t
VDD
t
Enable WD
Acknowledge WD
WD timer

SPI Interface

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS 30512. The implemented SPI block is designed to interface directly with numerous micro controllers from several manufacturers. AMIS 30512 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS 30512), and DI signal is the output from the Master. A chip select line (CSB) allows individual selection of a Slave SPI device in a multiple slave system. The CSB line is active low. If AMIS 30512 is not selected, DO is pulled up with the external pull up resistor. Since AMIS 30512 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes.

The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

Figure 16. Timing Diagram of a SPI Transfer

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS 30512 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS

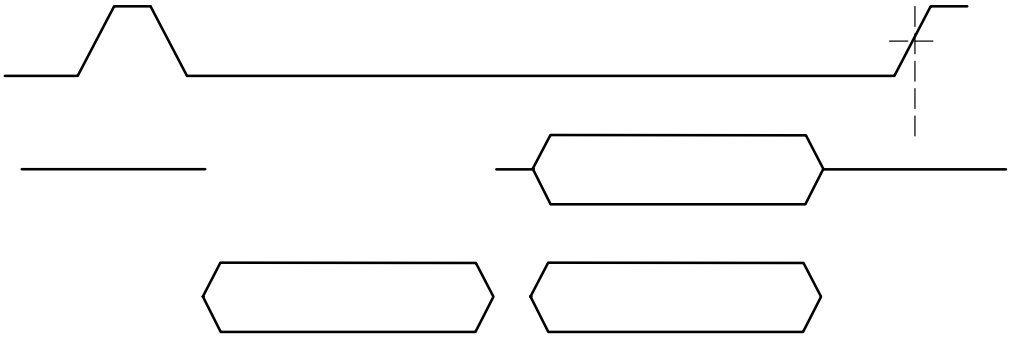


Figure 19. Single WRITE Operation where DATA from the Master is Written in SPI Register with Address 3

SPI Control Registers

All SPI control registers have Read/Write access and default to “0” after power on or hard reset.

Table 12. SPI Control Register WR

Control Register (WR)									
		Structure							
Address	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	WDEN	WDT[3:0]				–	–	–

Where:

R/W Read and Write access
Reset: Status after power-On or hard reset
WDEN: Watchdog enable. Writing “1” to this bit will activate the watchdog timer (if not enabled yet) or will clear this timer (if already enabled). Writing “0” to this bit will clear WD bit (SPI Status Register 0).
WDT[3:0]: Watchdog timeout interval

Table 13. SPI Control Register 0

Control Register 0 (CR0)									
		Structure							
Address	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	SM[2:0]			CUR[4:0]				

Where:

R/W Read and Write access
Reset: Status after power On or hard reset
SM[2:0]: Step mode
CUR[4:0]: Current amplitude

Table 14. SPI Control Register 1

Control Register 1 (CR1)									
		Structure							
Address	Content	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	DIRCTRL	NXTP	–	–	PWMF	PWMJ	EMC[1:0]	

Where:

R/W Read and Write access
Reset: Status after power on or hard reset
DIRCTRL Direction control
NXTP NEXT polarity
PWMF PWM frequency
PWMJ PWM jitter
EMC[1:0] EMC slope control

Table 15. SPI Control Register 2

Control Register 2 (CR2)	
Address	**Content**

eter Overview CUR[4:0]

		Current (mA)	Index	CUR[4:0]					Current (mA)
)	0	15	10	1	0	0	0	0	181
)	1	30	11	1	0	0	0	1	200
)	0	45	12	1	0	0	1	0	221
)	1	50	13	1	0	0	1	1	244
)	0	55	14	1	0	1	0	0	269
)	1	61	15	1	0	1	0	1	297
)	0	67	16	1	0	1	1	0	328
)	1	74	17	1	0	1	1	1	362
)	0	82	18	1	1	0	0	0	400
)	1	91	19	1	1	0	0	1	441
)	0	100	1A	1	1	0	1	0	487
)	1	110	1B	1	1	0	1	1	538
)	0	122	1C	1	1	1	0	0	594
)	1	135	1D	1	1	1	0	1	656
)	0	149	1E	1	1	1	1	0	724
)	1	164	1F	1	1	1	1	1	800

dV/dt of the PWM voltage slopes on the motor pins.

eter Overview EMC[1:0]

Slope (V/μs)	Remark
150	Turn−on and turn−off voltage slope 10% to 90%
100	”

SPI Status Register Description

All four SPI status registers have Read Access and are default to “0” after power on or hard reset.

Table 27. Status Register 0 (SR0)

Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	TW	CPfail	–	OPENX	OPENY	–	–

Where:

R	Read only mode access
Reset	Status after power on or hard reset
PAR	Parity check
TW	Thermal warning
Cpfail	Charge pump failure
OPENX	Open Coil X detected
OPENY	Open Coil Y detected

Remark: Data is **not** latched

Table 28. Status Register 1 (SR1)

Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0			

Soldering

Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS “Data Handbook IC26; Integrated Circuit Packages” (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards (PCB) with high population densities. In these situations re-flow soldering is often used.

Re−flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the PCB by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for re-flowing; for example, infrared/convection heating in a conveyor type oven.

Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on the heating method. Typical re-flow peak temperatures range from 215 to 260°C. The top-surface temperature of the packages should preferably be kept below 230°C.

Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or PCBs with a high component density, as solder bridging and non-wetting can

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