[redacted]

Primary camera interface

ORDERING INFORMATION

Adaptive Local Tone Mapping (ALTM)
Test Pattern Generator
Twoĭwire serial programming interface

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AP0101CS2L00SPGA0−DR1	1Mp Co−Processor, 100−ball VFBGA	Drypack
AP0101CS2L00SPGAD3−GEVK	AP0101CS Demo Kit	
AP0101CS2L00SPGAH−GEVB	AP0101CS Head Board	

5. See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

FUNCTIONAL OVERVIEW

Figure 1 shows the typical configuration of the AP0101CS in a camera system. On the host side, a two−wire serial interface is used to control the operation of the AP0101CS, and image data is transferred using the parallel bus between the AP0101CS and the host. The AP0101CS interface to the sensor also uses a parallel interface.

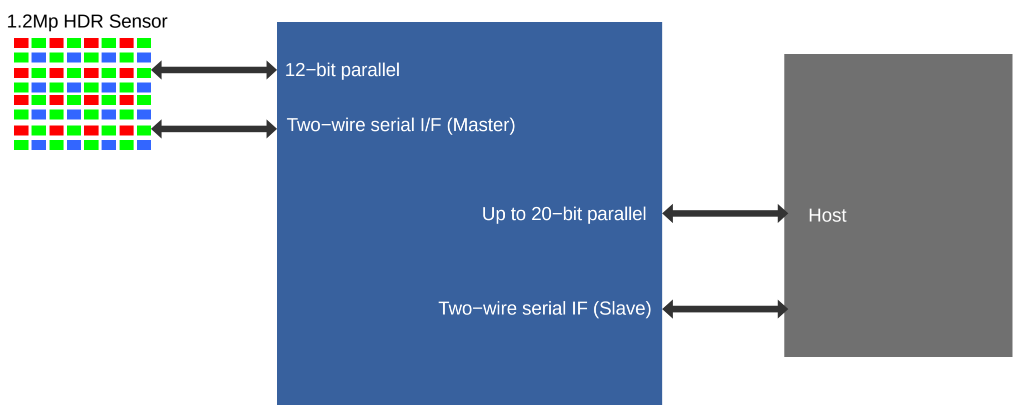
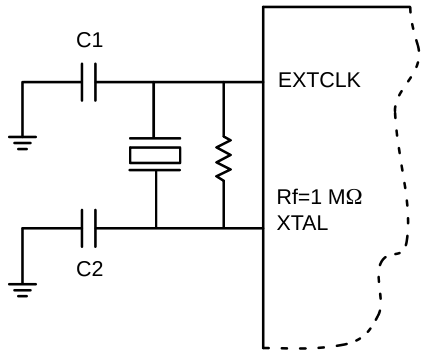


Figure 1. AP0101CS Connectivity

SYSTEM INTERFACES

Figure 2 shows typical AP0101CS device connections. All power supply rails must be decoupled from ground using capacitors as close as possible to the package. The AP0101CS signals to the sensor and host interfaces can be at different supply voltage levels to optimize power consumption and maximize flexibility. Table 4 provides the signal descriptions for the AP0101CS.



NOTE: Rf represents the feedback resistor, an Rf value of 1 MΩ would be sufficient for AP0101CS. C1 and C2 are decided according to the crystal or resonator CL specification. In the steady state of oscillation, CL is defined as (C1 x C2)/(C1+C2). In fact, the I/O ports, the bond pad, package pin and PCB traces all contribute the parasitic capacitance to C1 and C2. Therefore, CL can be rewritten to be (C1* x C2*)/(C1*+C2*), where C1*=(C1+Cin, stray) and C2*=(C2+Cout, stray). The stray capacitance for the IO ports, bond pad and package pin are known which means the formulas can be rewritten as C1*=(C1+1.5pF+Cin, PCB) and C2*=(C2+1.3pF+Cout, PCB).

Figure 3. Using a Crystal Instead of External Oscillator

Table 4. PIN DESCRIPTIONS

Name	Type	Description
EXTCLK	Input	Master input clock, nominally 27 MHz. This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected) or direct connection to a crystal.
XTAL	Output	If EXTCLK is connected to one pin of a crystal, this signal is connected to the other pin, otherwise this signal must be left unconnected.
RESET_BAR	Input/PU	Master reset signal, active LOW. This signal has an internal pull up.
S_{CLK}	Input	Two−wire serial interface clock (host interface).
S_{DATA}	Input/Output	Two−wire serial interface data (host interface).
S_{ADDR}	Input	Selects device address for the two−wire slave serial interface. When connected to GND, the device ID is 0x90. When wired to V_{DD}IO_H, a device ID of 0xBA is selected.
FRAME_SYNC	Input	This input can be used to set the output timing of the AP0101CS. This signal should be connected to GND if not used.
STANDBY	Input	Standby mode control, active HIGH.
SPI_S_{CLK}	Output	Clock output for interfacing to an external SPI flash or EEPROM memory
SPI_SDI	Input	Data in from SPI flash or EEPROM memory. When no SPI device is fitted, this signal is used to determine whether the AP0101CS should auto−configure: 0: Do not auto−configure; two−wire interface will be used to configure the device (host−config mode) 1: Auto−configure. This signal has an internal pull−up resistor
SPI_SDO	Output	Data out to SPI flash or EEPROM memory

Power Up and Down Sequence

Powering up and down the AP0101CS requires voltages to be applied in a particular order, as seen in Figure 4. The timing requirements are shown in Table 6. The AP0101CS includes a power-on reset feature that initiates a reset upon power up of the AP0101CS.

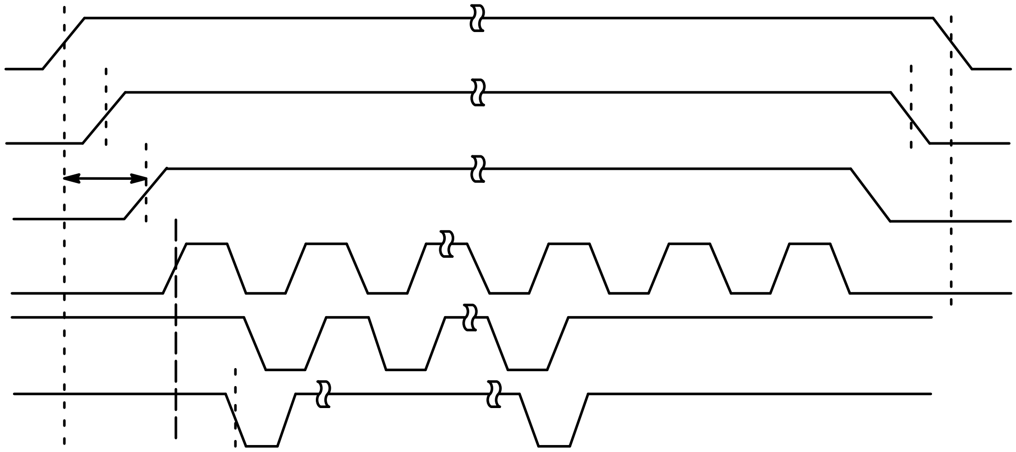


Table 7. OUTPUT STATES (continued)

Name	Hardware States	Firmware States		Notes
		Streaming	Idle	

Hard Reset

The AP0101CS enters the reset state when the external RESET_BAR signal is asserted LOW, as shown in Figure 5. All the output signals will be in High−Z state.

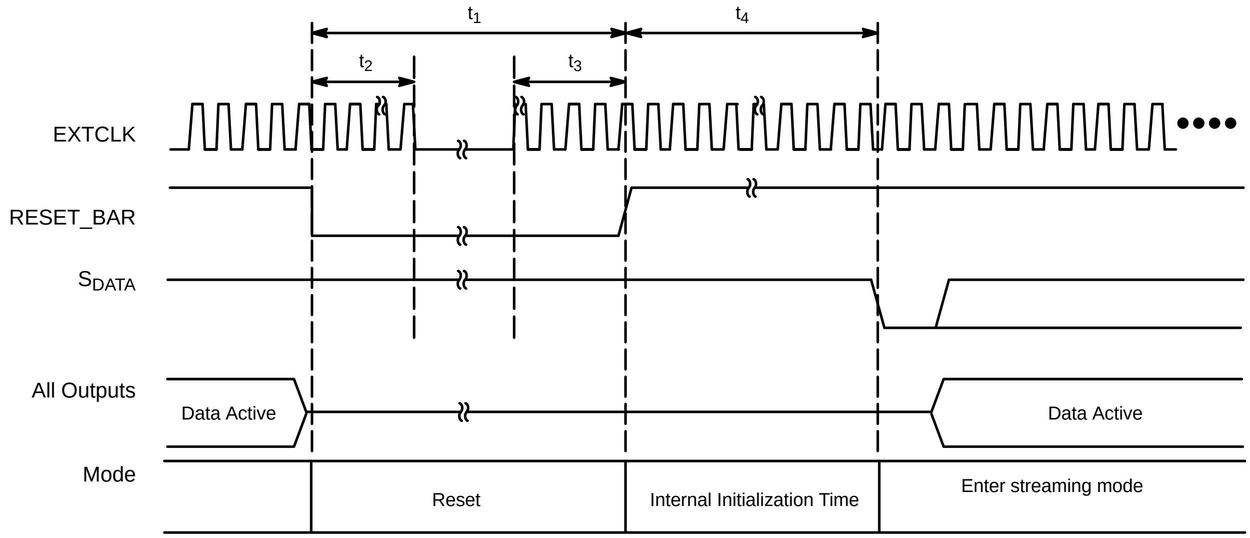


Figure 5. Hard Reset Operation

Table 8. HARD RESET

Symbol	Parameter	Min	Typ	Max	Unit
t_1	RESET_BAR pulse width	50	−	−	EXTCLK cycles
t_2	Active EXTCLK required after RESET_BAR asserted	10	−	−	
t_3	Active EXTCLK required before RESET_BAR de−asserted	10	−	−	
t_4	First two−wire serial interface communication after RESET_BAR is HIGH	100	−	−	

Soft Reset

A soft reset sequence to the AP0101CS can be activated by writing to a register through the two−wire serial interface.

Hard Standby Mode

The AP0101CS can enter hard standby mode by using the external STANDBY signal, as shown in Figure 6.

Entering Standby Mode

1. Assert STANDBY signal HIGH.

Exiting Standby Mode

1. De−assert STANDBY signal LOW.

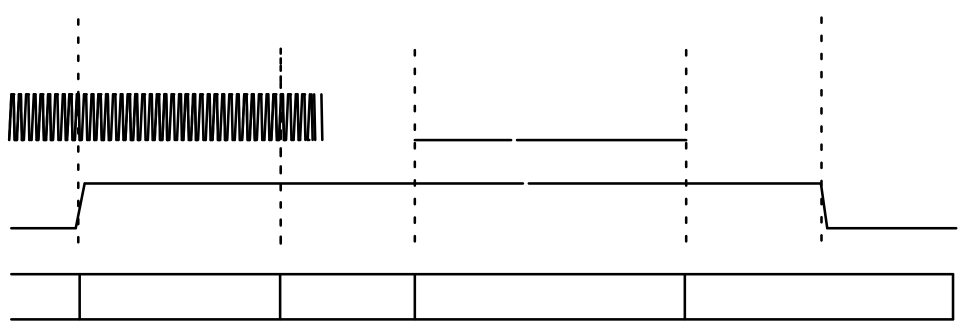
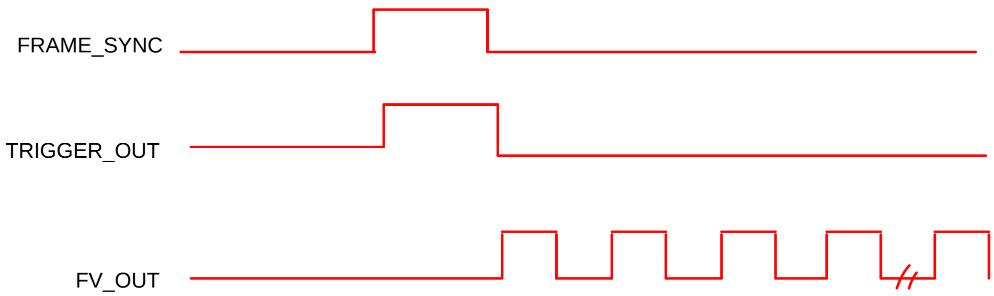


Table 9. HARD STANDBY SIGNAL TIMING

Symbol	Parameter	Min	Typ	Max	Unit



NOTE: This diagram is not to scale.

Figure 8. Continuous Mode

When two or more cameras have a signal applied to the FRAME_SYNC input at the same time, the respective FV_OUT signals would be synchronized within five PIXCLK_OUT cycles. This assumes that all cameras have the same configuration settings and that the exposure time is the same.

IMAGE FLOW PROCESSOR

Image and color processing in the AP0101CS is implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operating parameters. For normal operation of the AP0101CS, a stream of raw image data from the attached image sensor is fed into the color pipeline. The user also has the option to select a number of test patterns to be input instead of sensor data. The test pattern is fed to the IFP for testing the image pipeline without sensor operation.

The test patterns can be selected by programming variables. To select enter test pattern mode, set R0xC88F to 0x02 and issue a Changeĭ Config request; to exit this mode, set R0xC88F to 0x00.

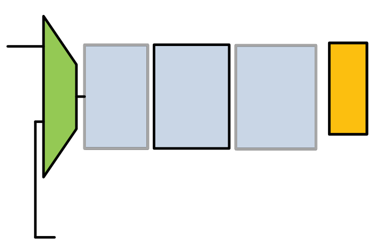
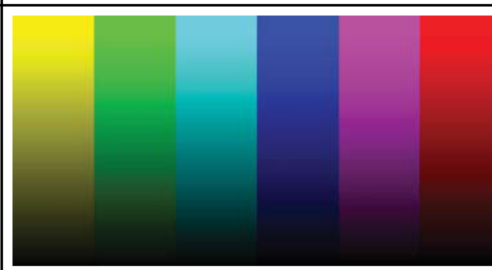


Figure 9. Continuous Mode

Test Patterns

Table 11. TRIGGER TIMING

Test Pattern	Example
FLAT FIELD FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x01 FIELD_WR= CAM_MODE_TEST_PATTERN_RED, 0x000FFFFF FIELD_WR= CAM_MODE_TEST_PATTERN_GREEN, 0x000FFFFF FIELD_WR= CAM_MODE_TEST_PATTERN_BLUE, 0x000FFFFF Load = Change−Config Changing the values in R0xC890−R0xC898 will change the color of the test pattern.	
100% Color Bar FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x02 Load = Change−Config	
Pseudo−Random FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x05 Load = Change−Config	
Fade−to−Gray FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x08 Load = Change−Config	
Linear Ramp FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x09 Load = Change−Config	

Defect Correction

After data decompanding the image stream processing starts with defect correction.

To obtain defect free images, the pixels marked defective during sensor readout and the pixels determined defective by the defect correction algorithms are replaced with values derived from the non−defective neighboring pixels. This image processing technique is called defect correction.

AdaCD (Adaptive Color Difference)

Automotive applications require good performance in extremely low light, even at high temperature conditions. In these stringent conditions the image sensor is prone to higher noise levels, and so efficient noise reduction techniques are required to circumvent this sensor limitation and deliver a high quality image to the user.

The AdaCD Noise Reduction Filter is able to adapt its noise filtering process to local image structure and noise level, removing most objectionable color noise while preserving edge details.

Black Level Subtraction and Digital Gain

After noise reduction, the pixel data goes through black level subtraction and multiplication of all pixel values by a programmable digital gain. Independent color channel digital gain can be adjusted with registers. Black level subtract (to compensate for sensor data pedestal) is a single value applied to all color channels. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The AP0101CS has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The correction functions

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row, col) = P_{sensor}(row, col) \times f(row, col) \qquad \text{(eq. 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

Adaptive Local Tone Mapping (ALTM)

Real world scenes often have very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest object in a scene. In recent years many technologies have been developed to capture the full dynamic range of real world scenes. For example, the multiple exposure method is a widely adopted method for capturing high dynamic range images, which combines a series of low dynamic range images of the same scene taken under different exposure times into a single HDR image.

Even though the new digital imaging technology enables the capture of the full dynamic range, low dynamic range display devices are the limiting factor. Today's typical LCD monitor has contrast ratio around 1,000:1; however, it is not atypical for an HDR image having contrast ratio around 250,000:1. Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping.

Tone mapping methods can be classified into global tone mapping and local tone mapping. Global tone mapping methods apply the same mapping function to all pixels. While global tone mapping methods provide computationally simple and easy to use solutions, they often cause loss of contrast and detail. A local tone mapping is thus necessary in addition to global tone mapping for the reproduction of visually more appealing images that also reveal scene details that are important for automotive safety and surveillance applications. Local tone mapping methods use a spatially varying mapping function determined by the neighborhood of a pixel, which allows it to increase the local contrast and the visibility of some details of the image. Local methods usually yield more pleasing results because they exploit the fact that human vision is more sensitive to local contrast.

onsemi's ALTM solution significantly improves the performance over global tone mapping. ALTM is directly applied to the Bayer domain to compress the dynamic range from 20-bit to 12-bit. This allows the regular color pipeline to be used for HDR image rendering.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 20- or 12-bit integer number, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including ALTM, preserve the one-color-per-pixel nature of the data stream, but after ALTM it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color correction and aperture correction colorĭcorrected image data. The gain and threshold for 2D correction can be defined through register settings.

Gamma Correction

The gamma correction curve is implemented as a piecewise linear function with 33 knee points, taking 12ĭbit arguments and mapping them to 10ĭbit output. The abscissas of the knee points are fixed at 0, 8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384, 448, 512, 640, 768, 896, 1024, 1280, 1536, 1792, 2048, 2560, 3072, 3584, and 4096. The 10ĭbit ordinates are programmable through variables.

The AP0101CS has the ability to calculate the 33ĭpoint knee points based on the tuning of cam_ll_gamma and cam_ll_contrast_gradient_bright. The other method is for the host to program the 33 knee point curve themselves.

Also included in this block is a Fadeĭto Black curve which sets all knee points to zero and causes the image to go black in extreme low light conditions.

Color Kill

To remove highĭor lowĭlight color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by oneĭdimensional lowĭpass filtering of Y and/or UV signals is possible. A 3ĭ or 5ĭtap filter can be selected for each signal.

CAMERA CONTROL AND AUTO FUNCTIONS

Auto Exposure

The auto exposure algorithm optimizes scene exposure to minimize clipping and saturation in critical areas of the image. This is achieved by controlling exposure time and analog gains of the sensor core as well as digital gains applied to the image.

The auto exposure module analyzes image statistics collected by the exposure measurement engine, makes a decision, and programs the sensor and color pipeline to achieve the desired exposure. The measurement engine subdivides the image into 25 windows organized as a 5 x 5 grid.

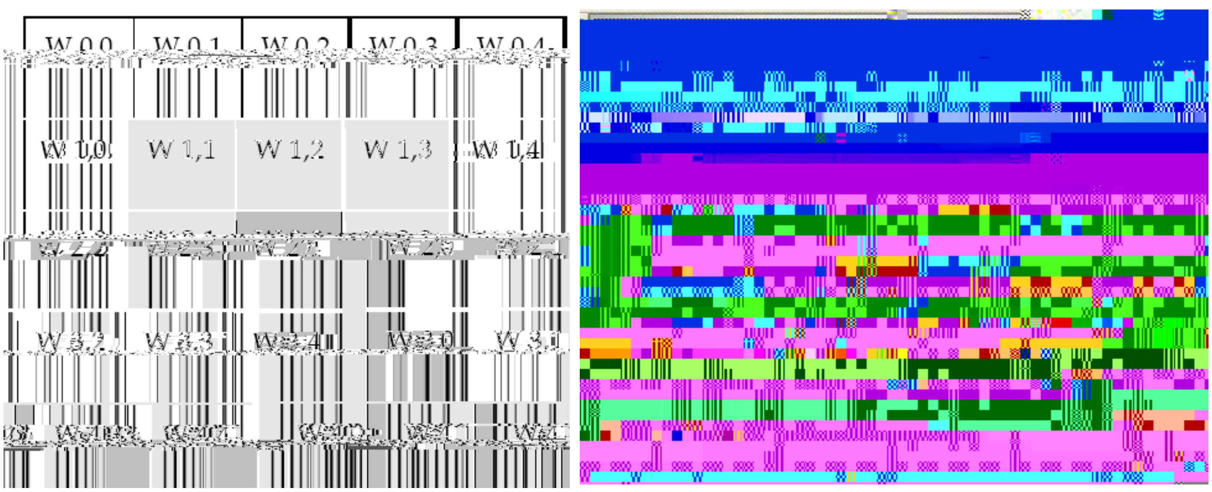


Figure 10. 5 x 5 Grid

AE TRACK DRIVER

Other algorithm features include the rejection of fast fluctuations in illumination (time averaging), control of speed of response, and control of the sensitivity to small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters described above.

The driver changes AE parameters (integration time, gains, and so on) to drive scene brightness to the programmable target.

To avoid unwanted reaction of AE on small fluctuations of scene brightness or momentary scene changes, the AE track driver uses a temporal filter for luma and a threshold around the AE luma target. The driver changes AE parameters only if the difference between the AE luma target and the filtered luma is larger than the AE target step and pushes the luma beyond the threshold.

AUTO WHITE BALANCE

The AP0101CS has a builtĭin AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a driver performing the selection of the optimal color correction matrix and IFP digital gain. While default settings of these algorithms are adequate in most situations,

Table 14. YCbCr OUTPUT MODES (cam_port_parallel_msb_align=0x0, cam_port_parallel_swap_bytes = 0, cam_output_format_yuv_swap_red_blue = 0)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (D_{OUT} [7:0])	Cbi	Cri	

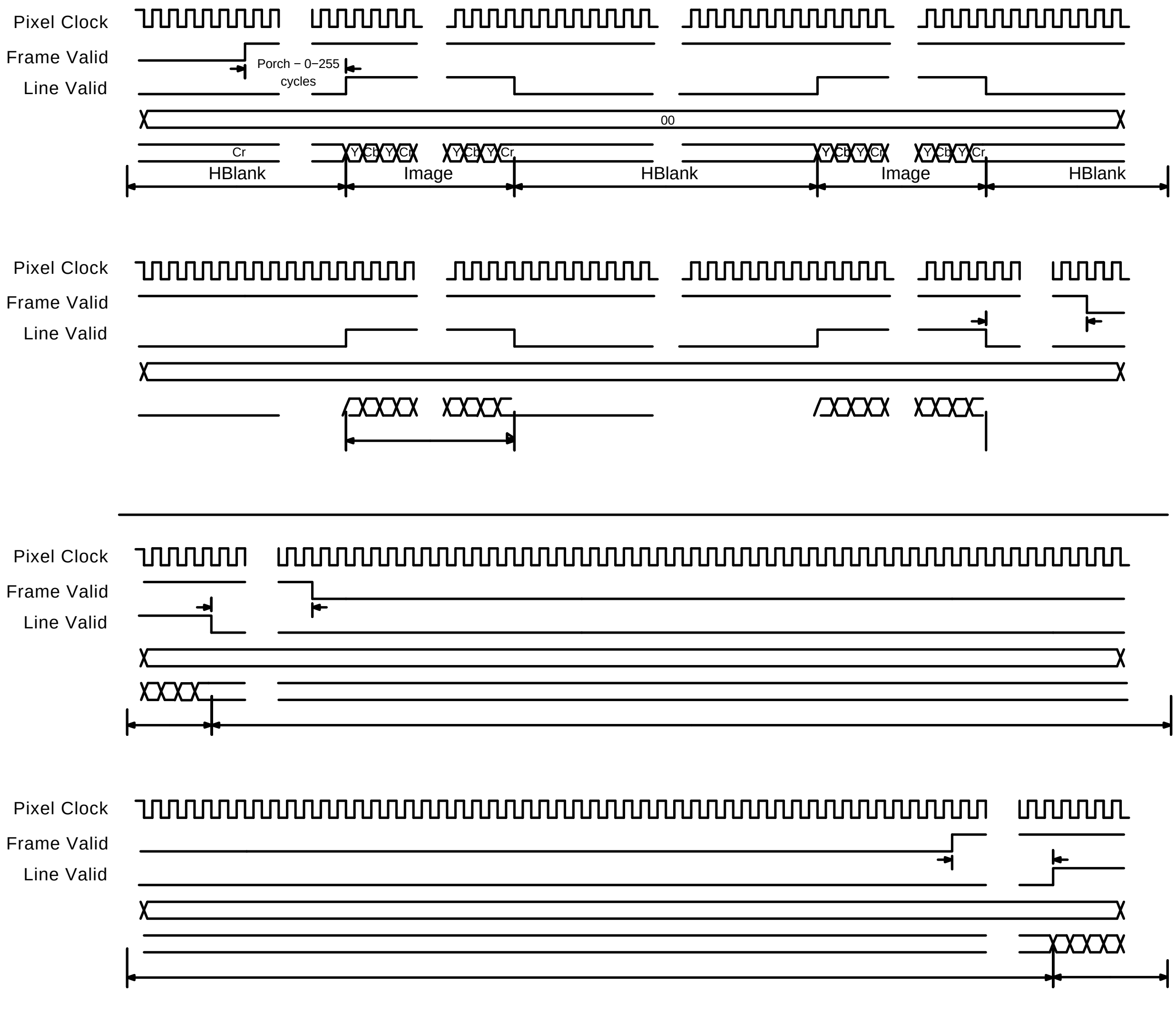


Figure 12. 10 bit YCbCr Output (YCbCr_422_10_10)

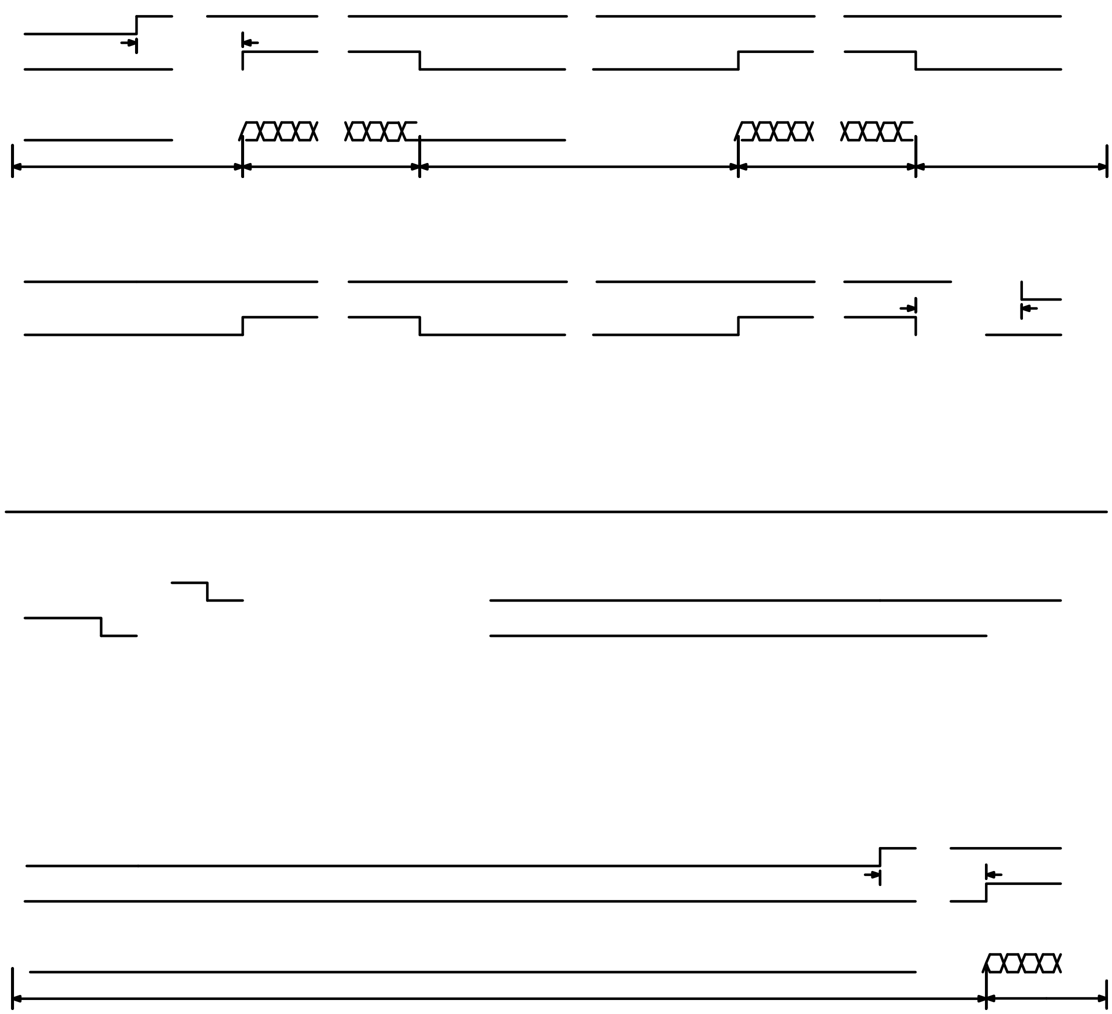


Figure 13. 16 bit YCbCr Output (YCbCr_422_16)

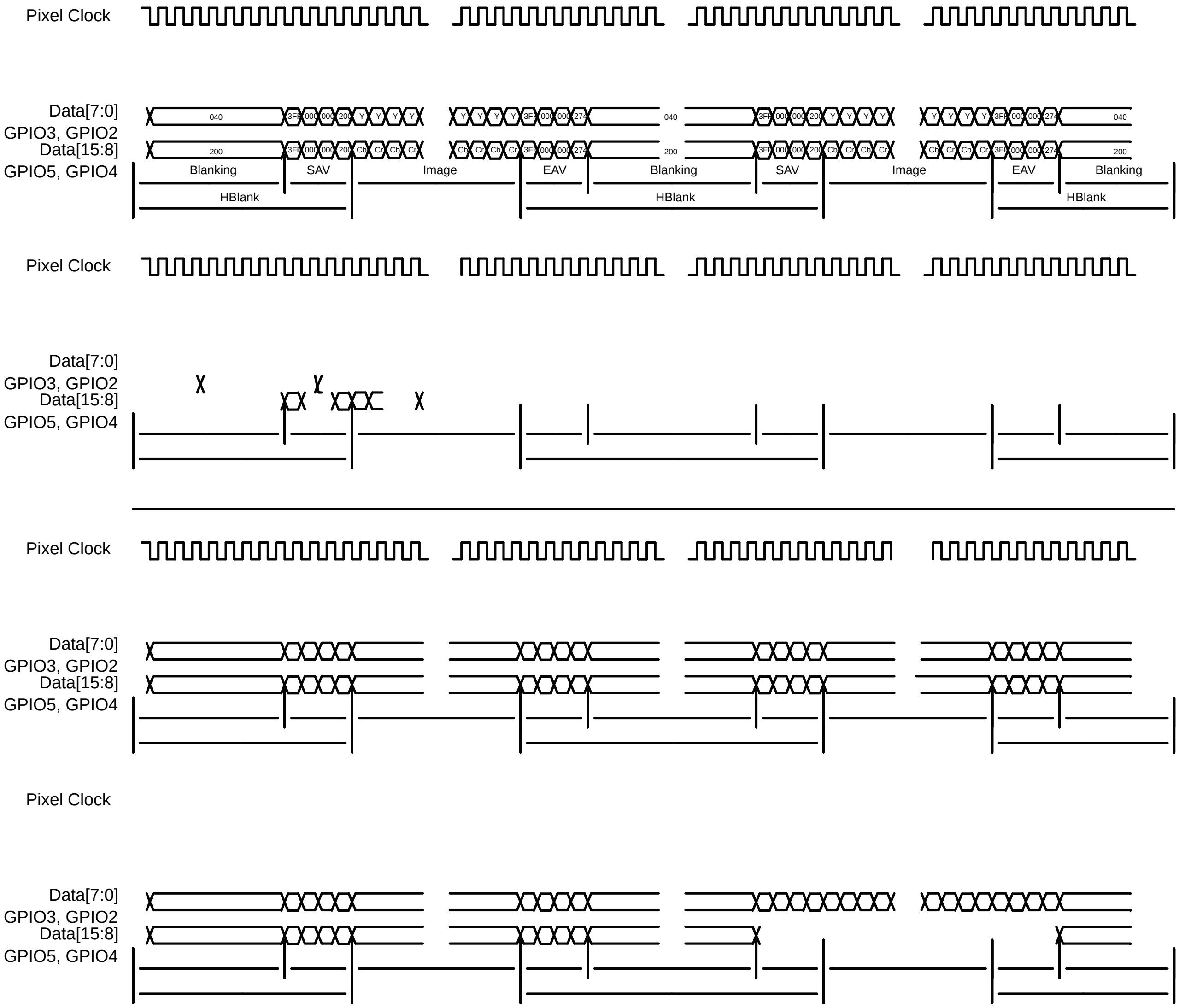


Figure 14. SMPTE296M Output

generates a (re)start condition and the 8ĭbit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8ĭbit transfer. The data transfer is stopped when the master sends a noĭacknowledge bit.

Single READ from random location

Figure 15 shows the typical READ cycle of the host to the AP0101CS. The first two bytes sent by the host are an

USAGE MODES

How a camera based on the AP0101CS will be configured depends on what features are used. In the simplest case, an AP0101AT operating in Auto−Config mode with no customized settings might be sufficient.

In the simplest case no EEPROM or Flash memory or µC is required, as shown in Figure 21.

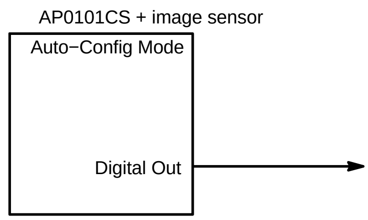


Figure 21. Auto−Config Mode

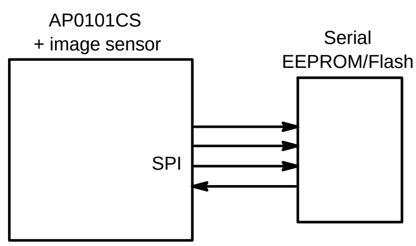
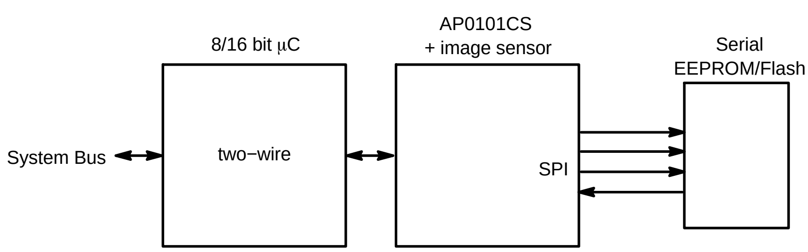


Figure 22. Flash Mode



NOTE: In this configuration all settings are communicated to the AP0101CS and sensor through the micro−controller.

Figure 23. Host Mode with Flash

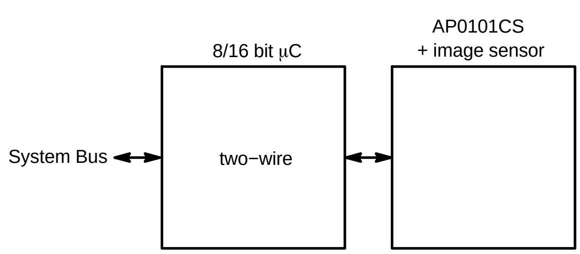


Figure 24. Host Mode

Supported NVM Devices

The AP0101AT supports a variety of SPI NVM devices. Refer to the Flash/EEPROM programming section of the Developer Guide for details.

HOST COMMAND INTERFACE

The AP0101CS has a mechanism to execute higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on−chip firmware and the results are reported back. EEPROM or Flash memory is also available to store commands for later execution. For details on the host command interface and host commands, refer to the Host Command Interface document.

ELECTRICAL SPECIFICATIONS

Caution: Stresses greater than those listed in Table 19 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{DD}_REG	Digital power (1.8 V)	−0.3	4.95	V
V_{DD}IO_H	Host I/O power (2.5 V, 3.3 V)	2.25	5.4	V
V_{DD}IO_S	Sensor I/O power (1.8 V, 2.8 V)	1.7	5.4	V
V_{DD}	Digital core power	1.1	2.5	V
V_{DD}_PLL	PLL power	1.1	2.5	V
V_{DD}IO_OTPM	OTPM power	2.25	5.4	V
V_{IN}	DC Input Voltage	−0.3	V_{DD}IO_* + 0.3	V
V_{OUT}	DC Output Voltage	−0.3	V_{DD}IO_* + 0.3	V
T_{STG}	Storage Temperature	−50	150	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 20. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Supply input to on−chip regulator (V_{DD}_REG)	1.62	1.8	1.98	V
Host IO voltage (V_{DD}IO_H)	2.25	2.5/3.3	3.6	V
Sensor IO voltage (V_{DD}IO_S)	1.7	1.8/2.8	3.1	V
Core voltage (V_{DD})	1.08	1.2	1.32	V
PLL voltage (V_{DD}_PLL)	1.08	1.2	1.32	V
OTPM power supply (V_{DD}IO_OTPM)	2.25	2.5/3.3	3.6	V
Functional operating temperature (ambient − T_A)	−30		70	C
Storage Temperature	−55		150	C

Table 24. STANDBY CURRENT CONSUMPTION

f_{EXTCLK}= 27 MHz, V_{DD}_REG = 1.8 V; V_{DDI}O_S = 1.8 V, V_{DDI}O_OTPM = V_{DDI}O_H = 3.3 V, T_A = 50 C, excludes V_{DDI}O_H current

Symbol	Parameter	Condition	Typ	Max	Unit
Hard standby	Total standby current when asserting the STANDBY signal		1.6		mA
Standby power			2.9		mW
Soft standby (clock on)	Total standby current	f_{EXTCLK} = 27 MHz	2.1		mA
Standby power			3.8		mW

Table 25. INRUSH CURRENT

Supply	Max. Current
V_{DD}_REG (1.8 V)	150 mA
V_{DD}IO_H (2.5/3.3 V)	80 mA

Table 27. MASTER TWO WIRE SERIAL BUS CHARACTERISTICS (CCIM) (continued)
(Default Setup Conditions: f_{EXTCLK} = 27 MHz, V_{DD}IO_H = V_{DD}_OTPM = 2.8 V, V_{DD}_REG = V_{DD}IO_S = 1.8 V, T_A = 25 C unless otherwise stated)

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
Fall time of both M_S_{DATA} and M_S_{CLK}						