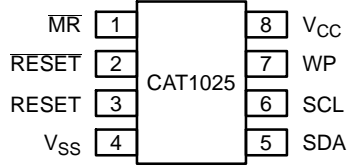
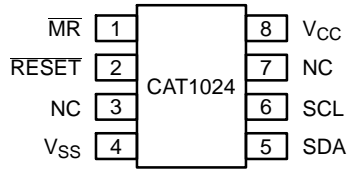


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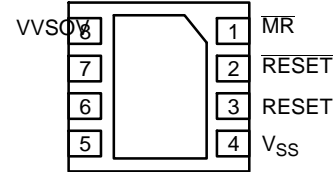
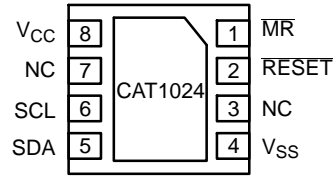
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PIN CONFIGURATION

DIP Package (L)
 SOIC Package (W)
 TSSOP Package (Y)
 MSOP Package (Z)



(Bottom View)
 TDFN Package: 3 mm x 3 mm
 0.8mm maximum height – (ZD4)



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Table 4. CAT102X FAMILY OVERVIEW

Device	Manual Reset Input Pin	Watchdog	Watchdog Monitor Pin	Write Protection Pin	Independent Auxiliary Voltage Sense	RESET: Active High and LOW	EEPROM
CAT1021	✓	✓	SDA	✓		✓	2k
CAT1022	✓	✓	SDA				2k
CAT1023	✓	✓	WDI			✓	2k
CAT1024	✓						2k
CAT1025	✓			✓		✓	2k
CAT1026					✓	✓	2k
CAT1027		✓	WDI		✓		2k

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

SPECIFICATIONS

Table 5. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	°C
Storage Temperature	-65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	-2.0 to $V_{CC} + 2.0$	V
V_{CC} with Respect to Ground	-2.0 to 7.0	V
Package Power Dissipation Capability ($T_A = 25^\circ\text{C}$)	1.0	W
Lead Soldering Temperature (10 s)	300	°C

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Table 6. D.C. OPERATING CHARACTERISTICS

$V_{CC} = 2.7\text{ V}$ to 5.5 V and over the recommended temperature conditions unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{TH}	Reset Threshold	CAT102x-45 ($V_{CC} = 5.0\text{ V}$)	4.50		4.75	V
		CAT102x-42 ($V_{CC} = 5.0\text{ V}$)	4.25		4.50	
		CAT102x-30 ($V_{CC} = 3.3\text{ V}$)	3.00		3.15	
		CAT102x-28 ($V_{CC} = 3.3\text{ V}$)	2.85		3.00	
		CAT102x-25 ($V_{CC} = 3.0\text{ V}$)	2.55		2.70	
V_{RVALID}	Reset Output Valid V_{CC} Voltage		1.00			V
V_{RT} (Note 4)	Reset Threshold Hysteresis		15			mV

- V_{IL} min and V_{IH} max are reference values only and are not tested.
- This parameter is tested initially and after a design or process change that affects the parameter. Not 100% tested.

Table 7. CAPACITANCE

$T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = 5\text{ V}$

Symbol	Test	Test Conditions	Max	Units
C_{OUT} (Note 5)	Output Capacitance	$V_{OUT} = 0\text{ V}$	8	pF
C_{IN} (Note 5)	Input Capacitance	$V_{IN} = 0\text{ V}$	6	pF

Table 8. AC CHARACTERISTICS

$V_{CC} = 2.7\text{ V}$ to 5.5 V and over the recommended temperature conditions, unless otherwise specified.

Memory Read & Write Cycle (Note 6)

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency		400	kHz
t_{SP}	Input Filter Spike Suppression (SDA, SCL)		100	ns
t_{LOW}	Clock Low Period	1.3		μs
t_{HIGH}	Clock High Period	0.6		μs
t_R (Note 5)	SDA and SCL Rise Time		300	ns
t_F (Note 5)	SDA and SCL Fall Time		300	ns
$t_{HD; STA}$	Start Condition Hold Time	0.6		μs
$t_{SU; STA}$	Start Condition Setup Time (for a Repeated Start)	0.6		μs
$t_{HD; DAT}$	Data Input Hold Time	0		ns
$t_{SU; DAT}$	Data Input Setup Time	100		ns
$t_{SU; STO}$	Stop Condition Setup Time	0.6		μs
t_{AA}	SCL Low to Data Out Valid		900	ns
t_{DH}	Data Out Hold Time	50		ns
t_{BUF} (Note 5)	Time the Bus must be Free Before a New Transmission Can Start	1.3		μs
t_{WC} (Note 7)	Write Cycle Time (Byte or Page)		5	ms

- This parameter is characterized initially and after a design or process change that affects the parameter. Not 100% tested.
- Test Conditions according to "AC Test Conditions" table.
- The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high and the device does not respond to its slave address.

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Table 9. RESET CIRCUIT AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PURST}	Power-Up Reset Timeout	Note 2	130	200	270	ms
t_{RDP}	V_{TH} to RESET output Delay	Note 3			5	μ s
t_{GLITCH}	V_{CC} Glitch Reject Pulse Width	Notes 4 and 5			30	ns
MR Glitch	Manual8.40659.8 137.h7munity	Note 1			100	ns
t_{MRW}	MR Pulse Width	Note 1	5			μ s
t_{MRD}	MR Input to RESET Output Delay	Note 1			1	μ s

Table 10. POWER-UP TIMING (Notes 5 and 6)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PUR}	Power-Up to Read Operation				270	ms
t_{PUW}	Power-Up to Write Operation				270	ms

Table 11. AC TEST CONDITIONS

Parameter	Test Conditions
Input Pulse Voltages	$0.2 \times V_{CC}$ to $0.8 \times V_{CC}$
Input Rise and Fall Times	10 ns
Input Reference Voltages	$0.3 \times V_{CC}$, $0.7 \times V_{CC}$
Output Reference Voltages	$0.5 \times V_{CC}$
Output Load	Current Source: $I_{OL} = 3 \text{ mA}$; $C_L = 100 \text{ pF}$

Table 12. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (Note 5)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR} (Note 5)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP} (Note 5)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH} (Notes 5 & 7)	Latch-Up	JEDEC Standard 17	100		mA

1. Test Conditions according to "AC Test Conditions" table.

Reset Controller Description

Hardware Data Protection

Manual Reset Operation

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EMBEDDED EEPROM OPERATON

Start Condition

I²C Bus Protocol

Stop Condition

DEVICE ADDRESSING

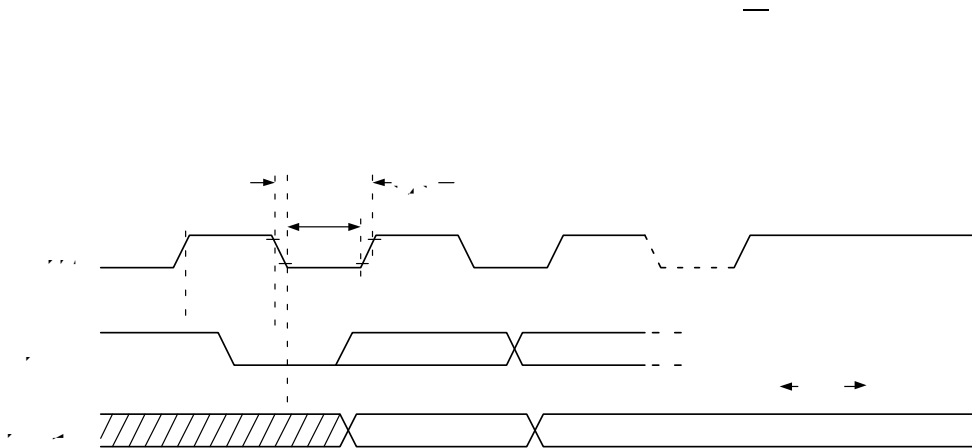


Figure 3. Bus Timing

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ACKNOWLEDGE

Page Write

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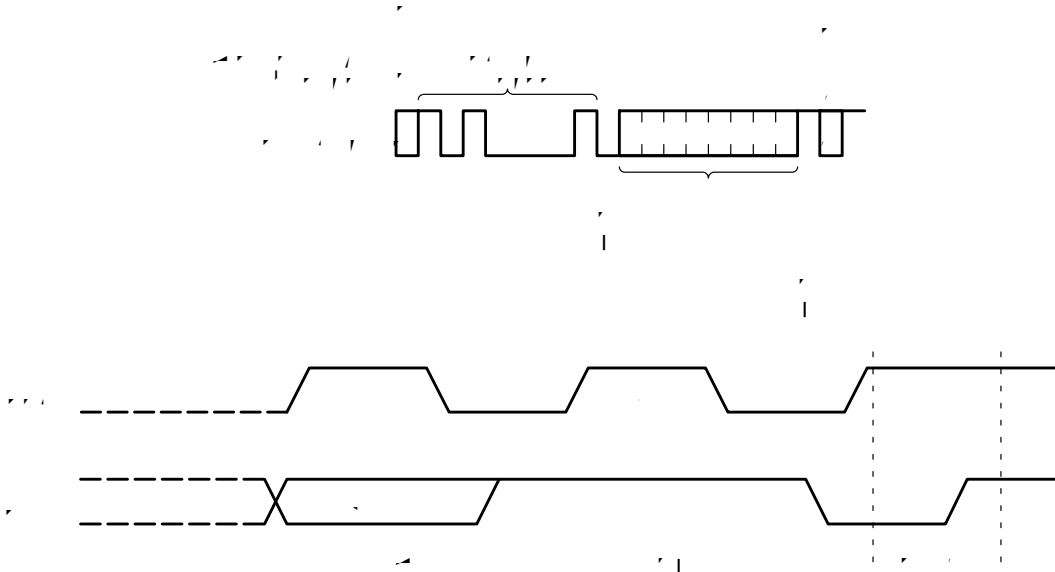


Figure 10. Immediate Address Read Timing

Immediate/Current Address Read

Sequential Read

Selective/Random Read

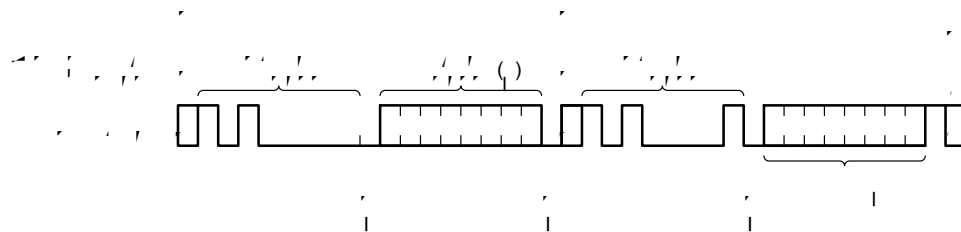


Figure 11. Selective Read Timing

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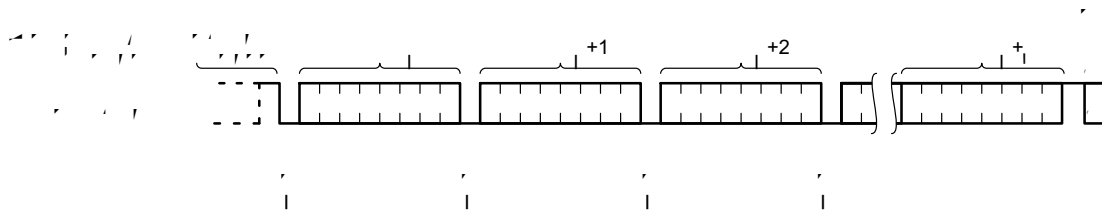


Figure 12. Sequential Read Timing

ORDERING INFORMATION

Orderable Part Numbers

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