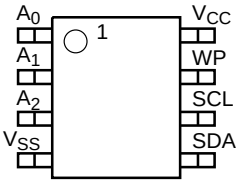
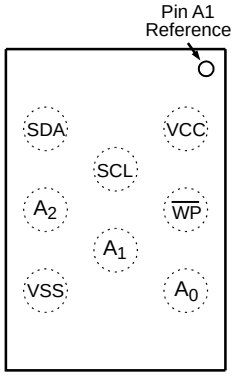
WLCSP−**8**
C8A SUFFIX
CASE 567JL

PIN CONFIGURATIONS



SOIC (W, X), TSSOP (Y),
UDFN (HU5)
(Top View)

For the location of
Pin 1, please consult
the corresponding
package drawing.



WLCSP (C8A)
(Top View)

- Industrial and Extended Temperature Range
- 8−pin, SOIC, TSSOP, 8−pad UDFN and 8−ball WLCSP Packages
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

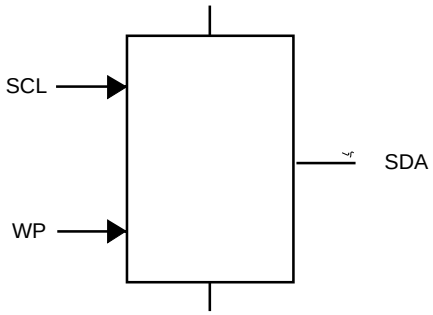
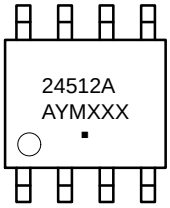


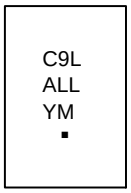
Figure 1. Functional Symbol

MARKING DIAGRAMS



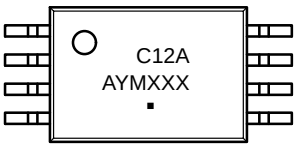
SOIC 8 (W, X)

24512A = Specific Device Code
A = Assembly Location Code
Y = Production Year (Last Digit)
M = Production Month (1 9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb Free Microdot



UDFN 8 (HU5)

C9L = Specific Device Code
A = Assembly Location Code
LL = Last Two Digits of Assembly Lot Number
Y = Production Year (Last Digit)
M = Production Month (1 9, O, N, D)
▪ = Pb Free Microdot



TSSOP 8 (Y)

C12A = Specific Device Code
A = Assembly Location Code
Y = Production Year (Last Digit)
M = Production Month (1 9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number
▪ = Pb Free Microdot

WLCSP (C8A)

C9A = Specific Device Code
A = Assembly Location
Y = Production Year
W = Production Week

Table 5. A.C. CHARACTERISTICS (Note 7)
V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.

Symbol	Parameter	Standard V_{CC} = 1.8 V − 5.5 V		Fast V_{CC} = 1.8 V − 5.5 V		Fast−Plus V_{CC} = 2.5 V − 5.5 V, T_A = −40°C to +85°C		Units
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6				

Power-On Reset (POR)

The CAT24C512 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi−directional POR behavior protects the device against brown−out failure, following a temporary loss of power.

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_0, A_1 and A_2: The Address pins accept the device address. These pins have on−chip pull−down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on−chip pull−down resistor.

Functional Description

The CAT24C512 supports the Inter−Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24C512 acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 8 devices may be connected to the bus as determined by the device address inputs A_0, A_1, and A_2.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the 2−wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 3 bits, A_2, A_1 and A_0, select one of 8 possible Slave devices. The last bit, R/W, specifies whether a Read (1) or Write (0) operation is to be performed.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

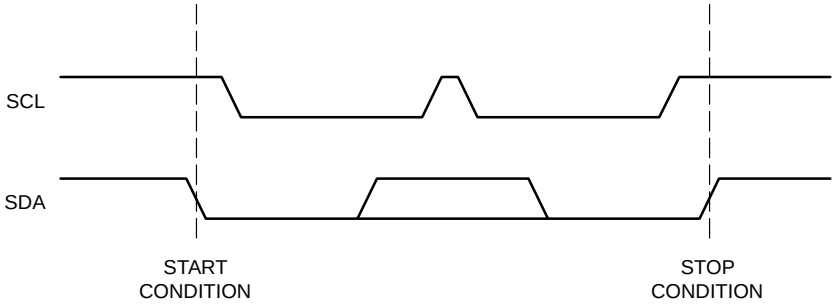


Figure 2. Start/Stop Timing

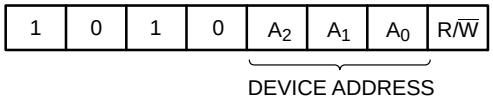


Figure 3. Slave Address Bits

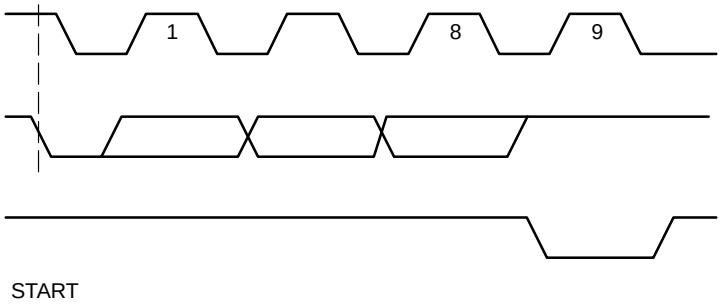


Figure 4. Acknowledge Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24C512 contains 65,536 bytes of data, arranged in 512 pages of 128 bytes each. A two byte address word, following the Slave address, points to the first byte to be written. The most significant 9 bits (A_{15} to A_7) identify the page and the last 7 bits identify the byte within the page. Up to 128 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 128 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap−around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

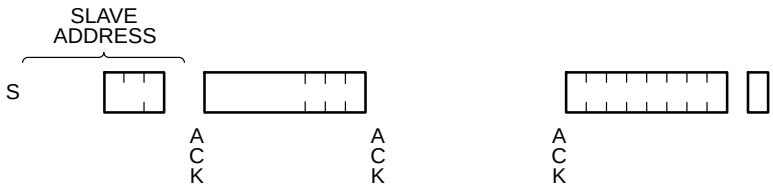
Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24C512 is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The CAT24C512 will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating


SLAVE
ADDRESS
S
ACK
ACK
ACK

READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24C512 internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that ‘previous’ byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24C512 is presented with a Slave address containing a ‘1’ in the R/W bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

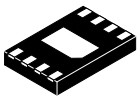
The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a ‘dummy’ Write operation (Figure 11). Here the START is followed by the Slave address (with the R/W bit set to ‘0’) and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the ‘Immediate Address Read’ sequence, as described earlier.

Sequential Read

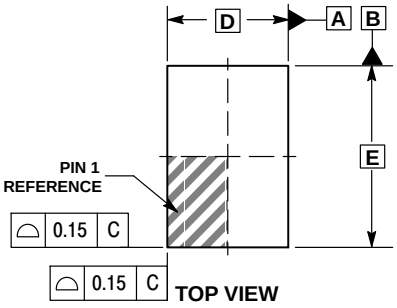
If the Master acknowledges the 1st data byte transmitted by the CAT24C512, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will ‘wrap−

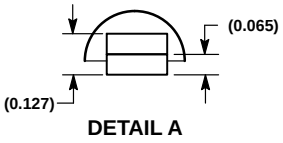
ORDERING INFORMATION (Notes 10, 11)

UDFN8 3.0x2.0, 0.5P

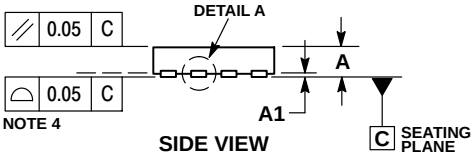


SCALE 4:1

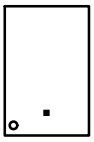


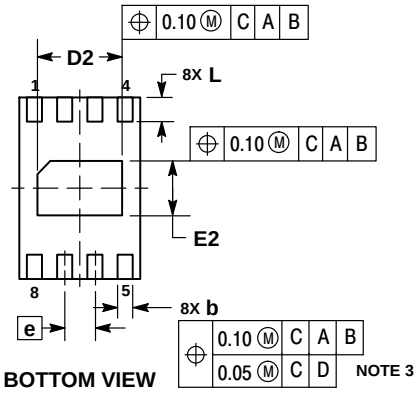


DIM	MILLIMETERS MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	0.85	0.95
e	0.50 BSC	
L	0.35	0.45

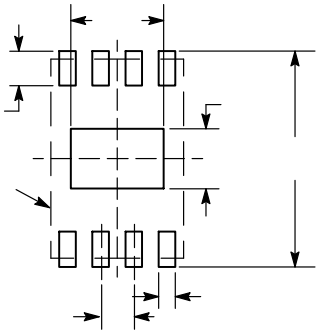


GENERIC MARKING DIAGRAM*





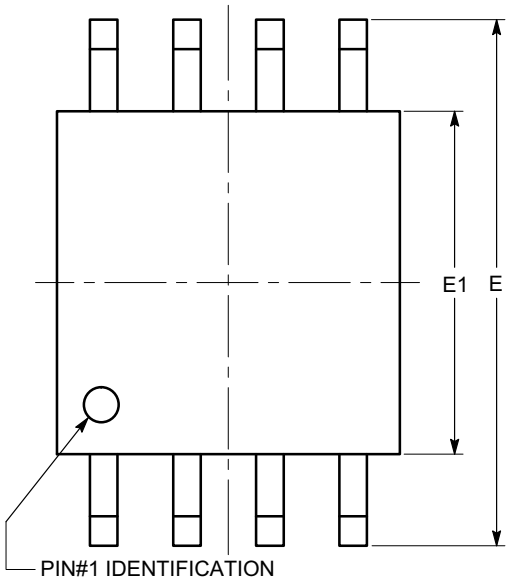
RECOMMENDED MOUNTING FOOTPRINT



DOCUMENT NUMBER:	**98AON55336E**
DESCRIPTION:	

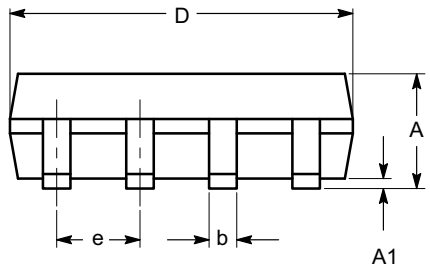
SOIC−8, 208 mils
CASE 751BE
ISSUE O

DATE 19 DEC 2008

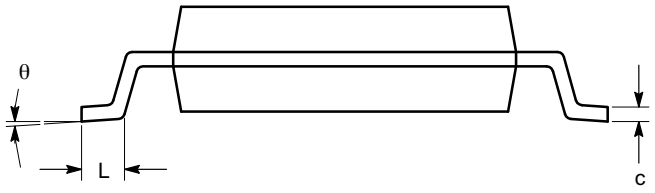


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			
A1	0.05		
b	0.36		
c	0.19		
D	5.13		
E			
E1			
e			
θ	0°		8°

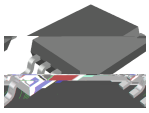


SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.



TSSOP8, 4.4x3.0, 0.65P
CASE 948AL
ISSUE A

DATE 20 MAY 2022

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSI_RS

TOP VIEW

	MILLIMETERS		
DIM	MIN.	NOM.	
A	---		1.20
A1	0.05		0.15
A2			
b	0.19		0.30
c			
D	2.90		3.10
E	6.3		
E1	4.30		4.50
e			
θ			