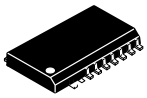
CAT310

LED Driver, 10-Channel

http://onsemi.com



SOIC−20
W SUFFIX
CASE 751BJ

Description

The CAT310 is a 10 channel LED driver for automotive and other lighting applications. All LED output channels are driven from a low on resistance open drain High Voltage CMOS Nch FETs and are fully compliant with “Load Dump” transients of up to 40 volts. The LED bias current of each channel can be set independently using an external series ballast resistor, making the device ideal for multi color instrumentation displays.

A high speed serial interface (suitable with both 3.3 volt and 5 volt systems) feeding a 10 bit shift register is used to program the desired state (on/off) of each channel. The device offers a blanking control pin (BLANK) which can be used to disable all channels on demand. A serial output data pin (SOUT) is provided to daisy chain devices in large cluster LED applications.

During initial power up all channels are reset and cleared via an under voltage lock out (UVLO) detector and for added protection all channels are disabled in the event of a battery over voltage condition (19 volts or more).

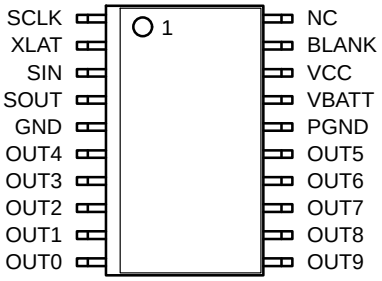
Features

- Automotive “Load Dump” Protection (40 V)
- 10 Independent LED Channels
- Up to 50 mA Output per Channel
- Overvoltage Detection at 19 V
- Serial Interface for Channel Programming
- Daisy Chain Output for Multi driver Cascading
- LED Blanking Control
- Operating Temperature from 40°C to +125°C
- 20 pin SOIC Package
- This Device is Pb Free, Halogen Free/BFR Free and RoHS Compliant

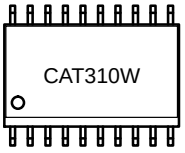
Applications

- Automotive Lighting
- White and Other Color High Brightness LEDs
- Multi color High brightness LED Cluster Displays
- General LED Lighting

PIN CONNECTIONS



MARKING DIAGRAM



CAT310W = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
CAT310W	SOIC−20 (Pb−Free)	1,000/Tape & Reel

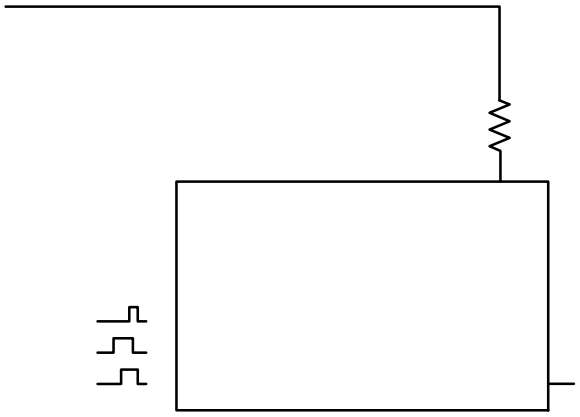


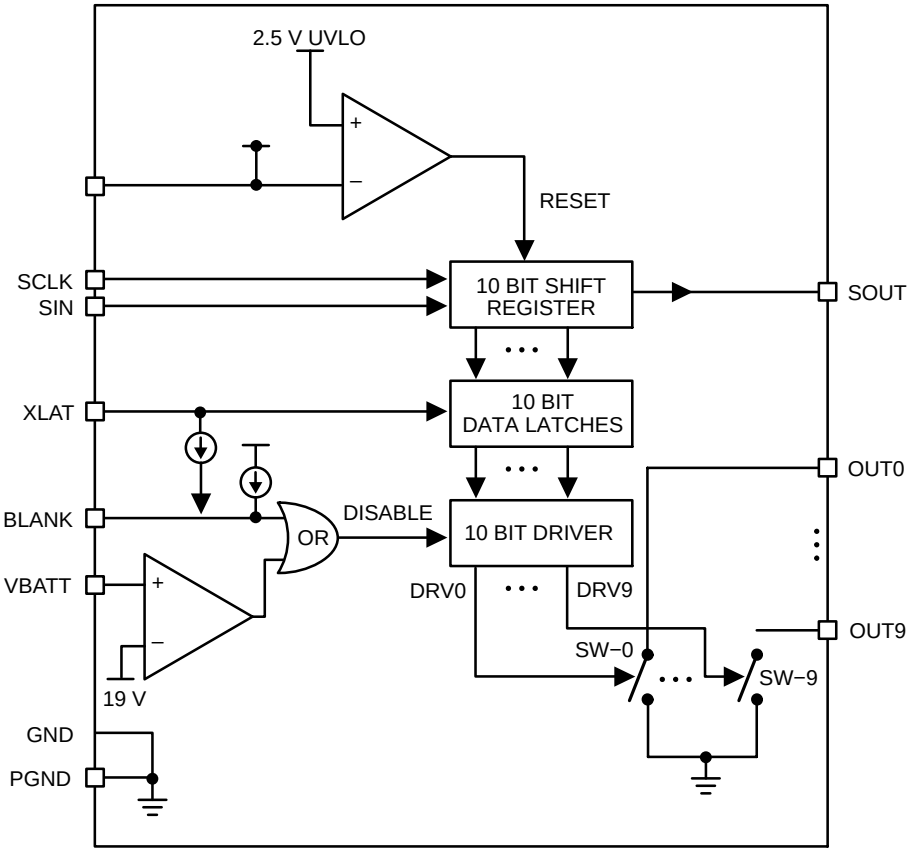
Figure 1. Typical Application Circuit

Electrical Operating Characteristics

Table 3. DC CHARACTERISTICS

(VCC = 5.0 V, −40°C ≤ T_A ≤ 125°C, over recommended operating conditions unless specified otherwise.)

Symbol	Name	Conditions	Min	Typ	Max	Units
I_{STBY}						


2.5 V UVLO
+
–
RESET
SCLK
SIN
10 BIT SHIFT REGISTER
SOUT
XLAT
10 BIT DATA LATCHES
OUT0
BLANK
OR
DISABLE
10 BIT DRIVER
VBATT
DRV0
DRV9
OUT9
SW−0
SW−9
19 V
GND
PGND

PIN DESCRIPTIONS

VCC is the supply input for the internal logic and is compatible with both 3.3 V and 5 V systems. The logic is held in a reset state until VCC exceeds 2.5 V. It is recommended that a small bypass ceramic capacitor (1 μF) be placed between VCC and GND pins on the device.

SIN is the CMOS logic pin for delivering the serial input data stream into the internal 10 bit shift register. The most recent or last data value in the serial stream is used to configure the state of output channel “zero” (OUT0). During the initial power up sequence all contents of the shift register are reset and cleared to zero.

SCLK is the CMOS logic pin used to clock the internal shift register. On each rising edge of clock, the serial data will advance through one stage of the shift register.

XLAT is the CMOS logic input used to transfer data from the 10

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TYPICAL CHARACTERISTICS

(VCC = 5 V, VBATT = 14 V, T_{AMB} = 25°C, unless otherwise specified.)

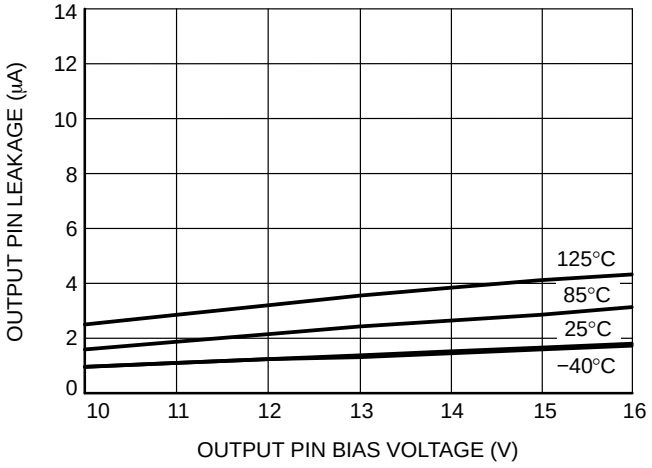

Figure 9. Output Channel Leakage vs. Bias Voltage

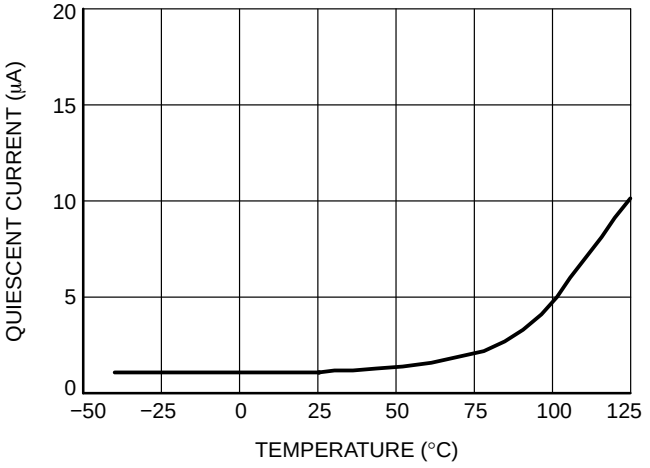

Figure 10. Quiescent Current vs. Temperature

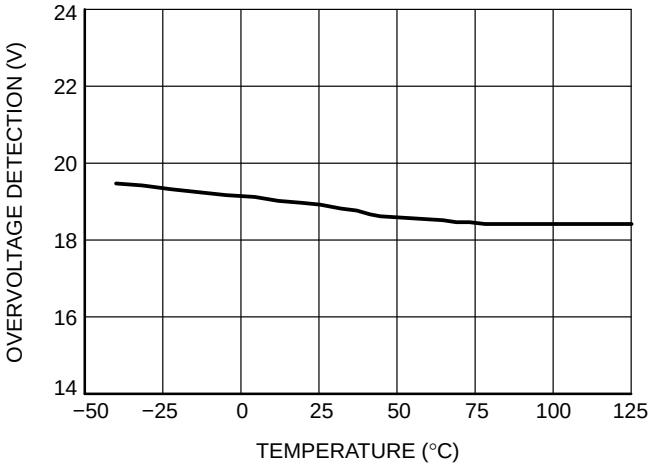

Figure 11. VBATT Overvoltage Detection vs. Temperature

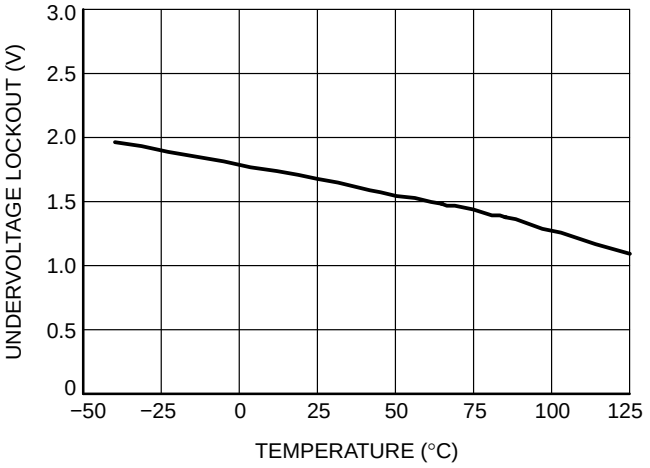

Figure 12. VCC Undervoltage Lockout vs. Temperature

Functional Description

The CAT310 implements a 10 bit serial in shift register for storing the setting of the ten outputs. Serial input data SIN are clocked into the shift register on the rising edge of the clock. At the 10th clock pulse, the first data bit entered is outputted from the shift register to SOUT. The following clock pulses will output the following data bits onto SOUT. The output data pattern replicates the input data stream with a delay of ten clock pulses.

The 10 bit data pattern present in the shift register is stored in the 10 bit data latch when the latch signal XLAT is logic high. When XLAT transitions to logic low, data are

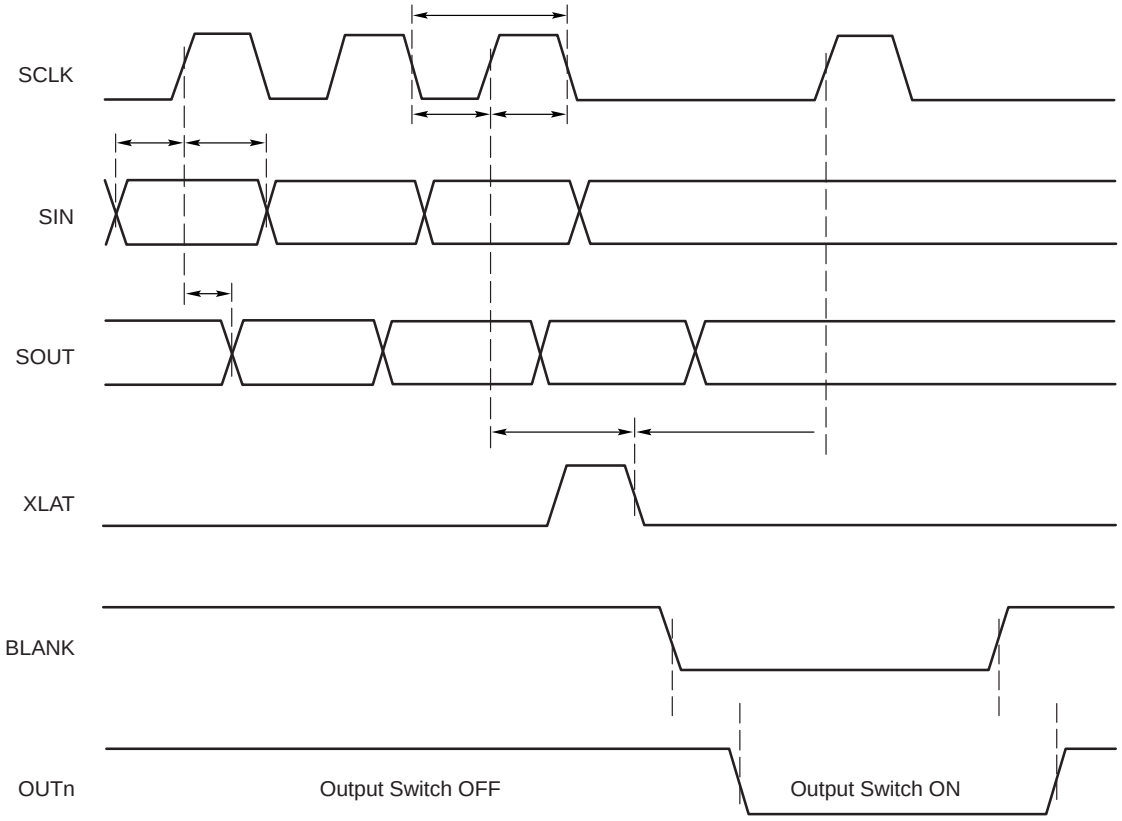

Figure 13. Timing Diagram

CAT310

Example of Ordering Information

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