Table 4. A.C. CHARACTERISTICS (V_{CC} = 1.7 V to 1.9 V, T_A = −20°C to +125°C)

Symbol	Parameter	100 kHz		400 kHz		Units
		Min	Max	Min	Max	
F_{SCL} (Note 5)	Clock Frequency	10	100	10	400	kHz
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
$t_{TIMEOUT}$ (Note 6)	SMBus SCL Clock Low Timeout	25	35	25	35	ms
t_R (Note 7)	SDA and SCL Rise Time		1000			

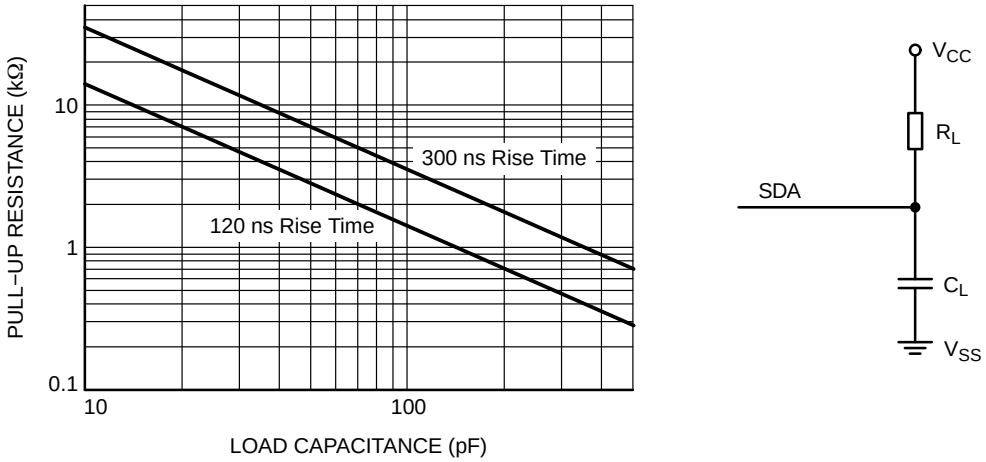


Figure 2. Pull−up Resistance vs. Load Capacitance

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the TS registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins accept the device address. These pins have on chip pull down resistors.

$\overline{\text{EVENT}}$: The open drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset (POR)

The CAT34TS00 incorporates Power On Reset (POR) circuitry which protects the device against powering up to an undetermined logic state. As V_{CC} exceeds the POR trigger level, the device will power up into conversion mode. When V_{CC} drops below the POR trigger level, the device will power down into Reset mode.

This bi directional POR behavior protects CAT34TS00 against brown out failure following a temporary loss of power. The POR trigger level is set below the minimum operating V_{CC} level.

Device Interface

The CAT34TS00 supports the Inter Integrated Circuit (I^2C) and the System Management Bus (SMBus) data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2 wire data bus. Data ow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT34TS00 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT34TS00 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2. The CAT34TS00 contains eight 16

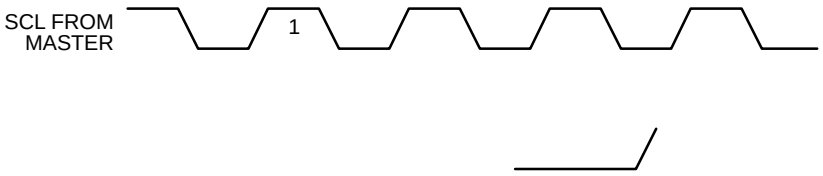


Figure 4. Acknowledge Timing

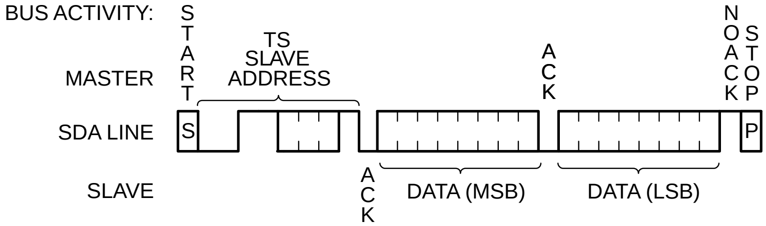


Figure 7. Temperature Sensor Immediate Read

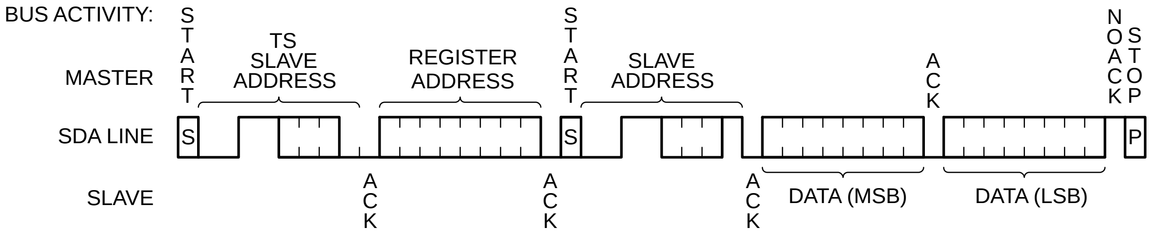


Figure 8. Temperature Sensor Selective Read

Temperature Sensor Operation

The TS component in the CAT34TS00 combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ Δ modulator, yielding a 12 bit plus sign digital temperature representation. The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to

[illegible]

[illegible]

[illegible]

Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI SIG trade organization to the CAT34TS00 device is fixed at 0x1B09.

Device ID and Revision Register (Read Only)

This register contains specific device ID and device revision information.

Table 7. THE TEMPERATURE SENSOR REGISTERS

Register Address	Register Name	Power−On Default	Read/Write
0x00	Capability Register	0x0077	Read
0x01	Configuration Register	0x0000	Read/Write
0x02	High Limit Register	0x0000	Read/Write
0x03	Low Limit Register	0x0000	Read/Write
0x04	Critical Limit Register	0x0000	Read/Write
0x05	Temperature Data Register	Undefined	Read
0x06	Manufacturer ID Register	0x1B09	Read
0x07			

Table 9. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TCRIT_LOCK	ALARM_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Bit	Description
B15:B11	

Table 10. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12 bit resolution, while the 3 trip temperature limits are set with 10 bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the "don't care" bits (B1 and B0) in the 10 bit resolution temperature limit registers, are always '0'.

Table 14. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 9, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the (enabled) $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de asserted by writing a '1' to the clear event bit (B5) in the configuration register. Once the temperature exceeds the critical limit, the $\overline{\text{EVENT}}$ remains asserted as long as the temperature stays above the critical limit and cannot be cleared. A clear request sent to the CAT34TS00 while the temperature is above the critical limit will be acknowledged, but will be executed only after the temperature drops below the critical limit.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. Clear requests are ignored in this mode. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 10.

Following a TS shut down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT34TS00 is 71962 TD0 37 Tc9.402 427.6

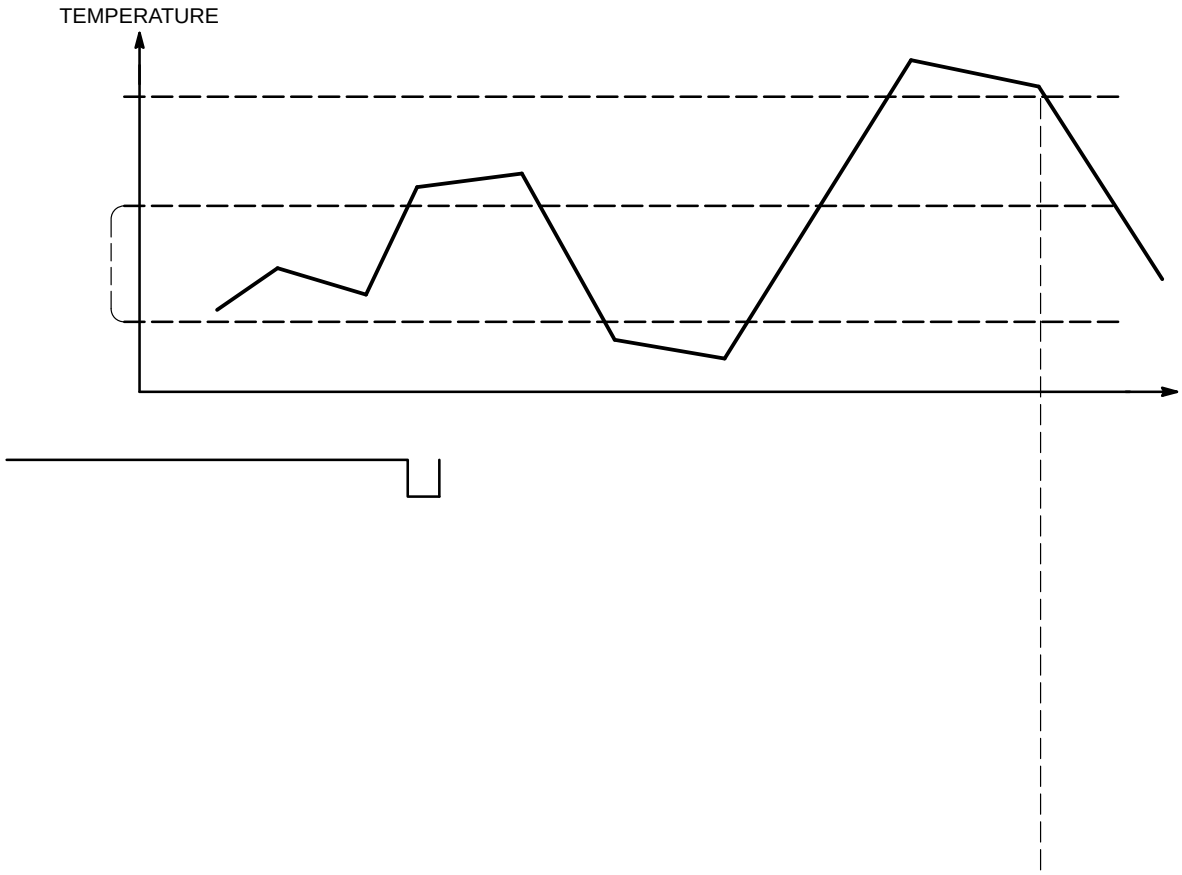


Figure 9. Event Detail

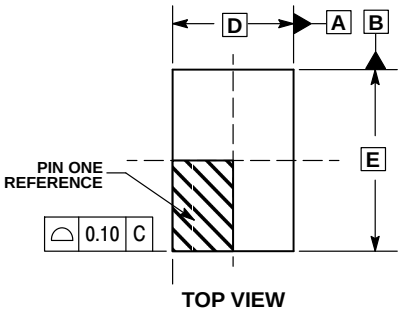
Example of Ordering Information

Device Order Number	Specific Device Marking	Package Type	Shipping†
CAT34TS00VP2GT4A			

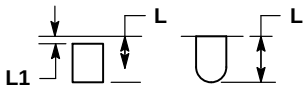
TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

SCALE 2:1

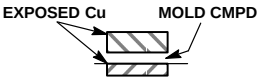
DATE 18 MAR 2015



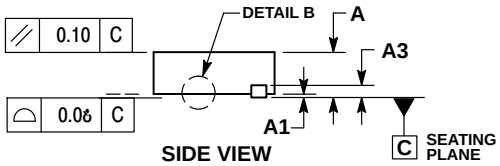
TOP VIEW



DETAIL A
ALTERNATE
CONSTRUCTIONS



DETAIL B
ALTERNATE
CONSTRUCTION

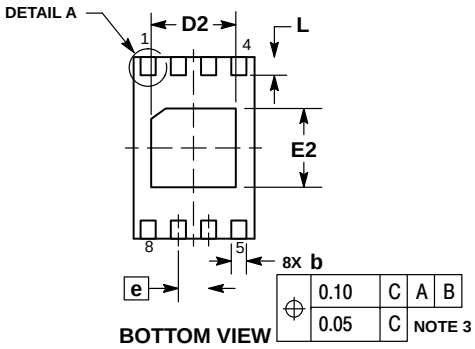


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.20	1.40
e	0.50 BSC	
L	0.20	0.40
L1	–––	0.15

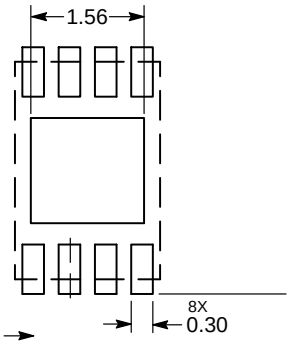
GENERIC
MARKING DIAGRAM*



BOTTOM VIEW

XXXXX = Specific Device Code

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.