# CAT34TS02

# Digital Output Temperature Sensor with On-board SPD EEPROM

**Description**

The CAT34TS02 combines a JC42.4 compliant Temperature Sensor (TS) with 2−Kb of Serial Presence Detect (SPD) EEPROM.

The TS measures temperature at least 10 times every second. Temperature readings can be retrieved by the host via the serial interface, and are compared to high, low and critical trigger limits



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CAT34TS02/D

**Table 1. ABSOLUTE MAXIMUM RATINGS**

| Parameter | Rating | Units |
|---|---|---|
| Operating Temperature | −45 to +130 | °C |
| Storage Temperature | −65 to +150 | °C |
| Voltage on any pin (except $A_0$) with respect to Ground (Note 1) | −0.5 to +6.5 | V |
| Voltage on pin $A_0$ with respect to Ground | −0.5 to +10.5 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{CC}$ = 3.3 V, $T_A$ = −20°C to +125°C, unless otherwise specified.)

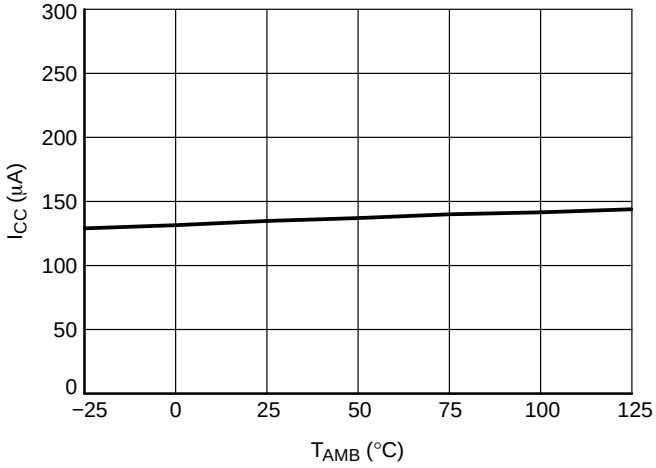



**Figure 2. TS Active Current (Rev. B) (I²C−bus and SPD EEPROM Idle)**

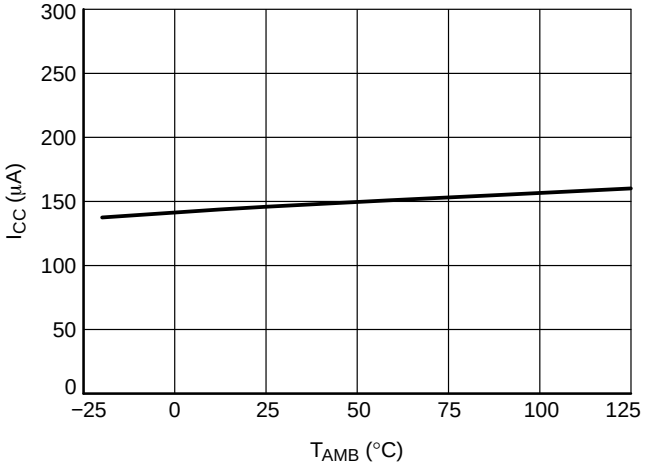



**Figure 3. TS Active Current (Rev. C) (I²C−bus and SPD EEPROM Idle)**

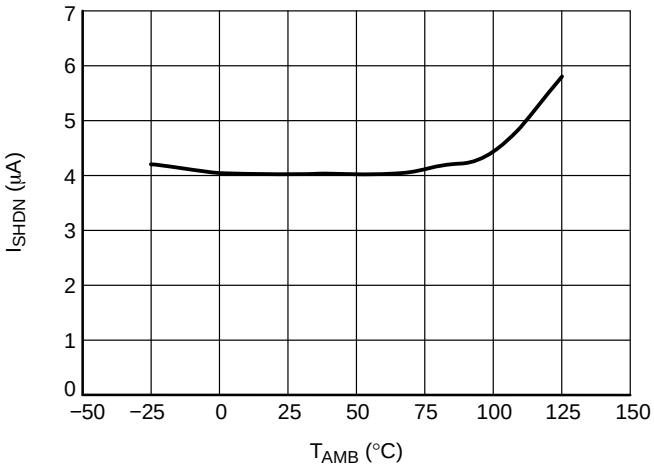



**Figure 4. Standby Current (Rev. B) (I²C−bus and SPD EEPROM Idle, TS Shut−down)**

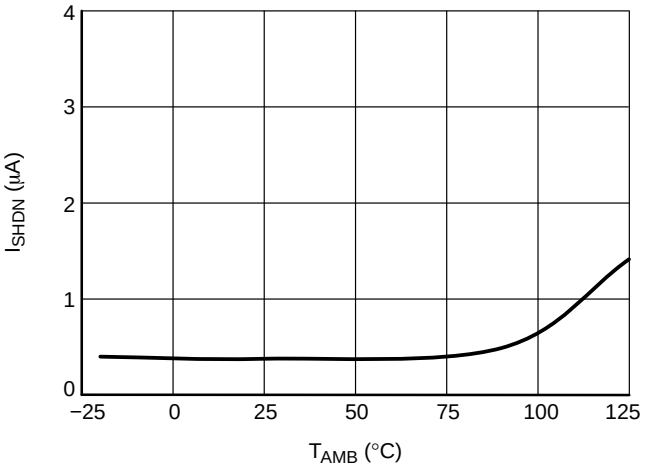



**Figure 5. Standby Current (Rev. C) (I²C−bus and SPD EEPROM Idle, TS Shut−down)**

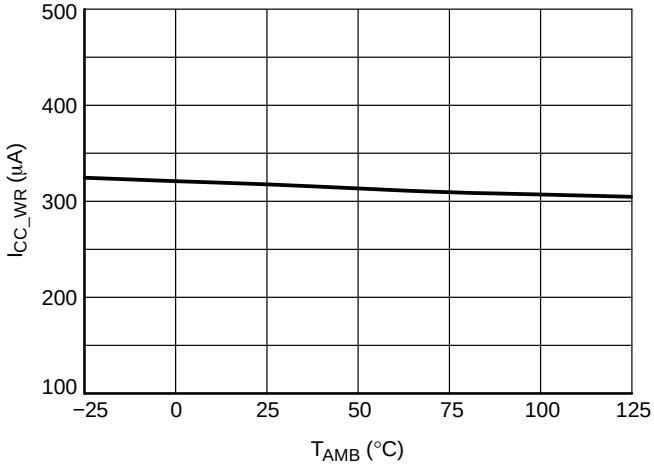



**Figure 6. SPD EEPROM Write Current (Rev. B) (I²C−bus Idle, TS Shut−down)**

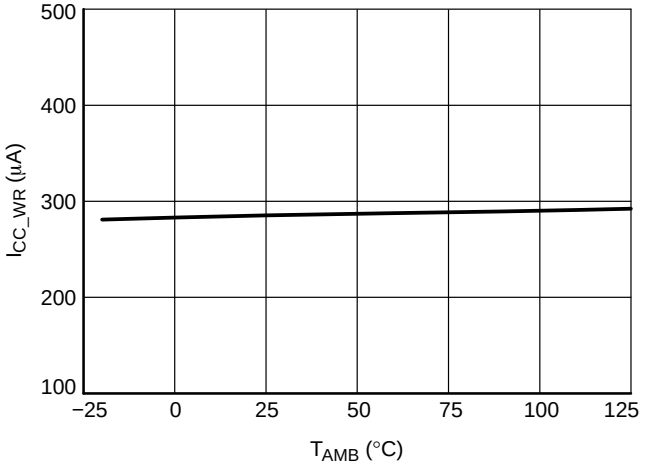



**Figure 7. SPD EEPROM Write Current (Rev. C) (I²C−bus Idle, TS Shut−down)**

## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{CC}$ = 3.3 V, $T_A$ = −20°C to +125°C, unless otherwise specified.)

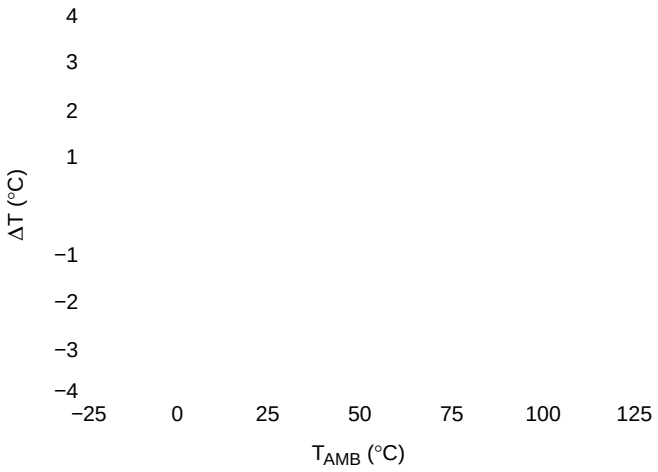
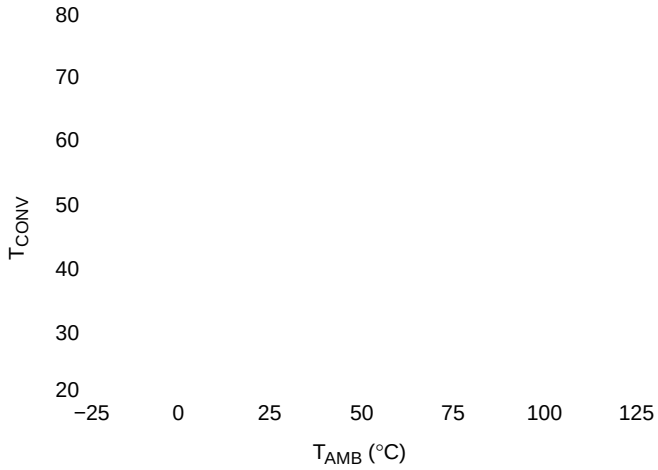
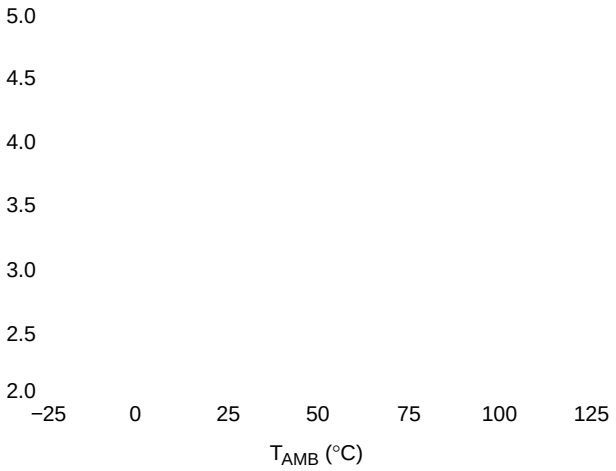



**Figure 8. Temperature Read−Out Error (Rev. B)**



### Pin Description

**SCL:** The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

**SDA:** The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

**A0, A1 and A2:** The Address pins accept the device address. These pins have on−chip pull−down resistors.

**$\overline{\text{EVENT}}$:** The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

### Power−On Reset (POR)

The CAT34TS02 incorporates Power−On Reset (POR) circuitry which protects the device against powering up to invalid state. The TS component will power up into conversion mode after $V_{CC}$ exceeds the TS POR trigger level and the SPD component will power up into standby mode after $V_{CC}$ exceeds the SPD POR trigger level. Both the TS and SPD components will power down into Reset mode when $V_{CC}$ drops below their respective POR trigger levels. This bi−directional POR behavior protects the CAT34TS02 against brown−out failure following a temporary loss of power. The POR trigger levels are set below the minimum operating $V_{CC}$ level.

### Device Interface

The CAT34TS02 supports the Inter−Integrated Circuit ($I^2$

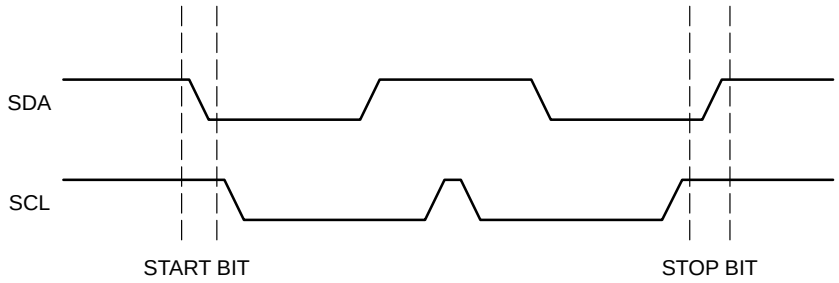



**Figure 20. Start/Stop Timing**

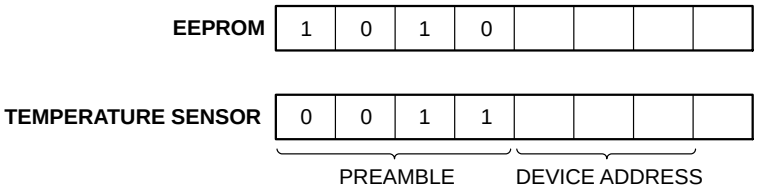



**Figure 21. Slave Address Bits**

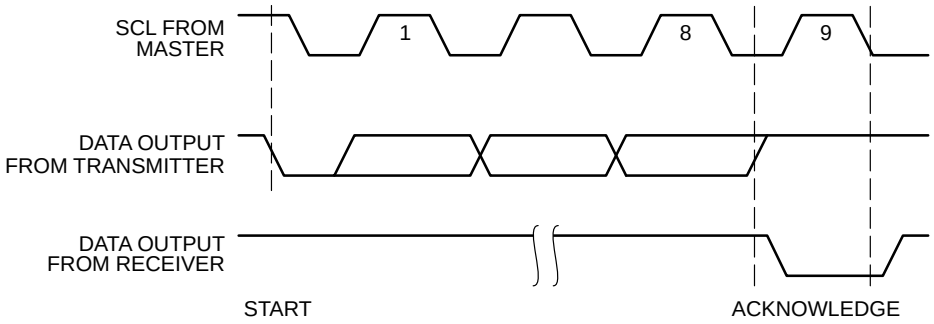
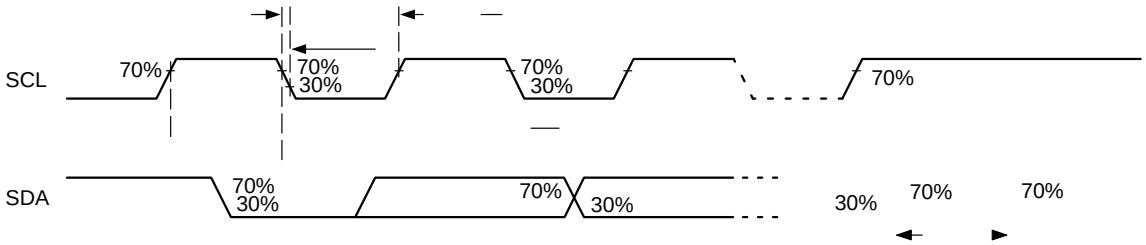



**Figure 22. Acknowledge Timing**



## Write Operations

### EEPROM Byte and TS Register Write

To write data to a TS register, or to the on−board EEPROM, the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to ‘0’), followed by an address byte and data byte(s). The matching Slave will acknowledge the Slave address, EEPROM byte address or TS register address and the data byte(s), one for EEPROM data (Figure 24) and two for TS register data (Figure 25). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the (volatile) TS register update or starts the internal Write cycle for the (non−volatile) EEPROM data (Figure 26).

### EEPROM Page Write

The on−board EEPROM contains 256 bytes of data, arranged in 16 pages of 16 bytes each. A page is selected by the 4 most significant bits of the address byte immediately following the Slave address, while the 4 least significant bits point to the byte within the page. Up to 16 bytes can be written in one Write cycle (Figure 27).

The internal EEPROM byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 16 data bytes, then earlier data will be overwritten by later data in a ‘wrap−around’ fashion within the selected page. The internal Write cycle, using the most recently loaded data, then starts immediately following the STOP.

### Acknowledge Polling

Acknowledge polling can be used to determine if the CAT34TS02 is busy writing to EEPROM, or is ready to accept commands. Polling is executed by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS). The CAT34TS02 will not acknowledge the Slave address as long as internal EEPROM Write is in progress.

## Delivery State

The CAT34TS02 is shipped ‘unprotected’, i.e. neither Software Write Protection (SWP) flag is set. The entire 2−Kb memory is erased, i.e. all bytes are 0xFF.

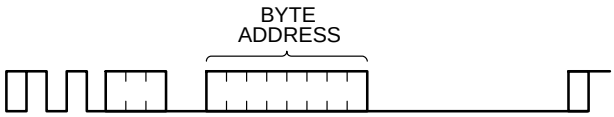
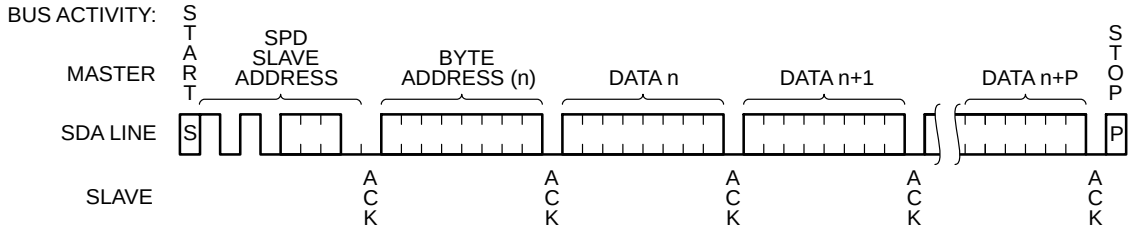



**Figure 24. EEPROM Byte Write**




NOTE: In this example n = XXXX 0000(B); X = 1 or 0

**Figure 27. EEPROM Page Write**

## Read Operations

### Immediate Read

Upon power−up, the address counters for both the Temperature Sensor (TS) and on−board EEPROM are initialized to 00h. The TS address counter will thus point to the Capability Register and the EEPROM address counter will point to the first location in memory. The two address counters may be upd536.4(-.085 -. .1( may9425 TD(rteequeon o.8788sor T41 Tw[(T)6ized[(the8zed)8.2( )]TA)0016.0014dreC014dreA)1

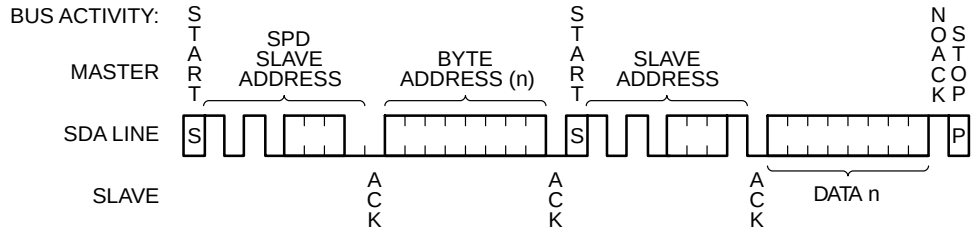



**Figure 29a. EEPROM Selective Read**

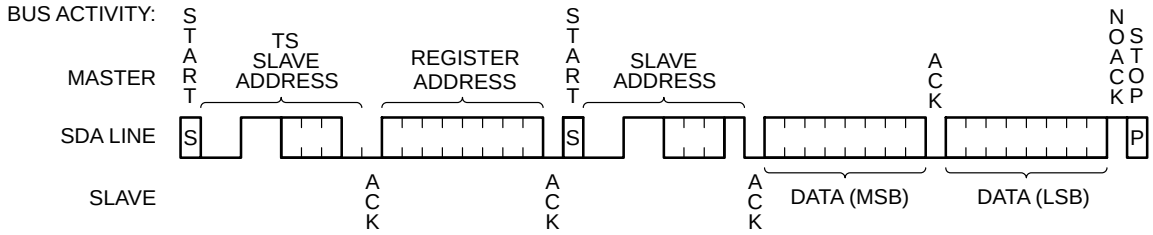



**Figure 29b. Temperature Sensor Selective Read**

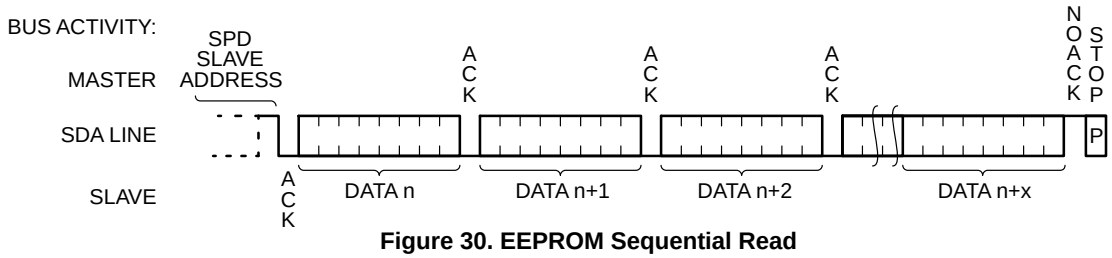



**Figure 30. EEPROM Sequential Read**

### Software Write Protection

The lower half of memory (first 128 bytes) can be protected against Write requests by setting one of two Software Write Protection (SWP) flags.

The Permanent Software Write Protection (PSWP) flag can be set or read while all address pins are at regular CMOS levels (GND or $V_{CC}$), whereas the very high voltage $V_{HV}$ must be present on address pin A0 to set, clear or read the Reversible Software Write Protection (RSWP) flag. The D.C. OPERATING CONDITIONS for RSWP operations are shown in Table 7.

The SWP commands are listed in Table 8. All commands are preceded by a START and terminated with a STOP, following the ACK or NoACK from the CAT34TS02. All SWP related Slave addresses use the pre−amble: 0110 (6h), instead of the regular 1010 (Ah) used for memory access. For **PSWP** commands, the three address pins can be at any logic level, whereas for **RSWP** commands the address pins must be at pre−assigned logic levels.

**$V_{HV}$ is interpreted as logic ‘1’. The $V_{HV}$ condition must be established on pin A0 before the START and maintained just beyond the STOP. Otherwise an RSWP request could be interpreted by the CAT34TS02 as a PSWP request.**

The SWP Slave addresses follow the standard $I^2C$ convention, i.e. to read the state of the SWP flag, the LSB of the Slave address must be ‘1’, and to set or clear a flag, it must be ‘0’. For Write commands a dummy byte address and dummy data byte must be provided (Figure 31). In contrast to a regular memory Read, a SWP Read does not return data. Instead the CAT34TS02 will respond with NoACK if the flag is set and with ACK if the flag is not set. Therefore, the Master can immediately follow up with a STOP, as there is no meaningful data following the ACK interval (Figure 32).

**Table 7. RSWP D.C. OPERATION CONDITION**

| Symbol | Parameter | Test Conditions | Min | Max | Units |
|---|---|---|---|---|---|

## Temperature Sensor Operation

The TS component in the CAT34TS02 combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ−Δ modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

## Registers

The CAT34TS02 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 9. Upon power−up, the internal address counter points to the capability register.

### Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

### Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

### Temperature Trip Point Registers (Read/Write)

The CAT34TS02 features 3 temperature limit registers,

# CAT34TS02

**Table 11. CONFIGURATION REGISTER**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|---|---|---|---|---|---|---|---|
| RFU | RFU | RFU | RFU | RFU | HYST [1:0] | | SHDN |
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| TCRIT_LOCK | EVENT_LOCK | CLEAR | EVENT_STS | EVENT_CTRL | TCRIT_ONLY | EVENT_POL | EVENT_MODE |

| Bit | Description |
|---|---|
| **B15:B11** | Reserved for future use; can not be written; should be ignored; will read as 0 |
| **B10:B9** (Note 14) | 00: Disable hysteresis<br>01: Set hysteresis at 1.5°C<br>10: Set hysteresis at 3°C<br>11: Set hysteresis at 6°C |
| **B8** (Note 18) | 0: Thermal Sensor is enabled; temperature readings are updated at sampling rate<br>1: Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN |
| **B7** (Note 17) | 0: Critical trip register can be updated<br>1: Critical trip register cannot be modified; this bit can be cleared only at POR |
| **B6** (Note 17) | 0: Alarm trip registers can be updated<br>1: Alarm trip registers cannot be modified; this bit can be cleared only at POR |
| **B5** (Note 16) | 0: Always reads as 0 (self−clearing)<br>1: Writing a 1 to this position clears an event recording in interrupt mode only |
| **B4** (Note 15) | 0: EVENT output pin is not being asserted<br>1: EVENT output pin is being asserted |
| **B3** (Note 14) | 0: EVENT output disabled; *polarity dependent*: open−drain for **B1** = 0; grounded for **B1** = 1<br>1: EVENT output enabled |
| **B2** (Note 20) | 0: event condition triggered by alarm or critical temperature limit crossing<br>1: event condition triggered by critical temperature limit crossing only |
| **B1** (Notes 14, 19) | 0: EVENT output active low<br>1: EVENT output active high |
| **B0** (Note 14) | 0: Comparator mode<br>1: Interrupt mode |

14. Can not be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.
15. This bit is a *polarity independent* ‘software’ copy of the $\overline{\text{EVENT}}$ pin, i.e. it is under the control of B3. This bit is read−only.
16. Writing a ‘1’ to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 33).
17. Cleared at power-on reset (POR). Once set, this bit can only be cleared by a POR condition.
18. The TS powers up into active mode, i.e. this bit is cleared at power-on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS can not be shut down (B8 can not be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.
19. The $\overline{\text{EVENT}}$ output is “open-drain” and requires an external pull-up resistor for either polarity. The “natural” polarity is “active low”, as it allows “wired-or” operation on the EVENT bus.
20. Can not be set as long as lock bit B6 is set.

**Table 12. HIGH LIMIT REGISTER**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Sign | 128°C | 64°C | 32°C | 16°C |
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 8°C | 4°C | 2°C | 1°C | 0.5°C | 0.25°C | 0 | 0 |

**Table 13. LOW LIMIT REGISTER**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Sign | 128°C | 64°C | 32°C | 16°C |
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 8°C | 4°C | 2°C | 1°C | 0.5°C | 0.25°C | 0 | 0 |

**Table 14. TCRIT LIMIT REGISTER**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | Sign | 128°C | 64°C | 32°C | 16°C |
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 8°C | 4°C | 2°C | 1°C | 0.5°C | 0.25°C | 0 | 0 |

**Table 15. TEMPERATURE DATA REGISTER**

| B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
|---|---|---|---|---|---|---|---|
| TCRIT | HIGH | LOW | Sign | 128°C | 64°C | 32°C | 16°C |
| **B7** | **B6** | **B5** | **B4** | **B3** | **B2** | **B1** | **B0** |
| 8°C | 4°C | 2°C | 1°C | 0.5°C | 0.25°C | | |

### Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

**Table 16. 12−BIT TEMPERATURE DATA FORMAT**

| Binary (B12 to B0) | Hex | Temperature |
|---|---|---|
| 1 1100 1001 0000 | 1C90 | −55°C |
| 1 1100 1110 0000 | 1CE0 | −50°C |
| 1 1110 0111 0000 | 1E70 | |

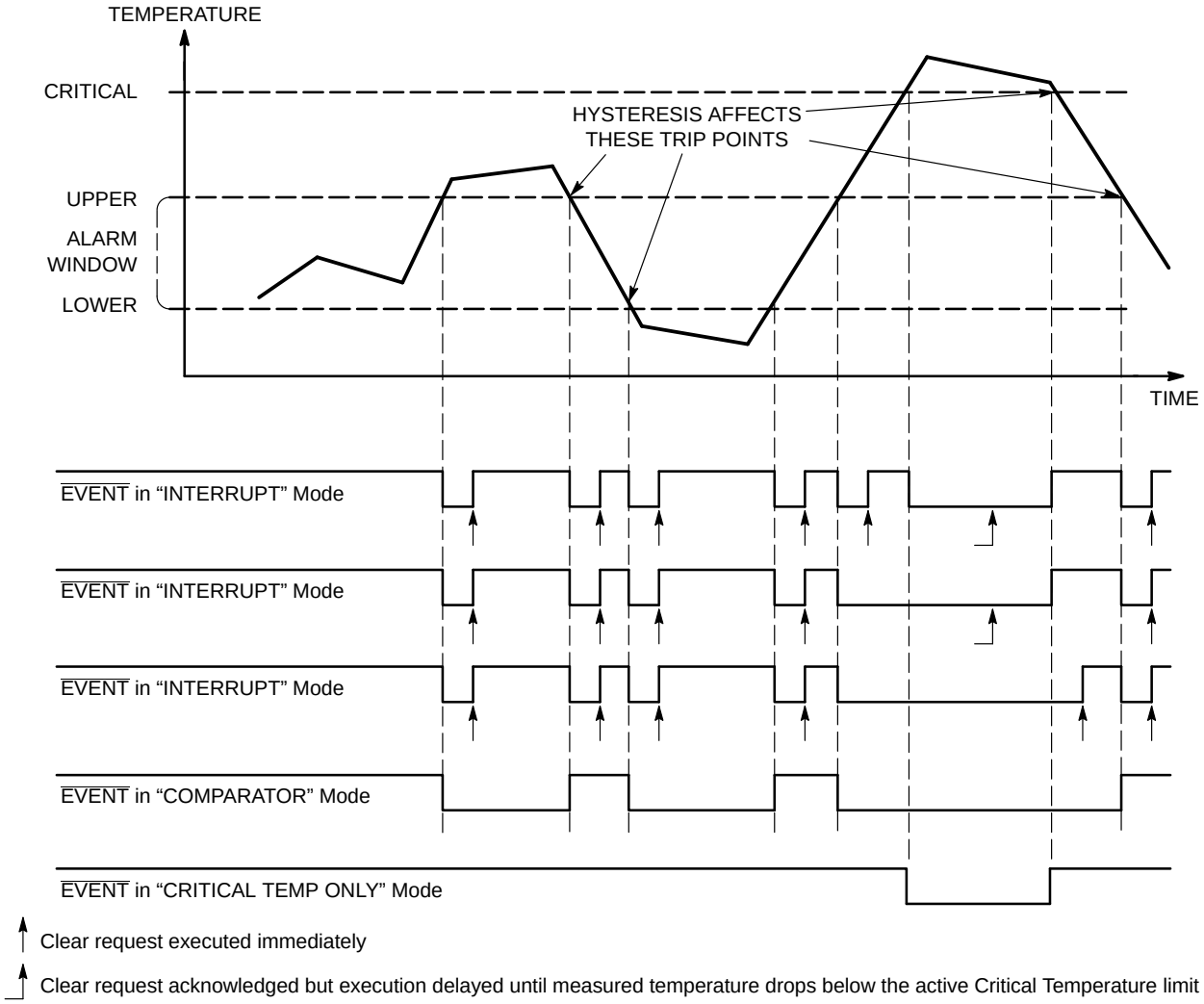



**Figure 33. Event Detail**

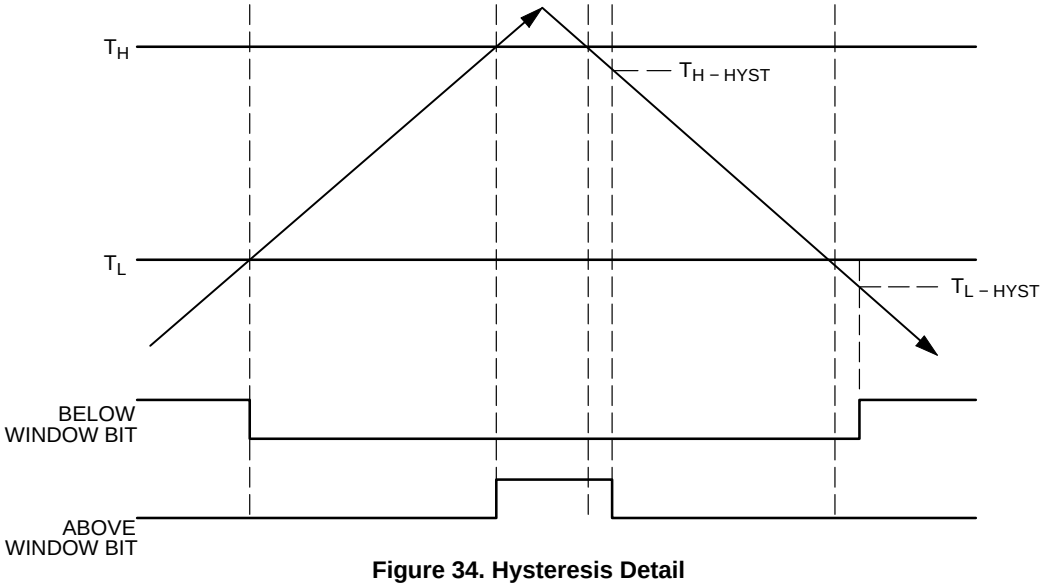
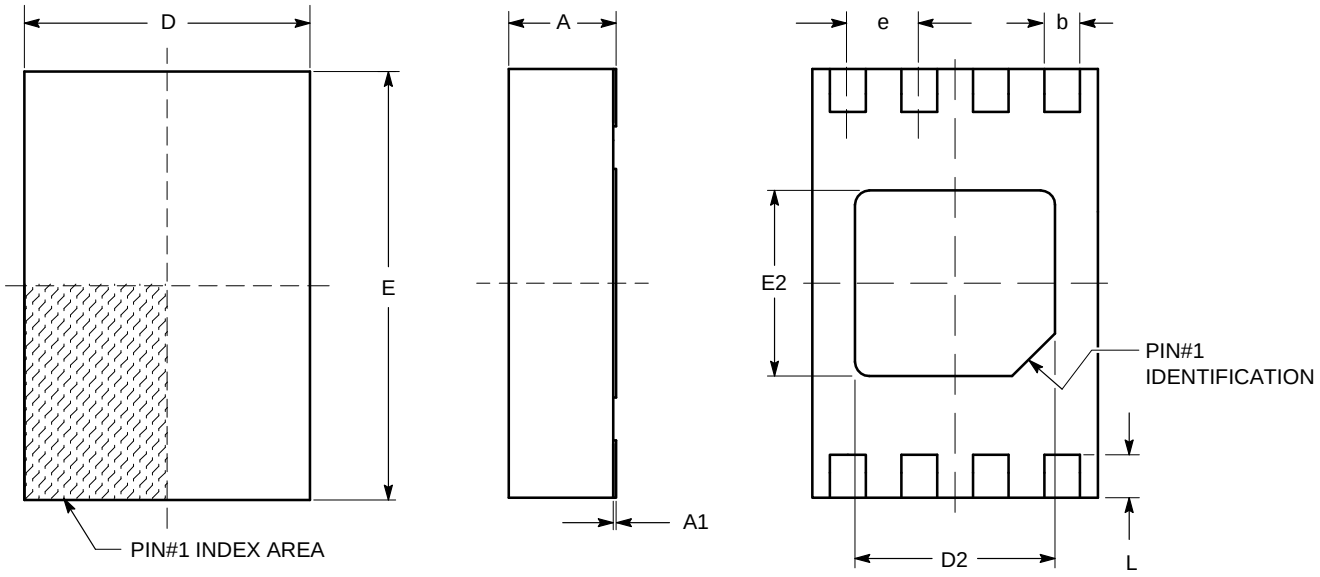



**Figure 34. Hysteresis Detail**

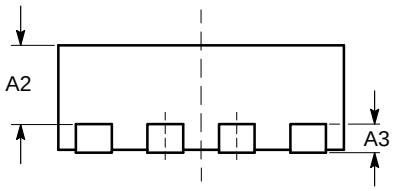
## PACKAGE DIMENSIONS

**TDFN8, 2x3**
CASE 511AK
ISSUE A




**TOP VIEW** **SIDE VIEW** **BOTTOM VIEW**

| SYMBOL | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A2 | 0.45 | 0.55 | 0.65 |
| A3 | | 0.20 REF | |
| b | 0.20 | 0.25 | 0.30 |
| D | 1.90 | 2.00 | 2.10 |
| D2 | 1.30 | 1.40 | 1.50 |
| E | 2.90 | 3.00 | 3.10 |
| E2 | 1.20 | 1.30 | 1.40 |
| e | | 0.50 TYP | |
| L | 0.20 | 0.30 | 0.40 |

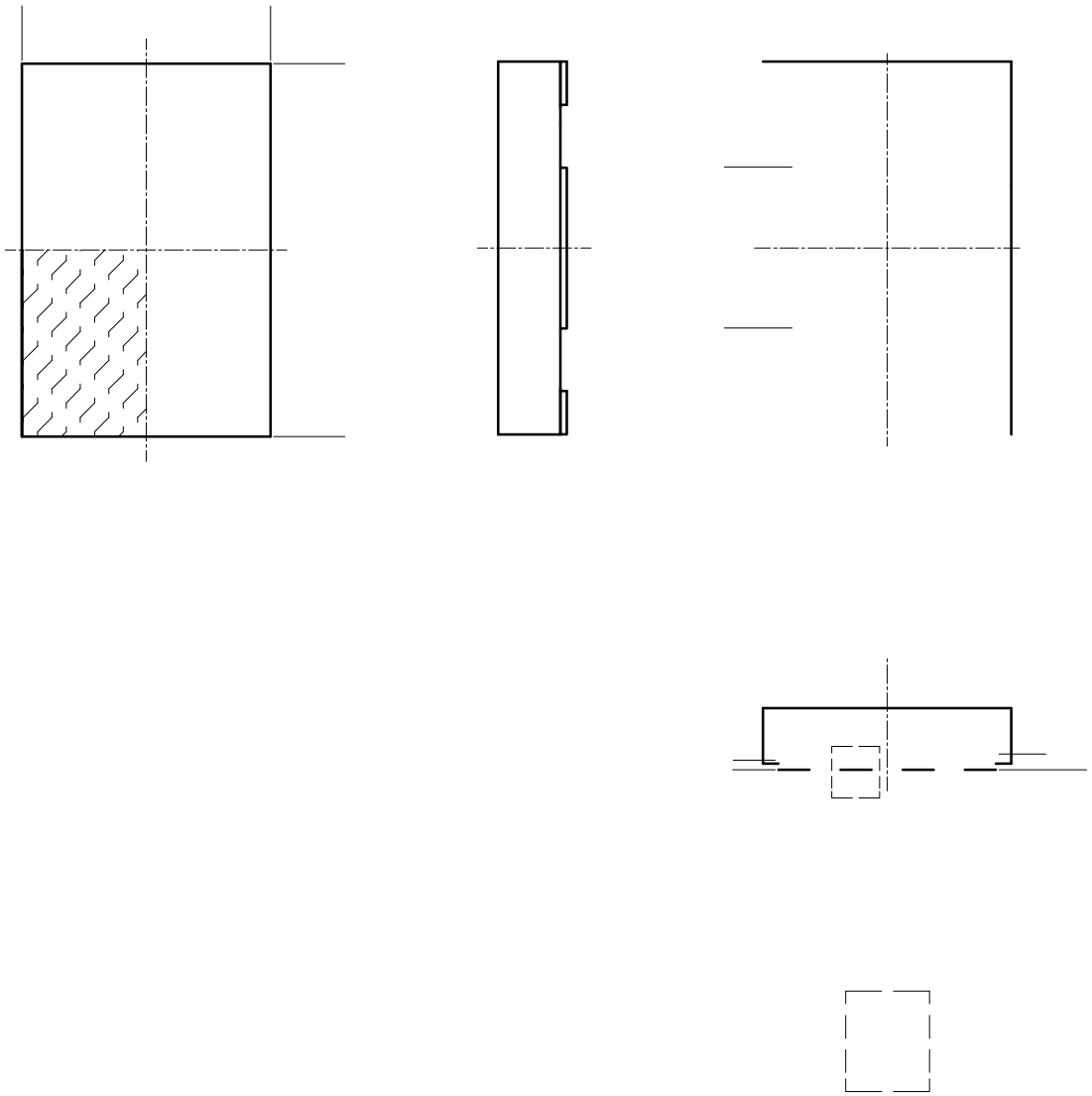



**FRONT VIEW**

**Notes:**
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

## PACKAGE DIMENSIONS

**UDFN8, 2x3 EXTENDED PAD**
CASE 517AZ−01
ISSUE O



## Example of Ordering Information

| Device Order Number | Specific Device Marking | Package Type | Lead Finish | Shipping | Device Revision |
|---|---|---|---|---|---|
| CAT34TS02VP2GT4B (Not recommended for new designs.) | GTB | TDFN−8 | NiPdAu | Tape & Reel, 4,000 Units / Reel | B |
| CAT34TS02VP2GT4C | GTC | TDFN−8 | NiPdAu | Tape & Reel, 4,000 Units / Reel | C |
| CAT34TS02HU4−GT4 | TSU | UDFN−8 | NiPdAu | Tape & Reel, 4,000 Units / Reel | C |

22. All packages are RoHS−compliant (Lead−free, Halogen−free)
23. The standard lead finish is NiPdAu.
24. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.