(Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at V_{DD} = 5.0 V, T_{AMB} = 25°C.)

I_{DD1}	Supply Current Outputs Off	V_{LED} = 5 V, R_{SET} = 24.9 kΩ		2	5	mA
I_{DD2}	Supply Current Outputs Off	V_{LED} = 5 V, R_{SET} = 5.23 kΩ		4	10	mA
I_{DD3}	Supply Current Outputs On	V_{LED} = 0.5 V, R_{SET} = 24.9 kΩ		2	5	mA
I_{DD4}	Supply Current Outputs On	V_{LED} = 0.5 V, R_{SET} = 5.23 kΩ		4	10	mA
I_{SHDN}	Shutdown Current	V_{OE} = 0 V			1	μA
I_{LKG}	LED Output Leakage	V_{LED} = 5 V, Outputs Off	−1		1	μA
R_{OE}	OE Pull−down Resistance		140	190	250	kΩ
V_{OE_IH} V_{OE_IL}	OE Logic High Level OE Logic Low Level		1.3		 0.4	V
V_{PWM_IH} V_{PWM_IL}	PWMx Logic High Level PWMx Logic Low Level		0.7 x V_{DD}		 0.3 x V_{DD}	V
I_{IL}	Logic Input Leakage Current (PWMx)	V_{PWMx} = V_{DD} or GND	−5	0	5	μA
V_{RSETx}	RSETx Regulated Voltage		1.17	1.2	1.23	V
T_{SD}	Thermal Shutdown			150		°C
T_{HYS}	Thermal Hysteresis			20		°C
I_{LED}/I_{RSET}	RSET to LED Current Gain Ratio	100 mA LED Current		400		
V_{UVLO}	Undervoltage Lockout (UVLO) Threshold			1.8		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

(Min and Max values are over recommended operating conditions unless specified otherwise. Typical values are at V_{DD} = 5.0 V, T_{AMB} = 25°C.)

t_{PS}	Turn−On time, OE rising to I_{LED} from Shutdown	I_{LED} = 100 mA		1.4		μs

(V_{IN}

PGND	1	Power Ground.
GND	2	Ground Reference.
PWM3	3	PWM control input for LED3
		PWM control input for LED2

The power dissipation (P_D) of the CAT4109/CAV4109 can be calculated as follows:

$$P_D = (V_{DD} \times I_{DD}) + \Sigma(V_{LEDN} \times I_{LEDN})$$

where V_{LEDN} is the voltage at the LED pin, and I_{LEDN} is the associated LED current. Combinations of high V_{LED} voltage or high ambient temperature can cause the CAT4109/CAV4109 to enter thermal shutdown. In applications where V_{LEDN} is high, a resistor can be inserted in series with the LED string to lower P_D.

Thermal dissipation of the junction heat consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) thermal resistance which is defined by the package style, and the second path is the case to ambient (θ_{CA}) thermal resistance, which is dependent on board layout. The overall junction to ambient (θ_{JA}) thermal resistance is equal to:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

For a given package style and board layout, the operating junction temperature T_J is a function of the power dissipation P_D, and the ambient temperature, resulting in the following equation:

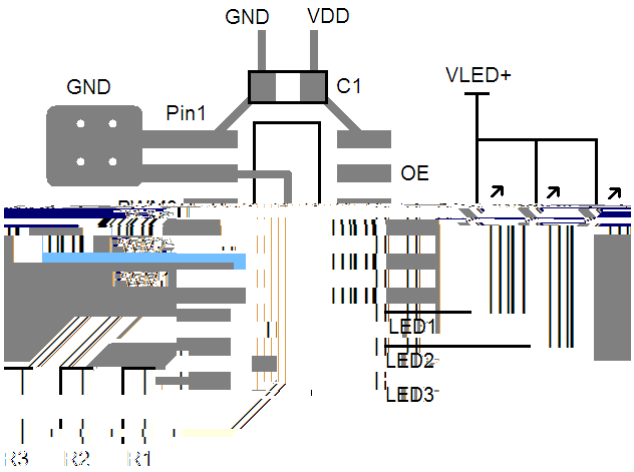
$$T_J = T_{AMB} + P_D (\theta_{JC} + \theta_{CA}) = T_{AMB} + P_D \theta_{JA}$$

When mounted on a double−sided printed circuit board with two square inches of copper allocated for “heat spreading”, the resulting θ_{JA} is about 74°C/W.

For example, at 60°C ambient temperature, the maximum power dissipation is calculated as follow:

$$P_{Dmax} = \frac{(T_{Jmax} - T_{AMB})}{\theta_{JA}} = \frac{(150 - 60)}{74} = 1.2\ W$$

Bypass capacitor C1 should be placed as close to the IC as possible. RSET resistors should be directly connected to the GND pin of the device. For better thermal dissipation, multiple via can be used to connect the GND pad to a large ground plane. It is also recommended to use large pads and traces on the PCB wherever possible to spread out the heat. The LEDs for this layout are driven from a separate supply (VLED+), but they can also be driven from the same supply connected to VDD.



SOIC−16, 150 mils
CASE 751BG
ISSUE O

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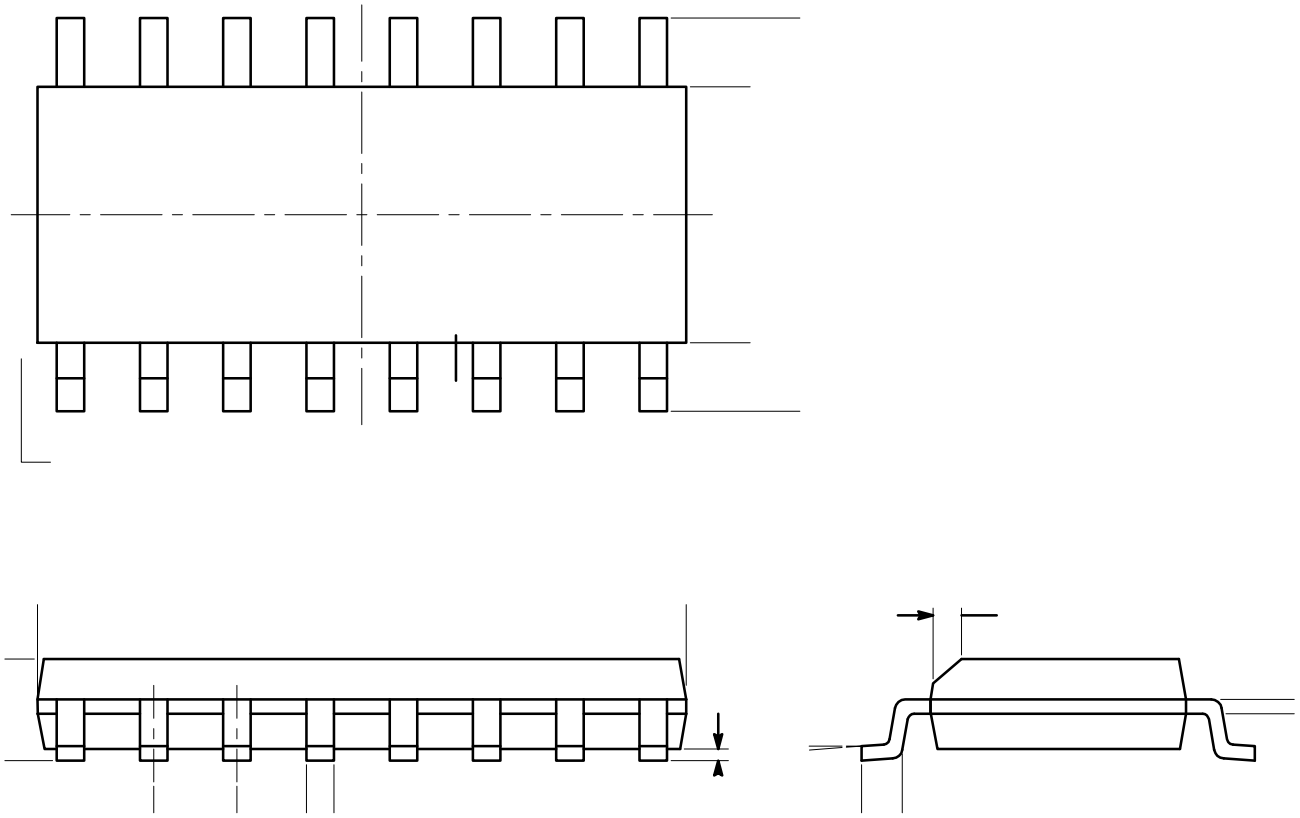

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