CAT6095

Digital Output Temperature Sensor

Description

The CAT6095 is a JEDEC JC42.4 compliant Temperature Sensor designed for general purpose temperature measurements requiring a digital output.

The CAT6095 measures temperature at least 10 times every second.

May, 2011 Rev. 5

Publication Order Number:
CAT6095/D

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the

Table 4. A.C. CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C) (Note 3)

Symbol	Parameter	Min	Max	Units
F_{SCL} (Note 4)	Clock Frequency	10	400	kHz
t_{HIGH}	High Period of SCL Clock	600		ns
t_{LOW}	Low Period of SCL Clock	1300		ns
$t_{TIMEOUT}$ (Note 4)	SMBus SCL Clock Low Timeout	25	35	ms
t_R (Note 5)	SDA and SCL Rise Time		300	ns
t_F (Note 5)	SDA and SCL Fall Time		300	ns
$t_{SU:DAT}$ (Note 6)	Data Setup Time	100		ns
$t_{HD:DAT}$ (Note 5)	Data Hold Time (for Input Data)	0		ns
	Data Hold Time (for Output Data)	300	900	ns
$t_{SU:STA}$	START Condition Setup Time	600		ns
$t_{HD:STA}$	START Condition Hold Time	600		ns
$t_{SU:STO}$	STOP Condition Setup Time	600		ns
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
T_i	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{PU} (Note 7)	Power−up Delay to Valid Temperature Recording		100	ms

3. Timing reference points are set at 30%, respectively 70% of V_{CC}, as illustrated in Figure 11. Bus loading must be such as to allow meeting the V_{IL}, V_{OL} as well as the various timing limits.
4. The TS interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count is started (and then re−started) on every negative transition of SCL in the time interval between START and STOP.
5. In a “Wired−OR” system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull−down device must be able to sink the (external) bus pull−up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} - t_{HD:DAT} - t_{SU:DAT}$, where t_{LOW} and $t_{HD:DAT}$ are actual values (rather than spec limits). A shorter $t_{HD:DAT}$

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins set the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power On Reset

The CAT6095 incorporates Power−On Reset (POR) circuitry which monitors the supply voltage, and then resets (initializes) the internal state machine below a POR trigger level of approximately 2.0 V, i.e. well below the minimum recommended V_{CC} value.

The temperature sensor (TS) powers-up into conversion mode. The internal state machine will operate properly above the POR trigger level, but valid temperature readings can be expected only after the first conversion cycle started and completed at nominal supply voltage.

Device Interface

The CAT6095 supports IPowe210 0 0 10 136.668..8225.419.0002 15(edgeC thenSMBusa storsmit)]Ts t8842 TD0 Tc.0027 5w[(On)3erltocol

Write Operations

Temperature Sensor Register Write

To write data to a TS register the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to ‘0’), followed by an address byte and two data bytes. The matching Slave will acknowledge the Slave address, TS register address and the TS register data (Figure 12). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the TS register update. Note that all registers in the TS are ‘volatile’ meaning any data contained in them is lost when power is removed from the chip.

Read Operations

Immediate Read

Upon power-up, the Temperature Sensor (TS) address counter is initialized to 00h. The TS address counter will thus point to the Capability Register. This address counter may be updated by subsequent operations.

A CAT6095 presented with a Slave address containing a ‘1’ in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting data being pointed at by the current TS register address counter. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 13).

Selective Read

The Read operation can be started at an address different from the one stored in the address counter, by preceding the Immediate Read sequence with a ‘data less’ Write operation. The Master sends out a START, Slave address and address byte, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figure 14).

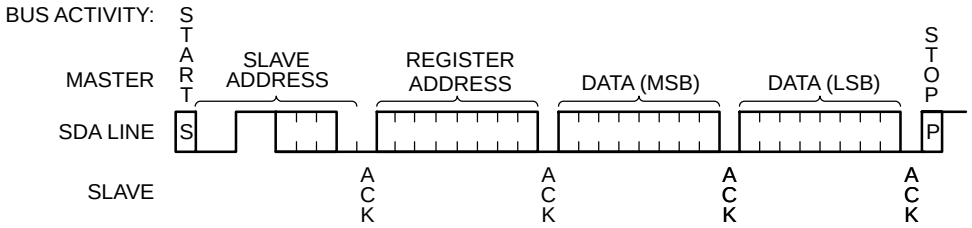


Figure 12. Temperature Sensor Register Write

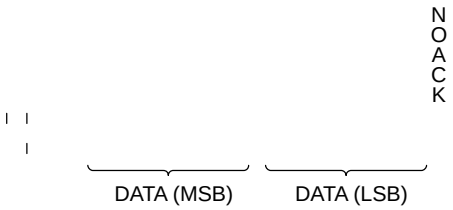


Figure 13. Immediate Read

Temperature Sensor Operation

The CAT6095 temperature sensor (TS) combines a Proportional to Absolute Temperature (PTAT) sensor with a $\Sigma-\Delta$ modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

Registers

The CAT6095 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 6. Upon power−up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The CAT6095 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the $\overline{\text{EVENT}}$ pin. To avoid undesirable $\overline{\text{EVENT}}$ pin activity, this pin is automatically disabled at power−up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two’s complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

Temperature Data Register (User Read Only)

Table 6. TEMPERATURE SENSOR REGISTERS

Register Address	Register Name	Power On Default	Read/Write
0x00			

Table 8. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**			

Table 9. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 10. LOW LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 11. TCRIT LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 12. TEMPERATURE DATA REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C (Note 16)	0.125°C (Note 16)	0.0625°C (Note 16)

16. When applicable (as defined by Capability bit TRES), unsupported bits will read as 0

Bit	Description
B15	0: Temperature is below the TCRIT limit 1: Temperature is equal to or above the TCRIT limit
B14	0: Temperature is equal to or below the High limit 1: Temperature is above the High limit
B13	0: Temperature is equal to or above the Low limit 1: Temperature is below the Low limit

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 13. 12 BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

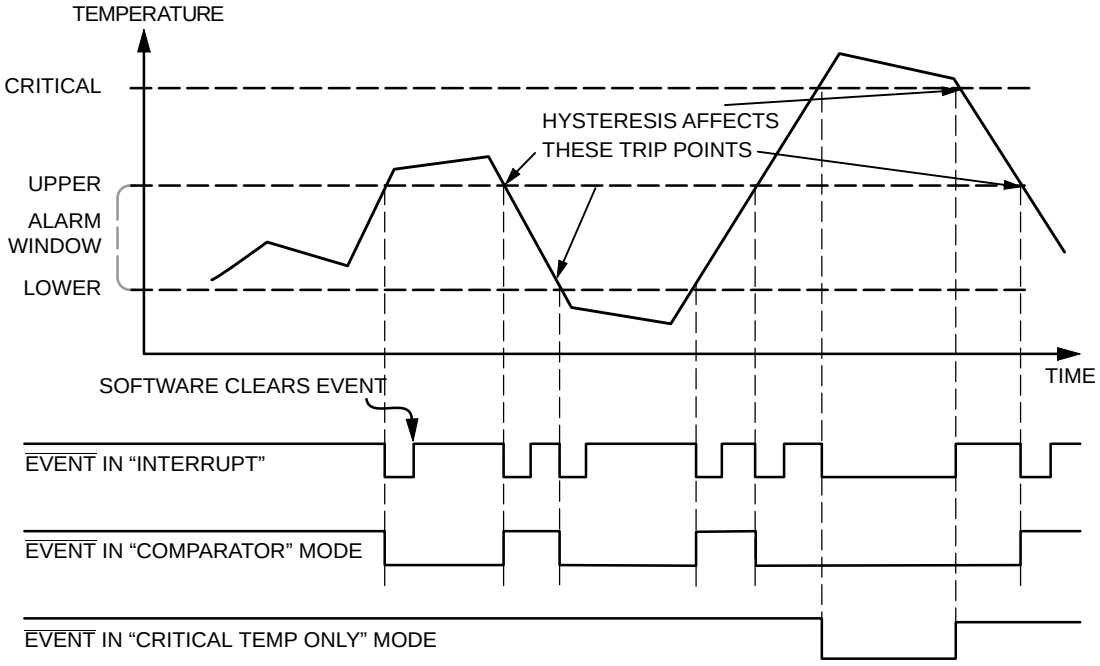
The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 15, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the enabled $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. When the temperature exceeds the critical limit, the event remains asserted as long as the temperature stays above the critical limit and can not be cleared.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 16.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT6095 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.



*EVENT cannot be cleared once the DUT temperature is greater than the critical temperature

Figure 15. Event Detail

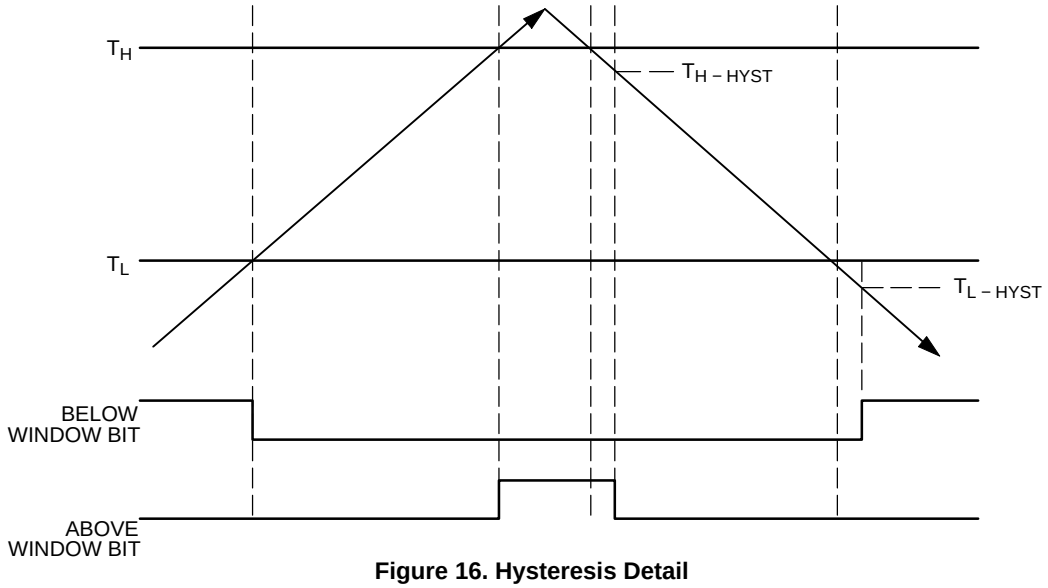
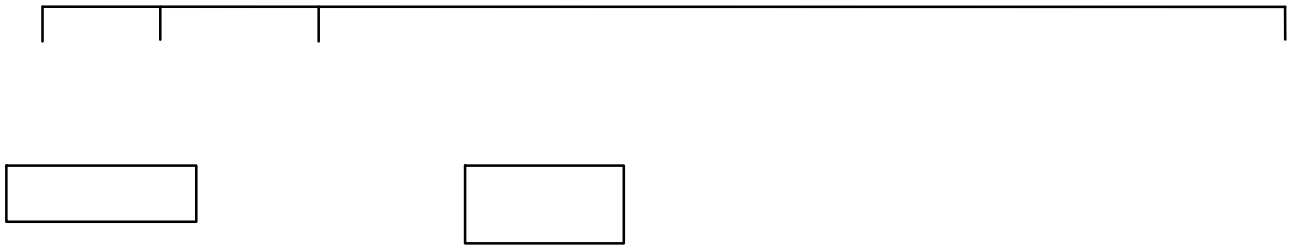


Figure 16. Hysteresis Detail

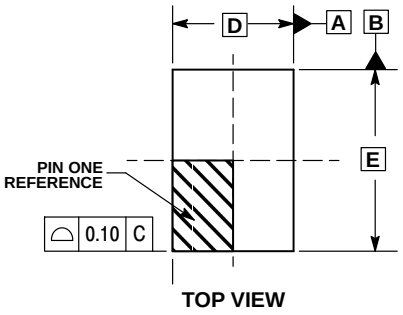
Example of Ordering Information



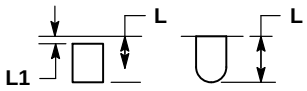
TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

SCALE 2:1

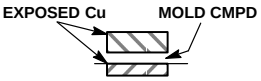
DATE 18 MAR 2015



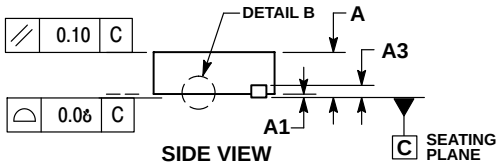
TOP VIEW



DETAIL A
ALTERNATE
CONSTRUCTIONS



DETAIL B
ALTERNATE
CONSTRUCTION

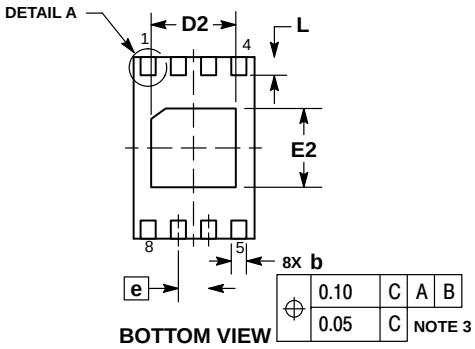


SIDE VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.20	1.40
e	0.50 BSC	
L	0.20	0.40
L1	–––	0.15

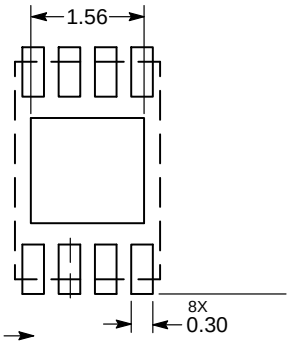
GENERIC
MARKING DIAGRAM*



BOTTOM VIEW

XXXXX = Specific Device Code

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.