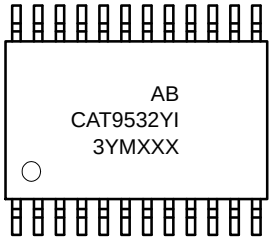
# 1 - 2 2

## Description

The CAT9532 is a CMOS device that provides 16−bit parallel input/output port expander optimized for LED dimming control. The CAT9532 outputs can drive directly 16 LEDs in parallel. Each individual LED may be turned ON, OFF, or blinking at one of two programmable rates. The device provides a simple solution for dimming

## MARKING DIAGRAMS

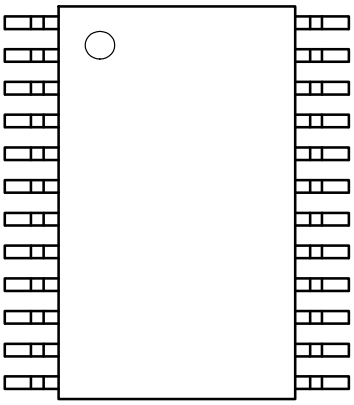



TSSOP (Y)

A = Assembly Location
B = Product Revision (Fixed as “B”)
CAT9532Y = Device Code
I = Temperature Range
3 = Matte-Tin Lead Finish
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number


TQFN (HV6)

LAAC = Device Code
A = Assembly Location
XXX = Last Three Digits of Assembly Lot Number
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
CC = Country Code
TH = Thailand
MY = Malaysia



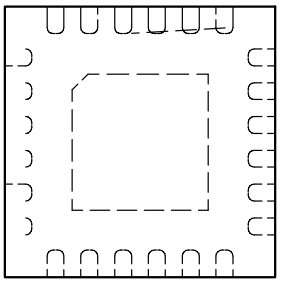


**Figure 1. Pin Configurations**

**LED5A2A1A0VCCSDASCLLED6LED7VSSLED8LED9LED10TSSOP (Y)(Top View)TQFN (HV**

## RESET

**Table 1. PIN DESCRIPTION**

| TSSOP | TQFN | Pin Name | Function |
|---|---|---|---|
| 1 | 22 | A0 | Address Input 0 |
| 2 | 23 | A1 | Address Input 1 |
| 3 | 24 | A2 | Address Input 2 |
| 4−11 | 1−8 | LED0 − LED7 | LED Driver Output 0 to 7, I/O Port 0 to 7 |
| 12 | 9 | $V_{SS}$ | Ground |
| 13−20 | 10−17 | LED8 − LED15 | LED Driver Output 8 to 15, I/O Port 8 to 15 |
| 21 | 18 | $\overline{\text{RESET}}$ | Reset Input |
| 22 | 19 | SCL | Serial Clock |
| 23 | 20 | SDA | Serial Data |
| 24 | 21 | $V_{CC}$ | Power Supply |

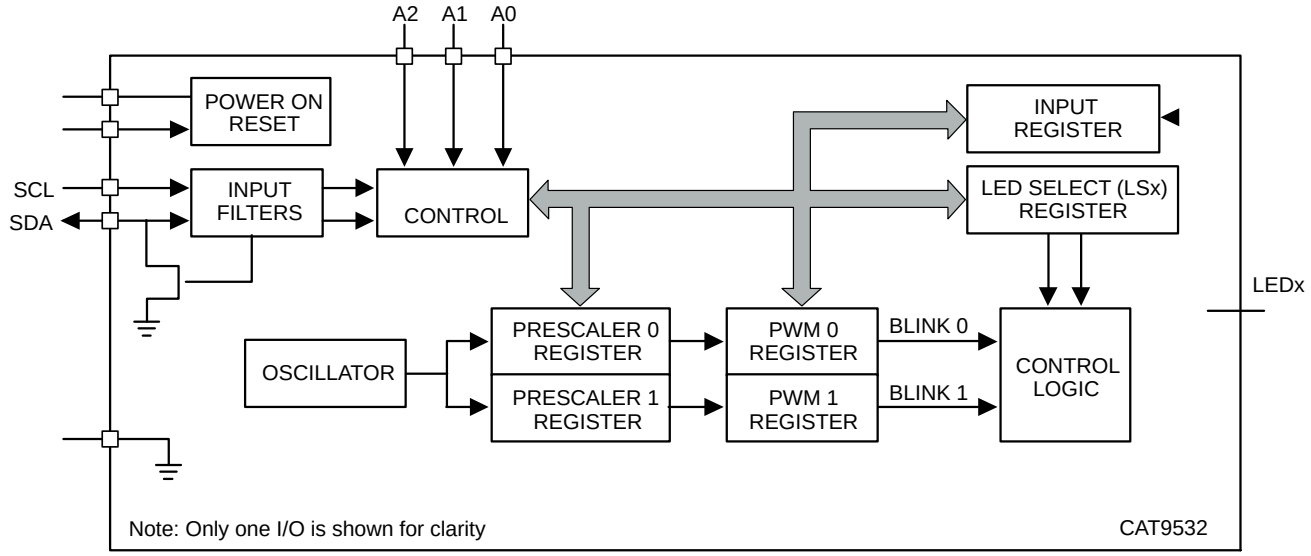


**Table 3. D.C. OPERATING CHARACTERISTICS** ($V_{CC}$ = 2.3 to 5.5 V, $V_{SS}$ = 0 V; $T_A$ = −40°C to +85°

**Table 4. A.C. CHARACTERISTICS** ($V_{CC}$ = 2.3 V to 5.5 V, $T_A$ = −40°C to +85°C, unless otherwise specified) (Note 5)

| Symbol | Parameter | Standard I²C | | Fast I²C | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $F_{SCL}$ | Clock Frequency | | 100 | | 400 | kHz |
| $t_{HD:STA}$ | START Condition Hold Time | 4 | | 0.6 | | µs |
| $t_{LOW}$ | | | | | | |

## Pin Description

### SCL: Serial Clock

The serial clock input clocks all data transferred into or out

### Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data. The SDA line remains stable LOW during the HIGH period of the acknowledge related clock pulse (Figure 7).

The CAT9532 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8− bit byte.

When the CAT9532 begins a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT9532 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition. The master must then issue a stop condition to return the CAT9532 to the standby power mode and place the device in a known state.

### Registers and Bus Transactions

After the successful acknowledgement of the slave address, the bus master will send a command byte to the CAT9532 which will be stored in the Control Register. The

The Input Register 0 and Input Register 1 reflect the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an

### Write Operations

Data is transmitted to the CAT9532 registers using the write sequence shown in Figure 9.

If the AI bit from the command byte is set to “1”, the CAT9532 internal registers can be written sequentially. After sending data to one register, the next data byte will be sent to the next register sequentially addressed.

### Read Operations

The CAT9532 registers are read according to the timing diagrams shown in Figure 10 and Figure 12. Data from the register, defined by the command byte, will be sent serially on the SDA line.

After the first byte is read, additional data bytes may be read when the auto−increment flag, AI, is set. The additional data byte will reflect the data read from the next register sequentially addressed by the (B3 B2 B1 B0) bits of the command byte.

When reading Input Port Registers (Figure 12), data is clocked into the register on the failing edge of the acknowledge clock pulse. The transfer is stopped when the master will not acknowledge the data byte received and issue the STOP condition.

### LED Pins Used as General Purpose I/O

Any LED pins not used to drive LEDs can be used as general purpose input/output, GPIO.

When used as input, the user should program the corresponding LED pin to Hi−Z (“00” for the LSx register bits). The pin state can be read via the Input Register according to the sequence shown in Figure 12.

For use as output, an external pull−up resistor should be connected to the pin. The value of the pull−up resistor is calculated according to the DC operating characteristics. To set the LED output high, the user has to program the output Hi−Z writing “00” into the corresponding LED Selector (LSx) register bits. The output pin is set low when the LED output is programmed low through the LSx register bits (“01” in LSx register bits).

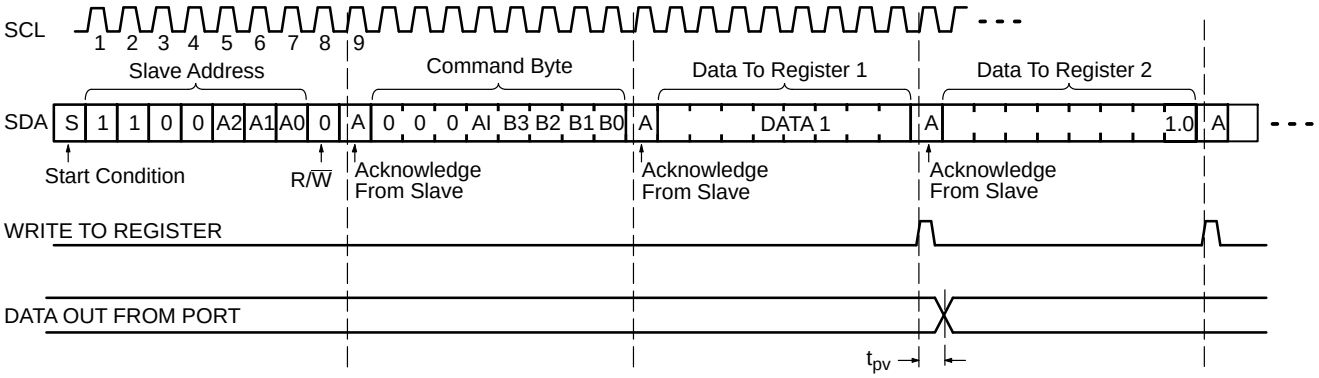
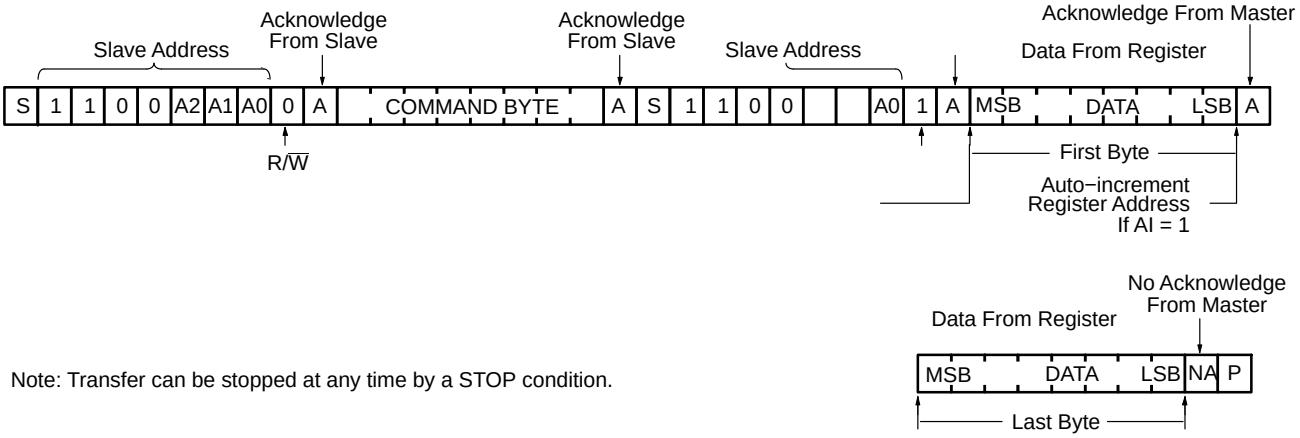



**Figure 9. Write to Register Timing Diagram**




Note: Transfer can be stopped at any time by a STOP condition.

**Figure 10. Read from Register Timing Diagram**

### External Reset Operation

The CAT9532 registers and the $I^2C$ state machine are initialized to their default state when the RESET input is held low for a minimum of $t_W$. The external Reset timing is shown in Figure 13.

### LED Output Operation

Figure 11 shows typical current values for LED pin voltages at various case temperatures.

### Power−On Reset Operation

The CAT9532 incorporates Power−On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state. The device is in a reset state for $V_{CC}$ less than the internal POR threshold level ($V_{POR}$). When $V_{CC}$ exceeds the $V_{POR}$ level, the reset state is released and the CAT9532 internal state machine and registers are initialized to their default state.

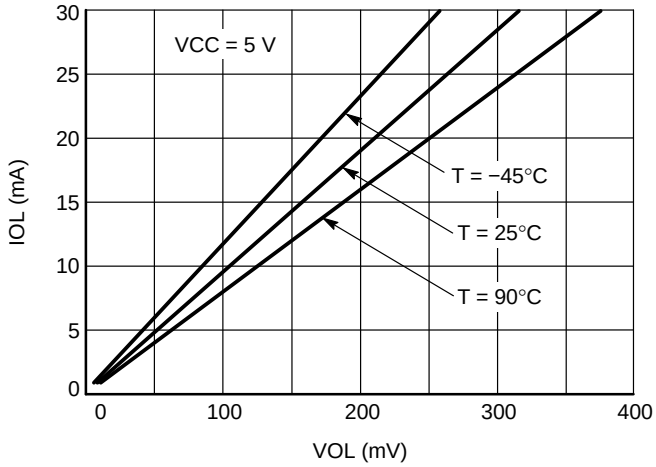



**Figure 11. IOL vs VOL for LED Pin**

## Application Information

### Programming Example

The following programming sequence is an example how to set:

- LED0 to LED3: ON
- LED4 to LED7: Dimming at 30% brightness; Blink 1: 152 Hz, duty cycle 30%
- LED8 to LED11: Blink at 2 Hz with 50% duty cycle (Blink 2)
- LED12 to LED15: OFF

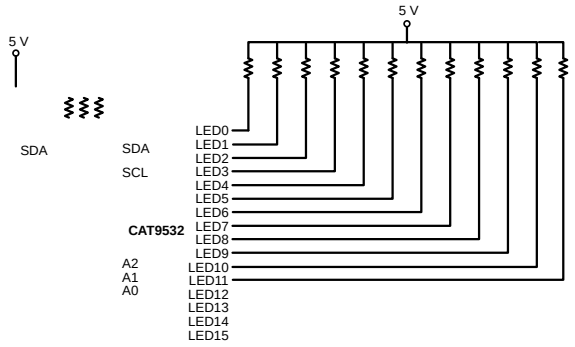



**Figure 14. Typical Application**

## Ordering Information (Notes 9 to 13)

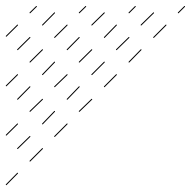
9. All packages are RoHS−compliant (Lead−free, Halogen−free).
10. The standard plated finish is Matte−Tin for SOIC and TSSOP packages. The standard plated finish is NiPdAu for TQFN package.
11. The device used in the above example is a CAT9532WI−T1 (SOIC, Industrial Temperature, Matte−Tin, Tape & Reel, 1,000/Reel).
12. For additional temperature options, please contact your nearest **onsemi** Sales office.
13. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**Table 12. ORDERING PART NUMBER**

| Part Number | Package | Lead Finish |
|---|---|---|
| CAT9532YI−9 | | |

**TQFN24, 4x4**
CASE 510AG
ISSUE B

DATE 04 DEC 2009



**TSSOP24, 4.4x7.8**
CASE 948AR
ISSUE A

DATE 17 MAR 2009