

• These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- White Goods (dishwashers, washing machines)
- Handheld Devices (cell phones, PDAs, digital cameras)
- Data Communications (routers, hubs and servers)
- 1. All I/Os are set to inputs at RESET.

(Top View)

TQFN 4 x 4 mm (HV4)

V_{SS} 1/05

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A1 A0 SDA SDA

A2

I/O₀

I/O₁

 I/O_2

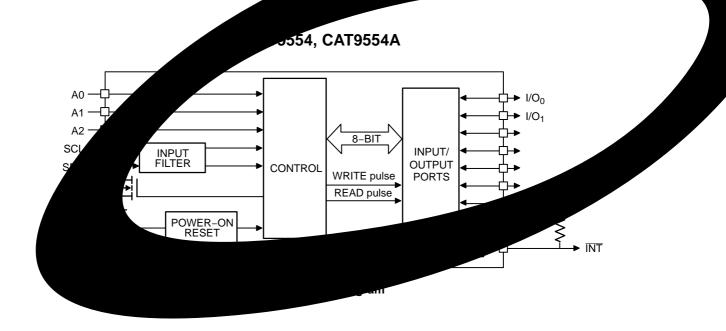
SCL

 I/O_6

C

ORDERING INFORMATION

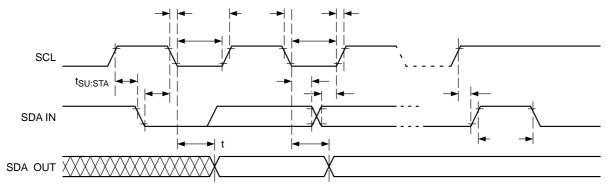
See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.



Symbol	Parameter	Stand	Standard I ² C		Fast I ² C	
		Min	Max	Min	Max	Units
F _{SCL}	Clock Frequency		100		400	kHz
t _{HD:STA}	START Condition Hold Time	4		0.6		μs
t _{LOW}	Low Period of SCL Clock	4.7		1.3		μS
t _{HIGH}	High Period of SCL Clock	4		0.6		μS
t _{SU:STA}	START Condition Setup Time	4.7		0.6		μS
t _{HD:DAT}	Data In Hold Time	0		0		μS
t _{SU:DAT}	Data In Setup Time	250		100		ns
_R (Note 9)	SDA and SCL Rise Time		1000		300	ns

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V; T_A = -40°C to +85°C, unless otherwise specified.) (Note 8)

t_F (Note 9)





INT: Interrupt Output

The open-drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read. Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.



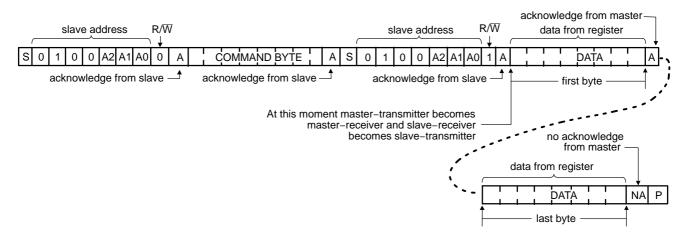
Acknowledge

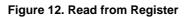
The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip–flop controlling the output, not the actual I/O pin value.

Power-On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power–on reset pulse holds the CAT9554/9554A in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset

condition is released and the internal state machine and the CAT9554/9554A registers are initialized to their default state.





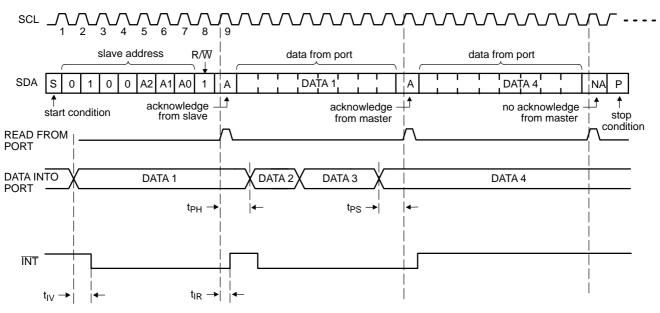
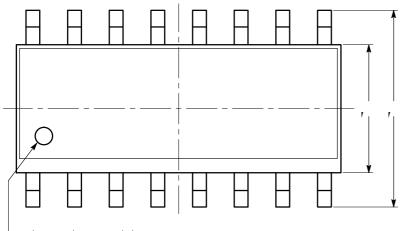


Figure 13. Read Input Port Register

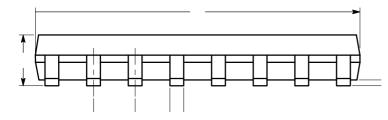
PACKAGE DIMENSIONS

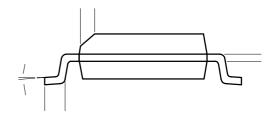
SOIC-16, 150 mils CASE 751BG-01 ISSUE O



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TOP VIEW





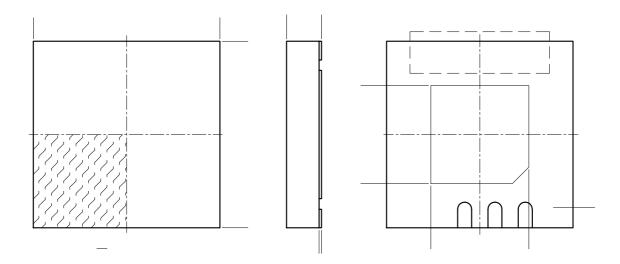
SIDE VIEW

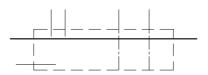
END VIEW

Notes:

PACKAGE DIMENSIONS

TQFN16, 4x4 CASE 510AE-01 ISSUE A







PACKAGE DIMENSIONS

TSSOP16, 4.4x5 CASE 948AN-01 ISSUE O

