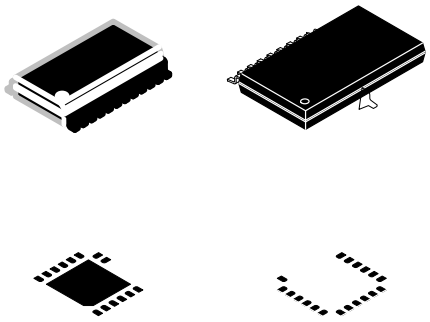


−24
HT6 SUFFIX
CASE 510AN

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 16 of this data sheet.

Table 1. PIN DESCRIPTION

SOIC / TSSOP	TQFN	Pin Name	Function
1	22	$\overline{INT}$	Interrupt Output (open drain)
2	23	A1	Address Input 1
3	24	A2	Address Input 2
4−11	1−8	$I/O_{0.0}$ − $I/O_{0.7}$	I/O Port 0.0 to I/O Port 0.7
12	9	V_{SS}	Ground
13−20	10−17	$I/O_{1.0}$ − $I/O_{1.7}$	I/O Port 1.0 to I/O Port 1.7
21	18	A0	Address Input 0
22	19	SCL	Serial Clock
23	20	SDA	Serial Data
24	21	V_{CC}	Power Supply

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
V_{CC} with Respect to Ground	−0.5 to +6.5	V
Voltage on Any Pin with Respect to Ground	−0.5 to +5.5	V
DC Current on $I/O_{1.0}$ to $I/O_{1.7}$, $I/O_{0.0}$ to $I/O_{0.7}$	±50	mA
DC Input Current	±20	mA
V_{CC} Supply Current	160	mA
V_{SS} Supply Current	200	mA
Package Power Dissipation Capability (T_A = 25°C)	1.0	W
Junction Temperature	+150	°C
Storage Temperature	−65 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 3. RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Units
V_{ZAP} (Note 1)	ESD Susceptibility	JEDEC Standard JESD 22	2000	V
I_{LTH} (Note 1)	Latch−up	JEDEC JESD78A	100	mA

1. This parameter is tested initially and after a design or process change that affects the parameter.

Table 4. D.C. OPERATING CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V; V_{SS} = 0 V; T_A = −40°C to +85°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SUPPLIES						
V_{CC}	Supply voltage		2.3	−	5.5	V
I_{CC}	Supply current	Operating mode; V_{CC} = 5.5 V; no load; f_{SCL} = 100 kHz	−	135	200	μA
I_{stbl}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{SS}$; f_{SCL} = 0 kHz; I/O = inputs	−	1.1	1.5	mA
I_{stbh}	Standby current	Standby mode; V_{CC} = 5.5 V; no load; $V_I = V_{CC}$; f_{SCL} = 0 kHz; I/O = inputs	−	0.75	1	μA
V_{POR}	Power−on reset voltage	No load; $V_I = V_{CC}$ or V_{SS}	−	1.5	1.65	V
SCL, SDA, $\overline{INT}$						
V_{IL} (Note 2)	Low level input voltage		−0.5	−	0.3 x V_{CC}	V
V_{IH}						

Table 5. A.C. CHARACTERISTICS (V_{CC} = 2.3 V to 5.5 V, T_A = −40°C to +85°C, unless otherwise specified) (Note 6)

Symbol	Parameter	Standard I^2C		Fast I^2C		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		μs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		μs
t_{HIGH}	High Period of SCL Clock	4		0.6		μs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		μs
$t_{HD:DAT}$	Data In Hold Time	0		0		μs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R (Note 7)	SDA and SCL Rise Time		1000		300	ns
t_F (Note 7)	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		μs
t_{BUF} (Note 7)	Bus Free Time Between STOP and START	4.7		1.3		μs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	μs
t_{DH}	Data Out Hold Time	100		50		ns
T_i (Note 7)						

Pin Description

SCL: Serial Clock

The serial clock input clocks all data transferred into or out of the device. The SCL line requires a pull−up resistor if it is driven by an open drain output.

SDA: Serial Data/Address

The bidirectional serial data/address pin is used to transfer all data into and out of the device. The SDA pin is an open drain output and can be wire−ORed with other open drain or open collector outputs. A pull−up resistor must be connected from SDA line to V_{CC}. The value of the pull−up resistor, R_P, can be calculated based on minimum and maximum values from Figure 4 and Figure 5 (see Note).

A0, A1, A2: Device Address Inputs

These inputs are used for extended addressing capability. The A0, A1, A2 pins should be hardwired to V_{CC} or V_{SS}. When hardwired, up to eight CAT9555s may be addressed on a single bus system. The levels on these inputs are compared with corresponding bits, A2, A1, A0, from the slave address byte.

$I/O_{0.0}$ to $I/O_{0.7}$, $I/O_{1.0}$ to $I/O_{1.7}$: Input / Output Ports

Any of these pins may be configured as input or output. The simplified schematic of I/O_0 to I/O_7 is shown in Figure 6. When an I/O is configured as an input, the Q1 and Q2 output transistors are off creating a high impedance input with a weak pull−up resistor (typical 100 kΩ). If the I/O pin is configured as an output, the push−pull output stage is enabled. Care should be taken if an external voltage is applied to an I/O pin configured as an output due to the low impedance paths that exist between the pin and either V_{CC} or V_{SS}.

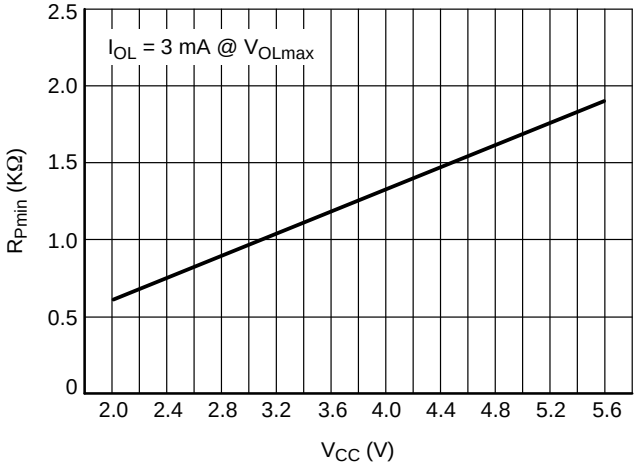


Figure 4. Minimum R_P as a Function of Supply Voltage

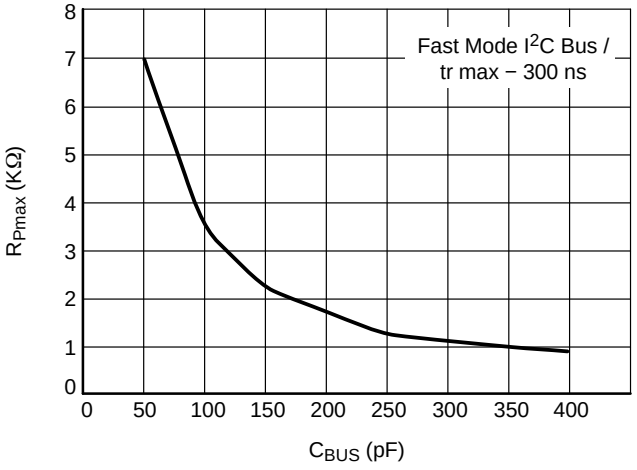


Figure 5. Maximum R_P Value vs. Bus Capacitance

NOTE: According to the Fast Mode I^2C bus specification, for bus capacitance up to 200 pF, the pull up device can be a resistor. For bus loads between 200 pF and 400 pF, the pull−up device can be a current source (Imax = 3 mA) or a switched resistor circuit.

$\overline{\text{INT}}$: Interrupt Output

The open−drain interrupt output is activated when one of the port pins configured as an input changes state (differs from the corresponding input port register bit state). The interrupt is deactivated when the input returns to its previous state or the input port register is read.

Since there are two 8−bit ports that are read independently, the interrupt caused by Port 0 will not be cleared by a read of Port 1, or vice versa.

Changing an I/O from an output to an input may cause a false interrupt if the state of the pin does not match the contents of the input port register.

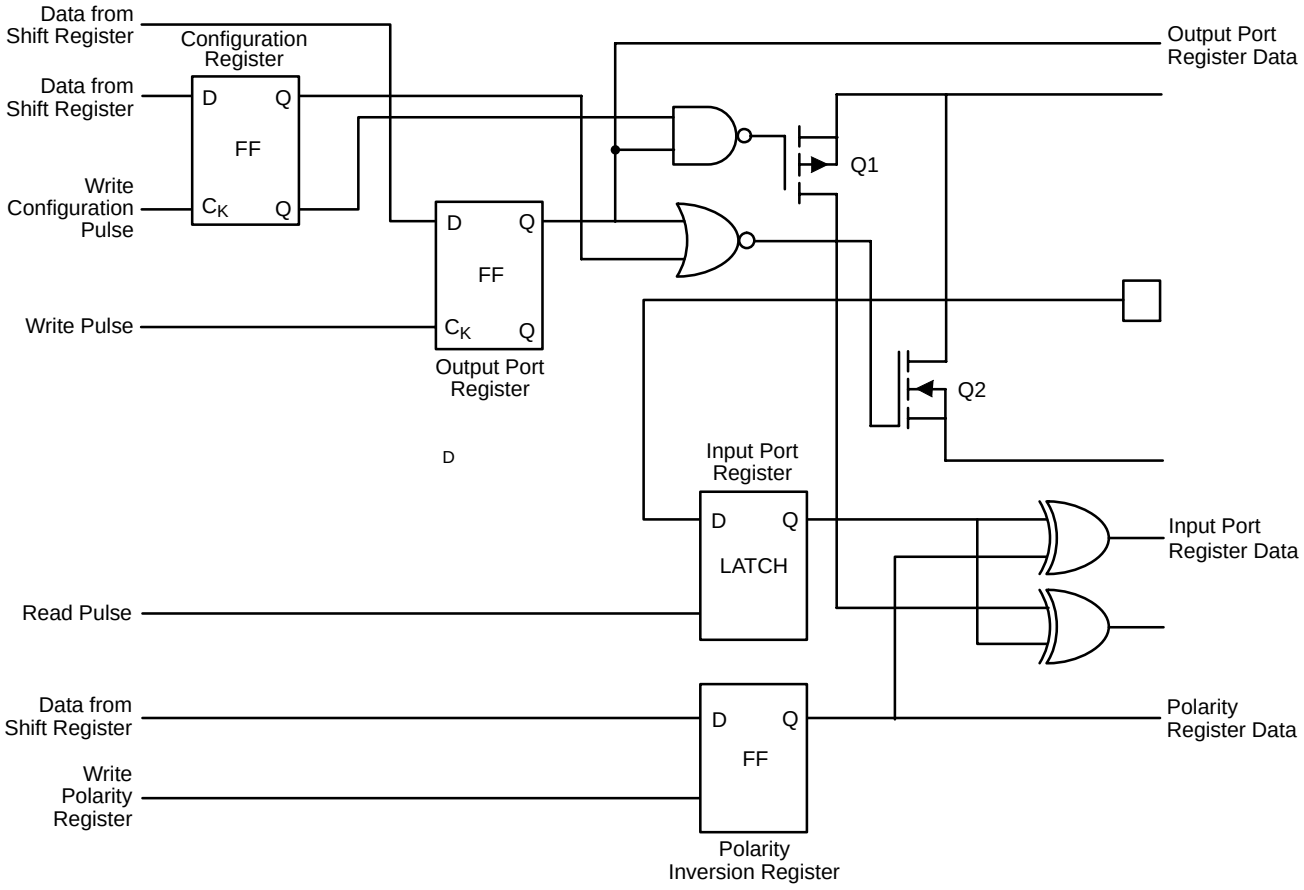


Figure 6. Simplified Schematic of I/Os

FUNCTIONAL DESCRIPTION

The CAT9555 general purpose input/output (GPIO) peripheral provides up to sixteen I/O ports, controlled through an I^2C compatible serial interface.

The CAT9555 supports the I^2C Bus data transmission protocol. This Inter−Integrated Circuit Bus protocol defines any device that sends data to the bus to be a transmitter and any device receiving data to be a receiver. The transfer is controlled by the Master device which generates the serial clock and all START and STOP conditions for bus access. The CAT9555 operates as a Slave device. Both the Master device and Slave device can operate as either transmitter or receiver, but the Master device controls which mode is activated.

I^2C Bus Protocol

The features of the I^2C bus protocol are defined as follows:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition (Figure 7).

START and STOP Conditions

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT9555 monitors the SDA and SCL lines and will not respond until this condition is met.

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

After the bus Master sends a START condition, a slave address byte is required to enable the CAT9555 for a read or write operation. The four most significant bits of the slave address are fixed as binary 0100 (Figure 8). The CAT9555 uses the next three bits as addressts as3( )is req3 the M0 TD-.eree bits as a performed. When thia-.00-is set to “1”, a read operation-is initiated, and when set to “0”, a write operation-is selected.

Following the START condition and the slave address byte, the CAT9555 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the

Registers and Bus Transactions

The CAT9555 internal registers and their address and function are shown in Table 7.

The command byte is the first byte to follow the device address byte during a write/read bus transaction. The register command byte acts as a pointer to determine which register will be written or read.

The input port register is a read only port. It reflects the incoming logic levels of the I/O pins, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

Table 7. REGISTER COMMAND BYTE

Command (hex)	Register
0h	Input Port 0
1h	Input Port 1
2h	Output Port 0
3h	Output Port 1
4h	Polarity Inversion Port 0
5h	Polarity Inversion Port 1
6h	Configuration Port 0
7h	Configuration Port 1

Table 8. REGISTERS 0 AND 1 – INPUT PORT REGISTERS

bit	$I_{0.7}$	$I_{0.6}$	$I_{0.5}$	$I_{0.4}$	$I_{0.3}$	$I_{0.2}$	$I_{0.1}$	$I_{0.0}$
default	X	X	X	X	X	X	X	X
bit	$I_{1.7}$	$I_{1.6}$	$I_{1.5}$	$I_{1.4}$	$I_{1.3}$	$I_{1.2}$	$I_{1.1}$	$I_{1.0}$
default	X	X	X	X	X	X	X	X

Table 9. REGISTERS 2 AND 3 – OUTPUT PORT REGISTERS

bit	$O_{0.7}$	$O_{0.6}$	$O_{0.5}$	$O_{0.4}$	$O_{0.3}$	$O_{0.2}$	$O_{0.1}$	$O_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$O_{1.7}$	$O_{1.6}$	$O_{1.5}$	$O_{1.4}$	$O_{1.3}$	$O_{1.2}$	$O_{1.1}$	$O_{1.0}$
default	1	1	1	1	1	1	1	1

Table 10. REGISTERS 4 AND 5 – POLARITY INVERSION REGISTERS

bit	$N_{0.7}$	$N_{0.6}$	$N_{0.5}$	$N_{0.4}$	$N_{0.3}$	$N_{0.2}$	$N_{0.1}$	$N_{0.0}$
default	0	0	0	0	0	0	0	0
bit	$N_{1.7}$	$N_{1.6}$	$N_{1.5}$	$N_{1.4}$	$N_{1.3}$	$N_{1.2}$	$N_{1.1}$	$N_{1.0}$
default	0	0	0	0	0	0	0	0

Table 11. REGISTERS 6 AND 7 – CONFIGURATION REGISTERS

bit	$C_{0.7}$	$C_{0.6}$	$C_{0.5}$	$C_{0.4}$	$C_{0.3}$	$C_{0.2}$	$C_{0.1}$	$C_{0.0}$
default	1	1	1	1	1	1	1	1
bit	$C_{1.7}$	$C_{1.6}$	$C_{1.5}$	$C_{1.4}$	$C_{1.3}$	$C_{1.2}$	$C_{1.1}$	$C_{1.0}$
default	1	1	1	1	1	1	1	1

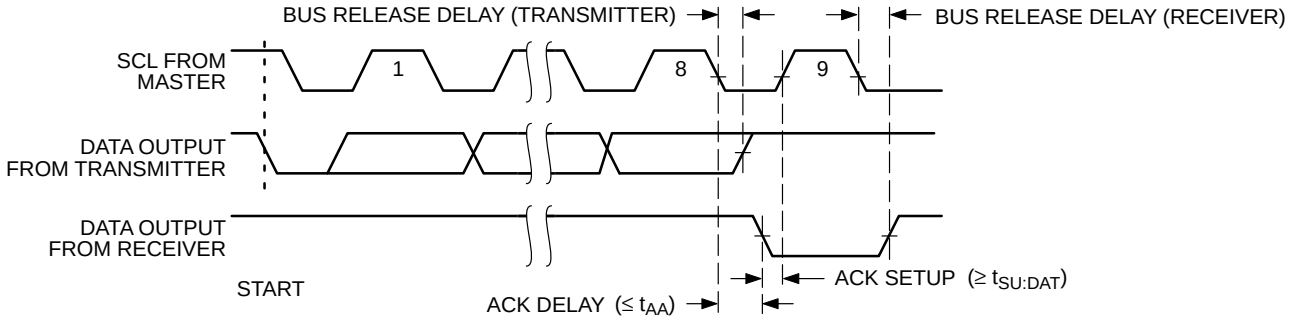


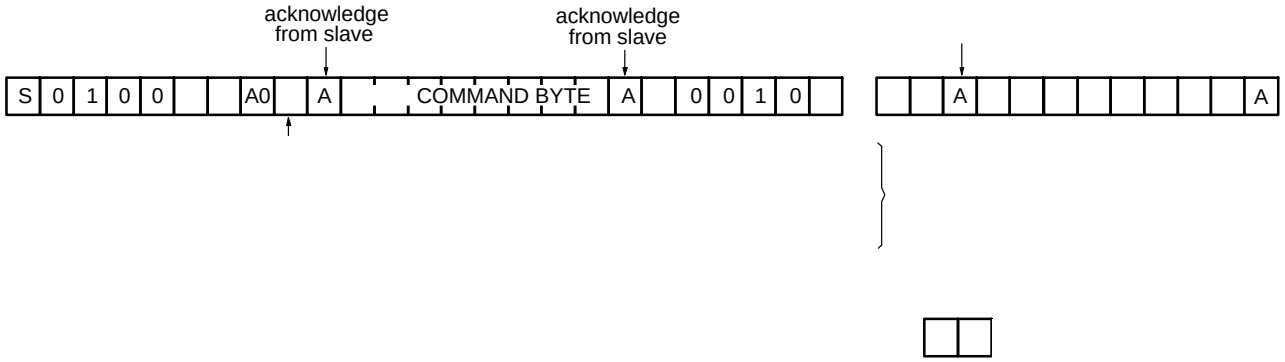
Figure 9. Acknowledge Timing

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Bit values in this register have no effect on I/O pins defined as inputs. Reads from the output port register reflect the value that is in the flip-flop controlling the output, not the actual I/O pin value.

The polarity inversion register allows the user to invert the polarity of the input port register data. If a bit in this register

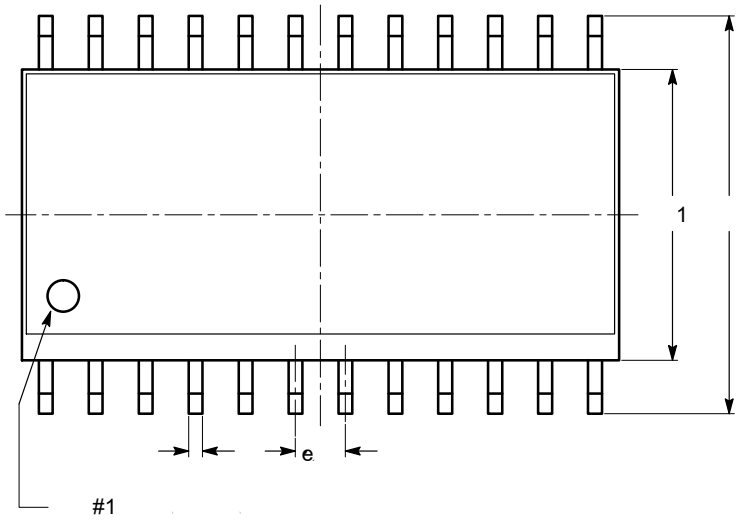
Power-On Reset Operation

When the power supply is applied to V_{CC} pin, an internal power-on reset pulse holds the CAT9555 in a reset state until V_{CC} reaches V_{POR} level. At this point, the reset condition is released and the internal state machine and the CAT9555 registers are initialized to their default state.



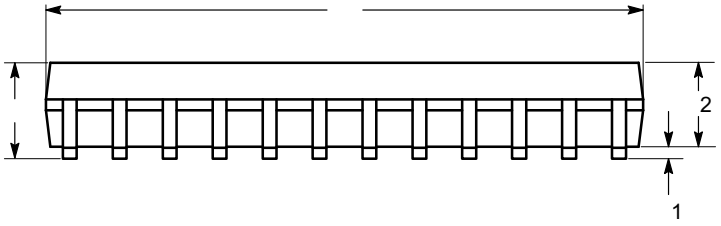
PACKAGE DIMENSIONS

SOIC−24, 300 mils
CASE 751BK−01
ISSUE O



TOP VIEW

SYMBOL	MIN	NOM	MAX
A			
A1	0.10		
b	0.31		
c	0.20		
D			
E			
E1			
e			
h	0.25		
θ	0		



SIDE VIEW

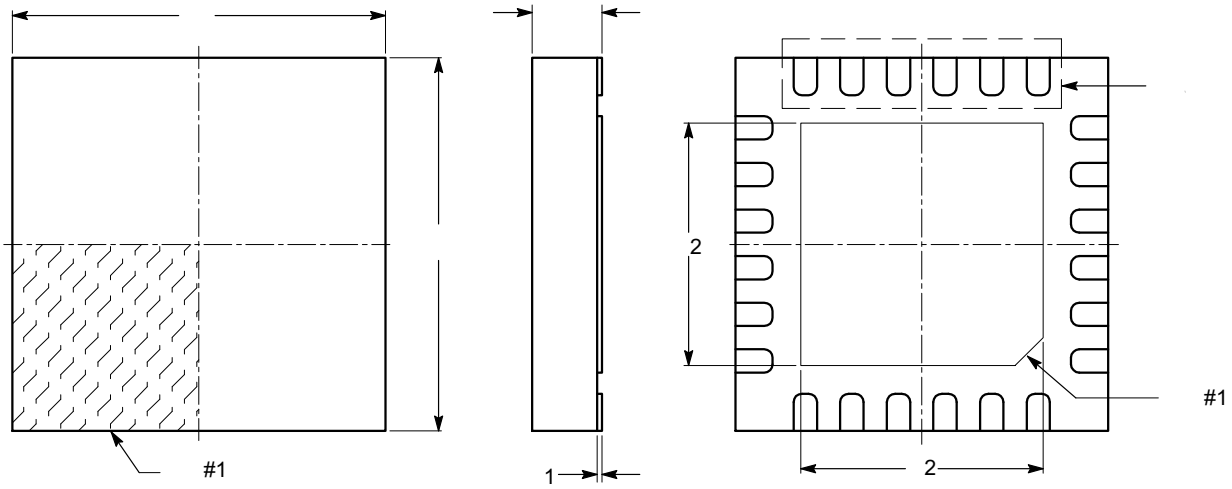
END VIEW

Notes:
(1)
(2) -013.

CAT9555

PACKAGE DIMENSIONS

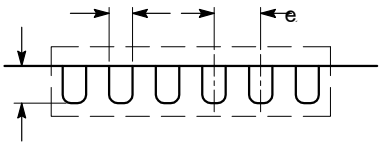
TQFN24, 4x4
CASE 510AG−01
ISSUE B



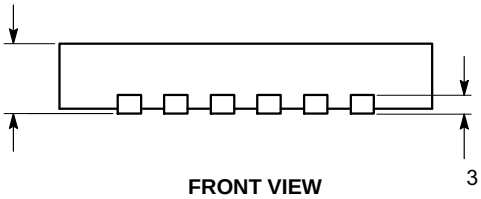
TOP VIEW **SIDE VIEW** **BOTTOM VIEW**

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00		0.05
A3		0.20 REF	
b	0.20	0.25	0.30
D		4.00 BSC	
D2	2.70	2.80	2.90
E		4.00 BSC	
E2	2.70	2.80	2.90
e		0.50 BSC	
L	0.30		0.50

Notes:
(1) e a e e e .
(2) e -220.



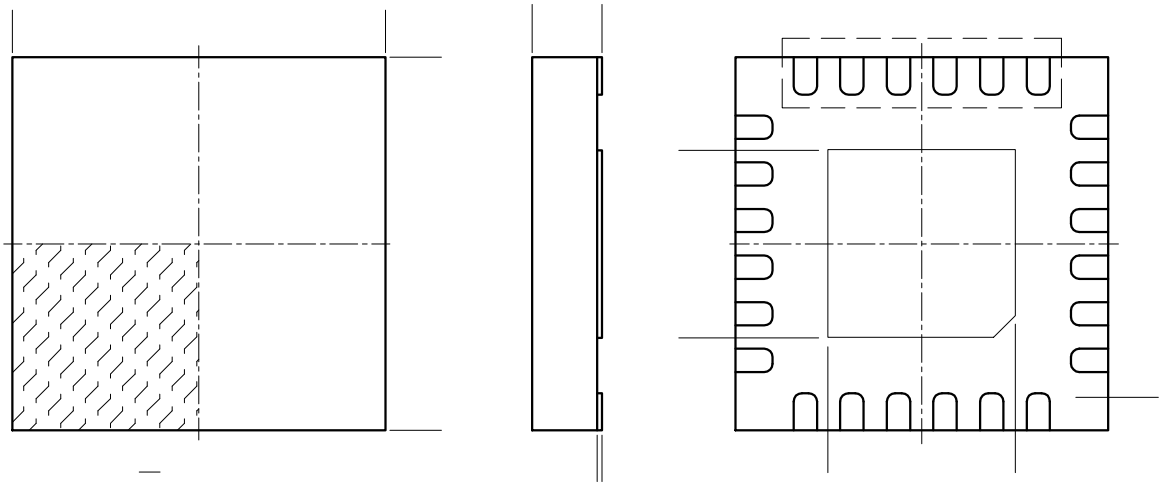
DETAIL A



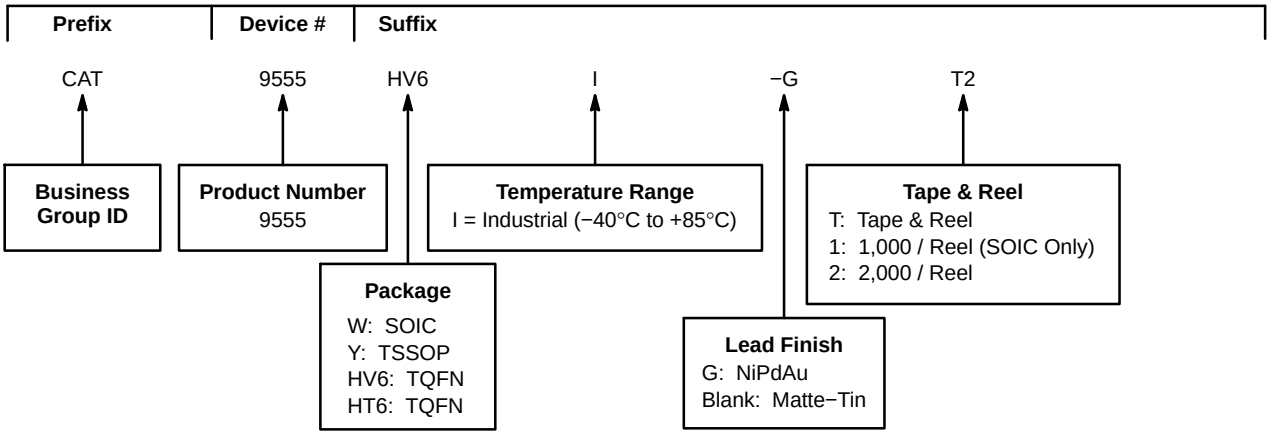
FRONT VIEW

PACKAGE DIMENSIONS

TQFN24, 4x4 TA
CASE 510AN−01
ISSUE O



Example of Ordering Information (Notes 8 to 12)



8. All packages are RoHS−compliant (Lead−free, Halogen−free).
9. The standard lead finish is Matte−Tin for SOIC and TSSOP packages and NiPdAu for TQFN package.
10. The device used in the above example is a CAT9555HV6I−GT2 (TQFN, Industrial Temperature, NiPdAu, Tape & Reel, 2,000/Reel).
11. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
12. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 12. ORDERING PART NUMBER

Part Number	Package	Lead Finish
CAT9555WI	SOIC	Matte−Tin
CAT9555WI−T1	SOIC	Matte−Tin
CAT9555YI	TSSOP	Matte−Tin
CAT9555YI−T2	TSSOP	Matte−Tin
CAT9555HV6I−G	TQFN	NiPdAu
CAT9555HV6I−GT2	TQFN	NiPdAu
CAT9555HT6I−G	TQFN	NiPdAu
CAT9555HT6I−GT2	TQFN	NiPdAu

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