Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Table 5. A.C. CHARACTERISTICS (T_A = −40°C to +125°C) (Note 4)

Symbol	Parameter	V_{CC} = 2.5 V − 5.5 V		Units
		Min	Max	
f_{SCK}	Clock Frequency	DC	10	MHz
t_{SU}	Data Setup Time	10		ns
t_H	Data Hold Time	10		ns
t_{WH}	SCK High Time	40		ns
t_{WL}	SCK Low Time	40		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z		25	ns
t_{RI} (Note 5)	Input Rise Time		2	μs
t_{FI} (Note 5)	Input Fall Time		2	μs
t_{HD}	$\overline{HOLD}$ Setup Time	0		ns
t_{CD}	$\overline{HOLD}$ Hold Time	10		ns
t_V	Output Valid from Clock Low		35	ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		20	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z		25	ns
t_{CS}	$\overline{CS}$ High Time	40		ns
t_{CSS}	$\overline{CS}$ Setup Time	30		ns
t_{CSH}	$\overline{CS}$ Hold Time	30		ns
t_{CNS}	$\overline{CS}$ Inactive Setup Time	20		ns
t_{CNH}	$\overline{CS}$ Inactive Hold Time	20		

Pin Description

SI: The serial data input pin accepts op−codes, addresses and data. In SPI modes (0,0) and (1,1) input data is latched on the rising edge of the SCK clock input.

SO: The serial data output pin is used to transfer data out of the device. In SPI modes (0,0) and (1,1) data is shifted out on the falling edge of the SCK clock.

SCK: The serial clock input pin accepts the clock provided by the host and used for synchronizing communication between host and CAV25320.

$\overline{\text{CS}}$: The chip select input pin is used to enable/disable the CAV25320. When $\overline{\text{CS}}$ is high, the SO output is tri−stated (high impedance) and the device is in Standby Mode (unless

Status Register

The Status Register, as shown in Table 8, contains a number of status and control bits.

The $\overline{\text{RDY}}$ (Ready) bit indicates whether the device is busy with a write operation. This bit is automatically set to 1 during an internal write cycle, and reset to 0 when the device is ready to accept commands. For the host, this bit is read only.

The WEL (Write Enable Latch) bit is set/reset by the WREN/WRDI commands. When set to 1, the device is in a Write Enable state and when set to 0, the device is in a Write Disable state.

The BP0 and BP1 (Block Protect) bits determine which blocks are currently write protected. They are set by the user with the WRSR command and are non−volatile. The user is allowed to protect a quarter, one half or the entire memory, by setting these bits according to Table 9. The protected blocks then become read−only.

The WPEN (Write Protect Enable) bit acts as an enable for the $\overline{\text{WP}}$ pin. Hardware write protection is enabled when the $\overline{\text{WP}}$ pin is low and the WPEN bit is 1. This condition prevents writing to the status register and to the block protected sections of memory. While hardware write protection is active, only the non−block protected memory can be written. Hardware write protection is disabled when the $\overline{\text{WP}}$ pin is high or the WPEN bit is 0. The WPEN bit, $\overline{\text{WP}}$ pin and WEL bit combine to either permit or inhibit Write operations, as detailed in Table 10.

Table 8. STATUS REGISTER

7	6	5	4	3	2	1	0
WPEN	0	0	0	BP1	BP0	WEL	$\overline{\text{RDY}}$

Table 9. BLOCK PROTECTION BITS

Status Register Bits		Array Address Protected	Protection
BP1	BP0		
0	0	None	No Protection
0	1	0C00−0FFF	Quarter Array Protection
1	0	0800−0FFF	Half Array Protection
1	1	0000−0FFF	Full Array Protection

Table 10. WRITE PROTECT CONDITIONS

WPEN	$\overline{\text{WP}}$	WEL	Protected Blocks	Unprotected Blocks	Status Register
0	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	Low	0	Protected	Protected	Protected
1	Low	1	Protected	Writable	Protected
X	High	0	Protected	Protected	Protected
X	High	1			

WRITE OPERATIONS

The CAV25320 device powers up into a write disable state. The device contains a Write Enable Latch (WEL) which must be set before attempting to write to the memory array or to the status register. In addition, the address of the memory location(s) to be written must be outside the protected area, as defined by BP0 and BP1 bits from the status register.

Write Enable and Write Disable

The internal Write Enable Latch and the corresponding Status Register WEL bit are set by sending the WREN instruction to the CAV25320. Care must be taken to take the $\overline{CS}$ input high after the WREN instruction, as otherwise the Write Enable Latch will not be properly set. WREN timing is illustrated in Figure 3. The WREN instruction must be sent prior to any WRITE or WRSR instruction.

The internal write enable latch is reset by sending the WRDI instruction as shown in Figure 4. Disabling write operations by resetting the WEL bit, will protect the device against inadvertent writes.

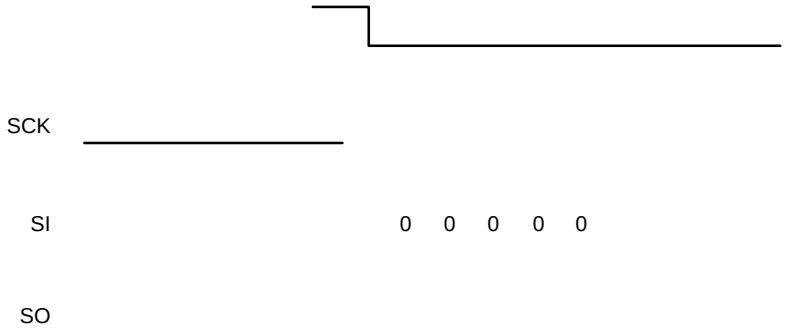

Figure 3. WREN Timing

Byte Write

Once the WEL bit is set, the user may execute a write sequence, by sending a WRITE instruction, a 16−bit address and data as shown in Figure 5. Only 12 significant address bits are used by the CAV25320. The rest are don't care bits, as shown in Table 11. Internal programming will start after the low to high $\overline{CS}$ transition. During an internal write cycle, all commands, except for RDSR (Read Status Register) will be ignored. The $\overline{RDY}$ bit will indicate if the internal write cycle is in progress ($\overline{RDY}$ high), or the device is ready to accept commands ($\overline{RDY}$ low).

Page Write

After sending the first data byte to the CAV25320, the host may continue sending data, up to a total of 32 bytes, according to

Write Status Register

The Status Register is written by sending a WRSR instruction according to timing shown in Figure 7. Only bits 2, 3 and 7 can be written using the WRSR command.

Write Protection

The Write Protect ($\overline{WP}$) pin can be used to protect the Block Protect bits BP0 and BP1 against being inadvertently altered. When $\overline{WP}$ is low and the WPEN bit is set to “1”, write operations to the Status Register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the Status Register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to “0”. The $\overline{WP}$ input timing is shown in Figure 8.

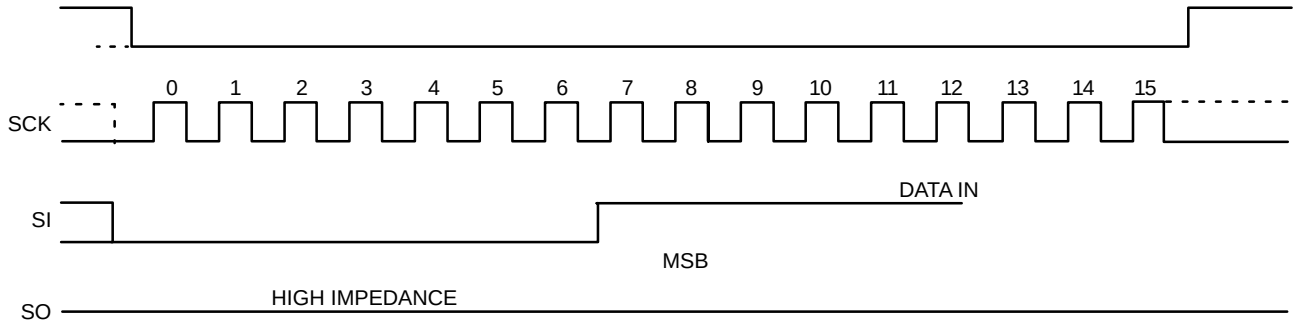

Figure 7. WRSR Timing

READ OPERATIONS

Read from Memory Array

To read from memory, the host sends a READ instruction followed by a 16−bit address (see Table 11 for the number of significant address bits).

After receiving the last address bit, the CAV25320 will respond by shifting out data on the SO pin (as shown in Figure 9). Sequentially stored data can be read out by simply continuing to run the clock. The internal address pointer is automatically incremented to the next higher address as data is shifted out. After reaching the highest memory address, the address counter “rolls over” to the lowest memory address, and the read cycle can be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ high.

Read Status Register

To read the status register, the host simply sends a RDSR command. After receiving the last bit of the command, the CAT25320 will shift out the contents of the status register on the SO pin (Figure 10). The status register may be read at any time, including during an internal write cycle. While the internal write cycle is in progress, the RDSR command will output the full content of the status register. For easy detection of the internal write cycle completion, both during writing to the memory array and to the status register, we recommend sampling the $\overline{RDY}$ bit only through the polling routine. After detecting the $\overline{RDY}$ bit “0”, the next RDSR instruction will always output the expected content of the status register.

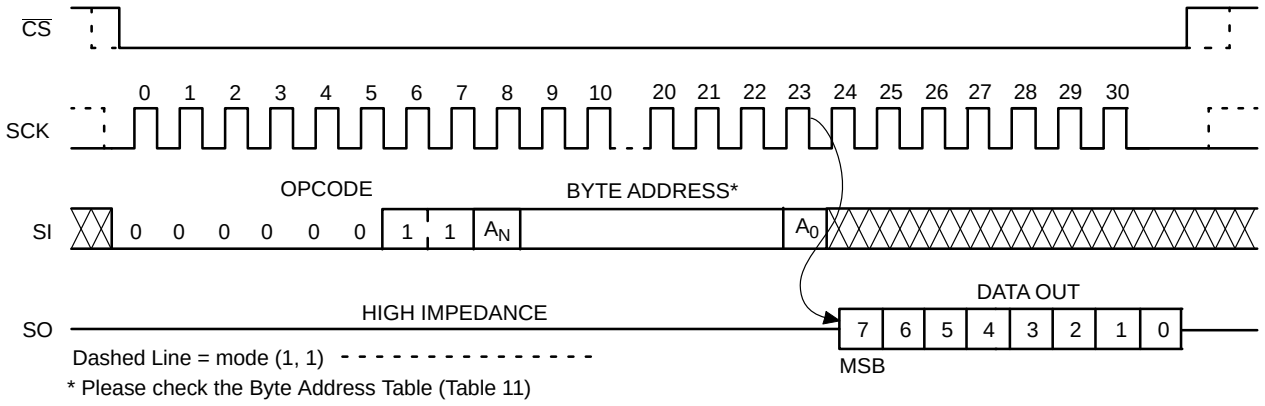

Figure 9. READ Timing

Figure 10. RDSR Timing

Hold Operation

The $\overline{\text{HOLD}}$ input can be used to pause communication between host and CAV25320. To pause, $\overline{\text{HOLD}}$ must be taken low while SCK is low (Figure 11). During the hold condition the device must remain selected ($\overline{\text{CS}}$ low). During the pause, the data output pin (SO) is tri−stated (high impedance) and SI transitions are ignored. To resume communication, $\overline{\text{HOLD}}$ must be taken high while SCK is low.

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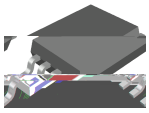

TSSOP8, 4.4x3.0, 0.65P
CASE 948AL
ISSUE A

DATE 20 MAY 2022

3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSI_RS

TOP VIEW

	MILLIMETERS		
DIM	MIN.	NOM.	
A	---		1.20
A1	0.05		0.15
A2			
b	0.19		0.30
c			
D	2.90		3.10
E	6.3		
E1	4.30		4.50
e			
θ			