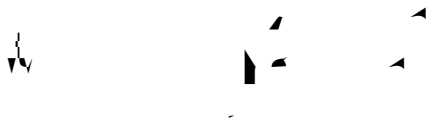
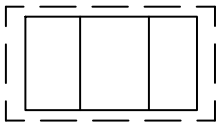


The CM1215 family of diode arrays provides ESD protection for electronic components or sub−systems requiring minimal capacitive loading. These devices are ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the positive (V_P) or negative (V_N) supply rail. The CM1215 protects against ESD pulses up to ±15 kV per the IEC 61000−4−2 standard.

This device is particularly well−suited for protecting systems using high−speed ports such as USB2.0, IEEE1394 (Firewire , iLink™), Serial ATA, DVI, HDMI and corresponding ports in removable storage, digital camcorders, DVD−RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

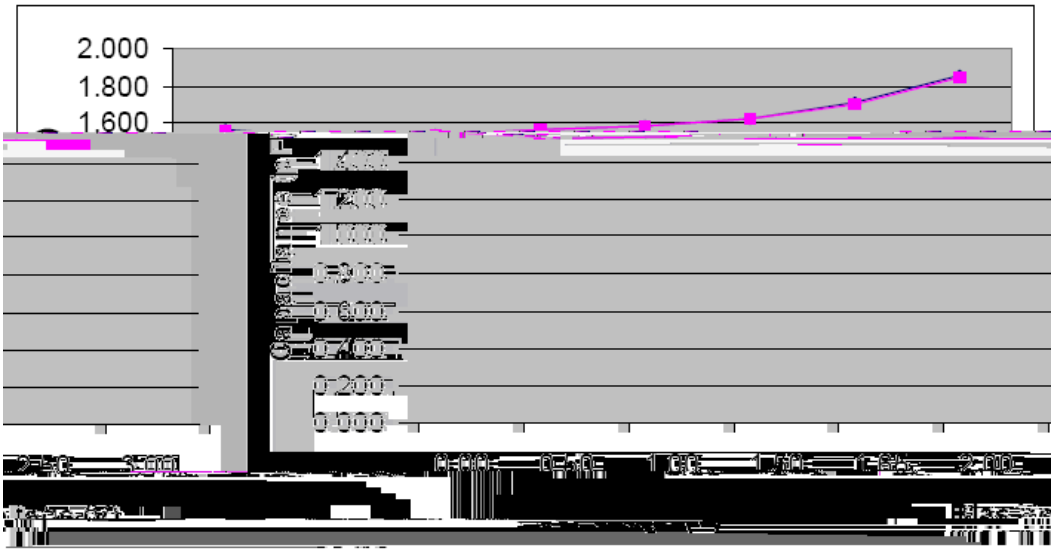
- One, two, and four channels of ESD Protection
- Provides ±15 kV ESD Protection on Each Channel Per the IEC 61000−4−2 ESD Requirements
- Channel Loading Capacitance of 1.6 pF Typical
- Channel I/O to GND Capacitance Difference of 0.04 pF Typical
- Mutual Capacitance of 0.13 pF Typical
- Minimal Capacitance Change with Temperature and Voltage
- Each I/O Pin Can Withstand Over 1000 ESD Strikes
-



Operating Supply Voltage (V_P−V_N)	6	V
Diode Forward DC Current (Note 1)	20	mA
DC Voltage at any Channel Input	(V_N−0.5) to (V_P+0.5)	V
Operating Temperature Range		
Ambient	−40 to +85	°C
Junction	−40 to +125	°C
Storage Temperature Range	−40 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Operating Temperature Range	–40 to +85	°C
Package Power Rating SOT23−3 Package (CM1215−01SO) SOT143 Package (CM1215−02SR) SOT23−5 Package (CM1215−02SO) SOT23−6 Package (CM1215−04SO)	 225 225 225 225	mW



μ

In order to realize the maximum protection against ESD pulses, care must be taken in the PCB layout to minimize parasitic series inductances on the Supply/ Ground rails as well as the signal trace segment between the signal input (typically a connector) and

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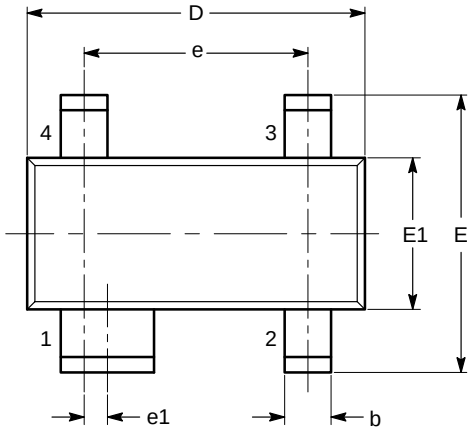
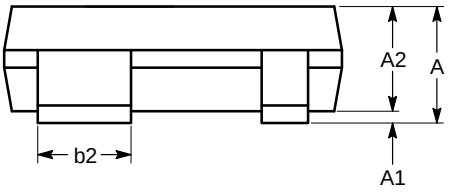
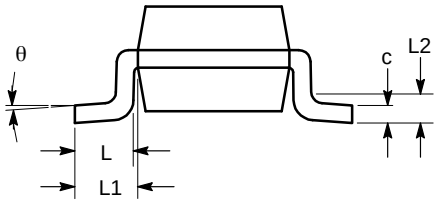
CASE 527AF−01
ISSUE A



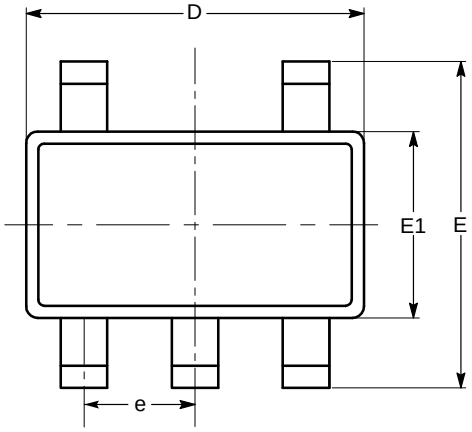
A	0.80		1.22
A1	0.05		0.15
A2	0.75	0.90	1.07
b	0.30		0.50
b2	0.76		0.89
c	0.08		0.20
D	2.80	2.90	3.04
E	2.10		2.64
E1	1.20	1.30	1.40
e	1.92 BSC		
e1	0.20 BSC		
L	0.40	0.50	0.60
L1	0.54 REF		
L2		0.25	
θ	0°		8°



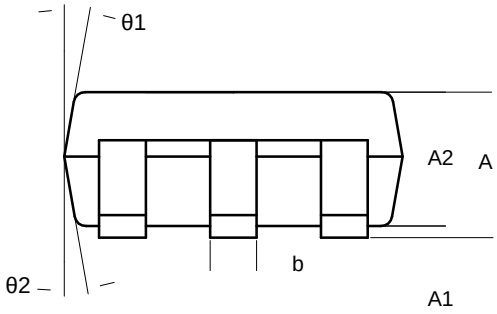


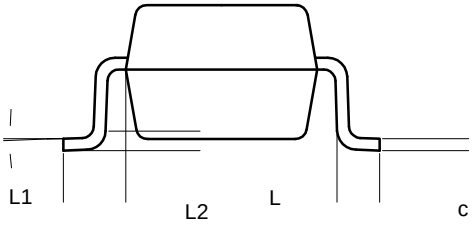
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC TO-253.

CASE 527AH−01
ISSUE O



PIN #1 IDENTIFICATION





(1) All dimensions in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MO-178.