CM1216

6 and 8-Channel Low Capacitance ESD Arrays

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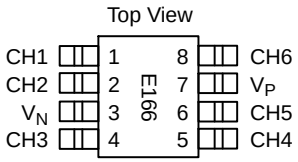
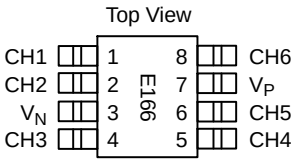
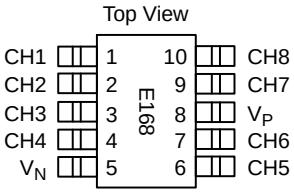
Publication Order Number:



8−Pin SOIC−8



8−Pin MSOP−8



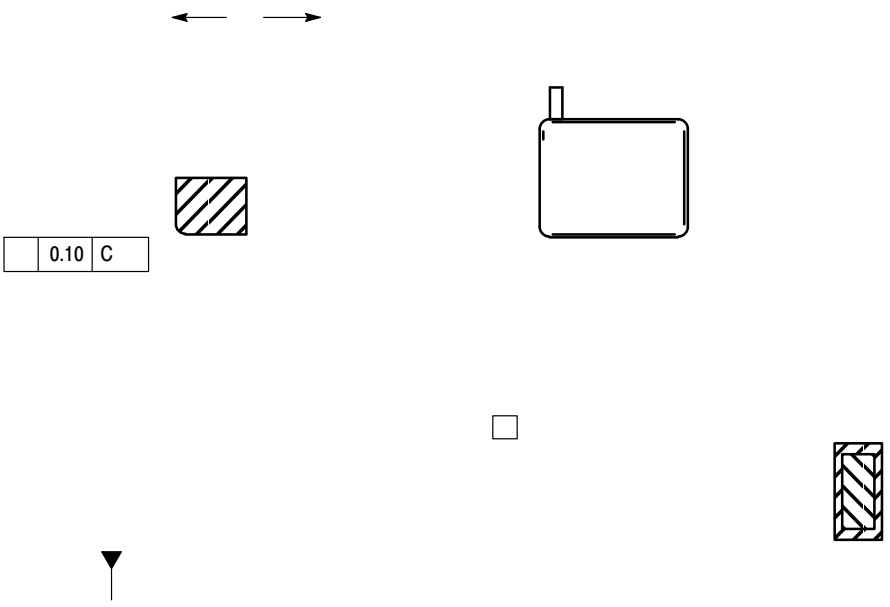
10−Pin MSOP−10

	–	–	–		
CH1	1	1	1	I/O	ESD Channel
CH2	2	2	2	I/O	ESD Channel
CH3	4	4	3	I/O	ESD Channel
CH4	5	5	4	I/O	ESD Channel
V_N	3	3	5	GND	Negative voltage supply rail
CH5	6	6	6	I/O	ESD Channel
CH6	8	8	7	I/O	ESD Channel
V_P	7	7	8	PWR	Positive voltage supply rail
CH7	−	−	9	I/O	ESD Channel
CH8	−	−	10	I/O	ESD Channel

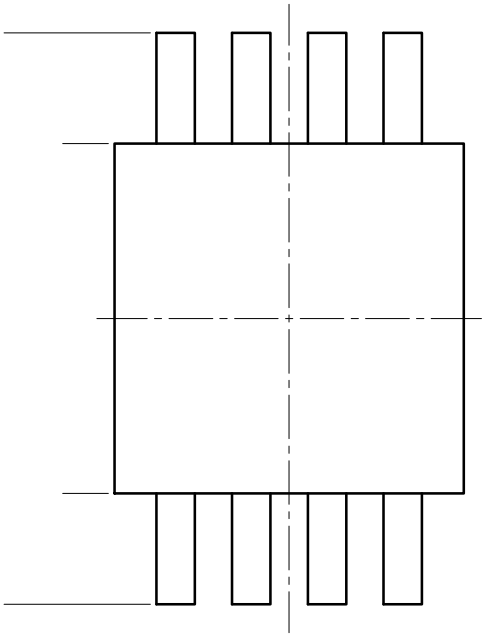
$$V_{CL} = \text{Fwd voltage drop of } D_1 + V_{SUPPLY} + L_1 \times d(I_{ESD}) / dt + L_2 \times d(I_{ESD}) / dt$$

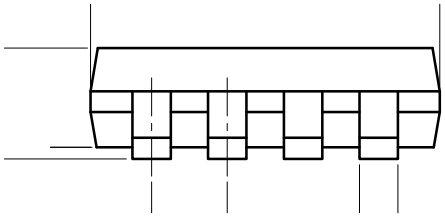
$$\Delta \quad \Delta$$

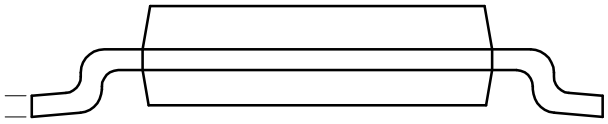
CASE 751AC−01
ISSUE B

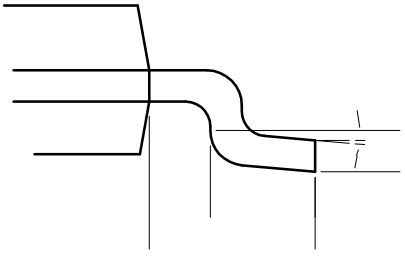
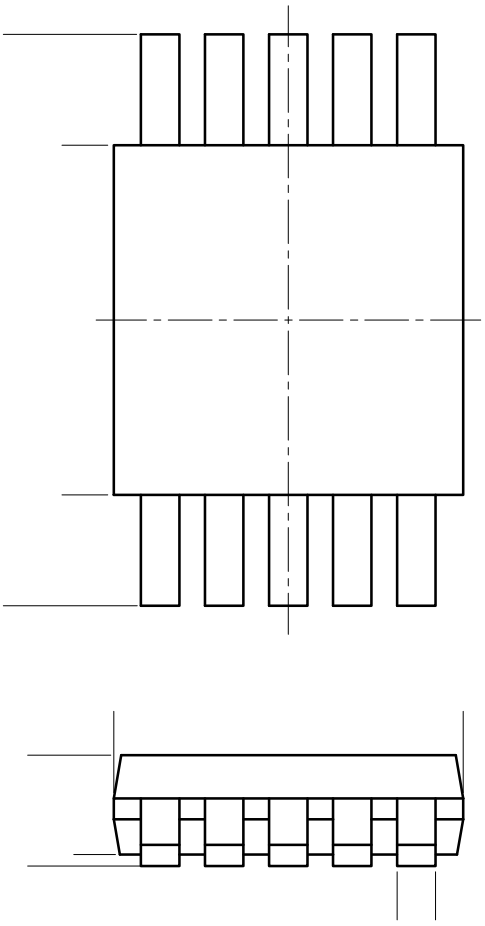
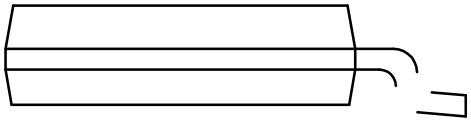


CASE 846AD−01
ISSUE O









CASE 846AE−01
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