

## ESD Clamp Array for High Speed Data Line Protection

### Product Description

The CM1234 is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading and tightly controlled signal skews (with channel-to-channel matching at 2% max deviation).

The device is particularly well-suited for protecting systems using high-speed ports such as DVI or HDMI, along with corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required.

The CM1234 also features easily routed “pass-through” pinouts in a RoHS compliant (lead-free), 16-lead WDFN, small footprint package.

### Features

- ESD Protection for 4 Pairs of Differential Channels
- ESD Protection to IEC61000-4-2 Level 4
  - $\pm 15$  kV Contact Discharge
  - $\pm 20$  kV Air Discharge
- Pass-through Impedance Matched Clamp Architecture
- Flow-through Routing for High-speed Signal Integrity
- Minimal Line Capacitance Change with Temperature and Voltage
- $100 \Omega$  Matched Impedance for Each Paired Differential Channel
- Each I/O Pin can Withstand Over 1000 ESD Strikes\*
- RoHS Compliant (lead-free) WDFN

Figure 1. Block Diagram

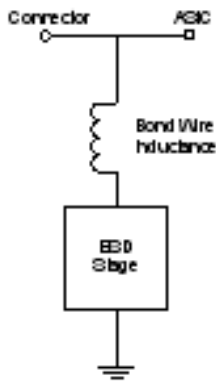
**ESD Protection Architecture**

Conceptually, an ESD protection device performs the following actions upon an ESD strike discharge into a protected ASIC (see Figure 2):

1. When an ESD potential is applied to the system under test (contact or air-discharge), Kirchoff's Current Law (KCL) dictates that the Electrical Overstress (EOS) currents will immediately divide throughout the circuit, based on the dynamic impedance of each path.
2. Ideally, the classic shunt ESD clamp will switch within 1 ns to a low-impedance path and return

**The Architecture Advantages**

Figure 3 illustrates a standard ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.



**Figure 3. Standard ESD Protection Model**

Figure 4 illustrates a standard ESD protection device. The inductor element represents the parasitic inductance arising from the bond wire and the PCB trace leading to the ESD protection diodes.



**Figure 4. CM1234 ESD Protection Model**

**CM1234 Inductor Elements**

In the CM1234 architecture, the inductor elements and ESD protection diodes interact differently compared to the standard ESD model.

In the standard ESD protection device model, the inductive element presents high impedance against high slew rate strike voltage, i.e. during an ESD strike. The impedance increases the resistance of the conduction path

leading to the ESD protection element. This limits the speed that the ESD pulse can discharge through the ESD protection element.

In the architecture, the inductive elements are in series to the conduction path leading to the protected device. The elements actually help to limit the current and voltage striking the protected device.

First the reactance of the inductive element, L1, on the connector side when an ESD strike occurs, acts in the opposite direction of the ESD striking current. This helps limit the peak striking voltage. Then the reactance of the inductive element, L2, on the ASIC side forces this limited ESD strike current to be shunted through the ESD protection diodes. At the same time, the voltage drop across both series element acts to lower the clamping voltage at the protected device terminal.

Through this arrangement, the inductive elements also tune the impedance of the ESD protection element by cancelling the capacitive load presented by the ESD diodes to the signal line. This improves the signal integrity and makes the overall ESD protection device more transparent to the high bandwidth data signals passing through the channel.

The innovative architecture turns the disadvantages of the parasitic inductive elements into useful components that help to limit the ESD current strike to the protected device and also improves the signal integrity of the system by balancing the capacitive loading effects of the ESD diodes. At the same time, this architecture provides an impedance matched signal path for 50 Ω loading applications.

Board designs can take advantage of precision internal component matching for improved signal integrity, which is not otherwise possible with discrete components at the system level. This helps to simplify the PCB layout considerations by the system designer and eliminates the associated passive components for load matching that is normally required with standard ESD protection circuits.

Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to either the Zener diode or to ground. This embedded Zener diode also serves to eliminate the need for a separate bypass capacitor to absorb positive ESD strikes to ground. The CM1234 protects against ESD pulses up to ±18 kv contact per the IEC 61000-4-2 standard.

# CM1234

## PIN DESCRIPTIONS

Pin	Name	Description
1	In_1+	Bidirectional Clamp to ASIC (inside system)
2	In_1-	Bidirectional Clamp to ASIC (inside system)
3	In_2+	Bidirectional Clamp to ASIC (inside system)
4	In_2-	Bidirectional Clamp to ASIC (inside system)
5	In_3+	Bidirectional Clamp to ASIC (inside system)
6	In_3-	Bidirectional Clamp to ASIC (inside system)
7	In_4+	Bidirectional Clamp to ASIC (inside system)
8	In_4-	Bidirectional Clamp to ASIC (inside system)
9	Out_4-	Bidirectional Clamp to Connector (outside system)
10	Out_4+	Bidirectional Clamp to Connector (outside system)
11	Out_3-	Bidirectional Clamp to Connector (outside system)
12	Out_3+	Bidirectional Clamp to Connector (outside system)
13	Out_2-	Bidirectional Clamp to Connector (outside system)
14	Out_2+	Bidirectional Clamp to Connector (outside system)
15	Out_1-	Bidirectional Clamp to Connector (outside system)
16	Out_1+	Bidirectional Clamp to Connector (outside system)
PAD	GND	Ground return to shield

# CM1234

## Specifications

**Table 1. ABSOLUTE MAXIMUM RATINGS**

Parameter	Rating	Units
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Breakdown Voltage (Positive)	6	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 2. ELECTRICAL OPERATING CHARACTERISTICS**

(All parameters specified at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN}$	I/O Voltage Relative to GND		-0.5		5.5	V
$I_{IN}$	Continuous Current through signal pins (IN to OUT) 1000 Hr			100		mA
$I_F$	Channel Leakage Current	$T_A = 25^{\circ}\text{C}; V_N = 0\text{ V}, V_{TEST} = 5\text{ VFF}$				

Performance Information

Graphical Comparison and Test Setup

Figure 5 shows that the CM1234 (ESD protector) lowers the peak voltage and clamping voltage by 45% across a wide range of loading conditions in comparison to a standard ESD protection device. Figure 6 also indicates that the DUP/ASIC protected by the CM1234 dissipates less energy than a standard ESD protection device. This data was derived using the test setups shown in Figure 7.

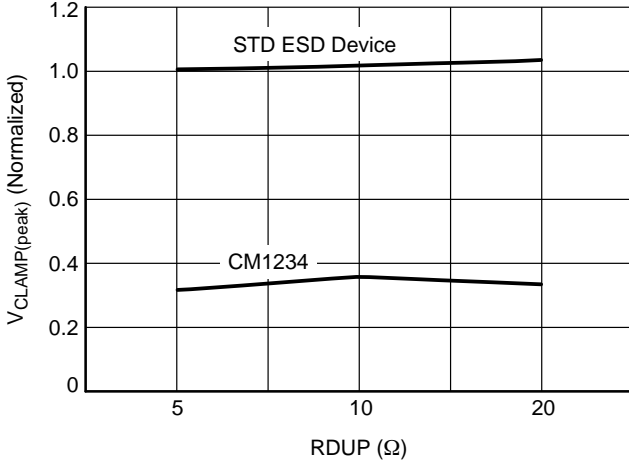


Figure 5. Normalized VPeak (8 KV IEC-61000 4-2 ESD Contact Strike) vs. Loading (RDUP)\*

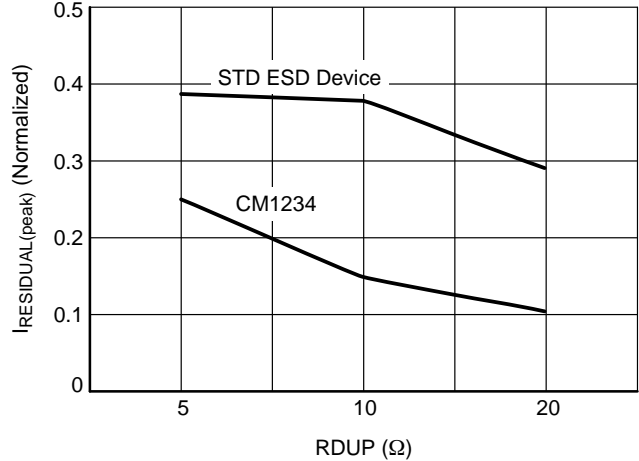


Figure 6. Normalized Residual Current into DUP vs. RDUP\*

\*RDUP is the emulated Dynamic Resistance (load) of the Device Under Protection (DUP).

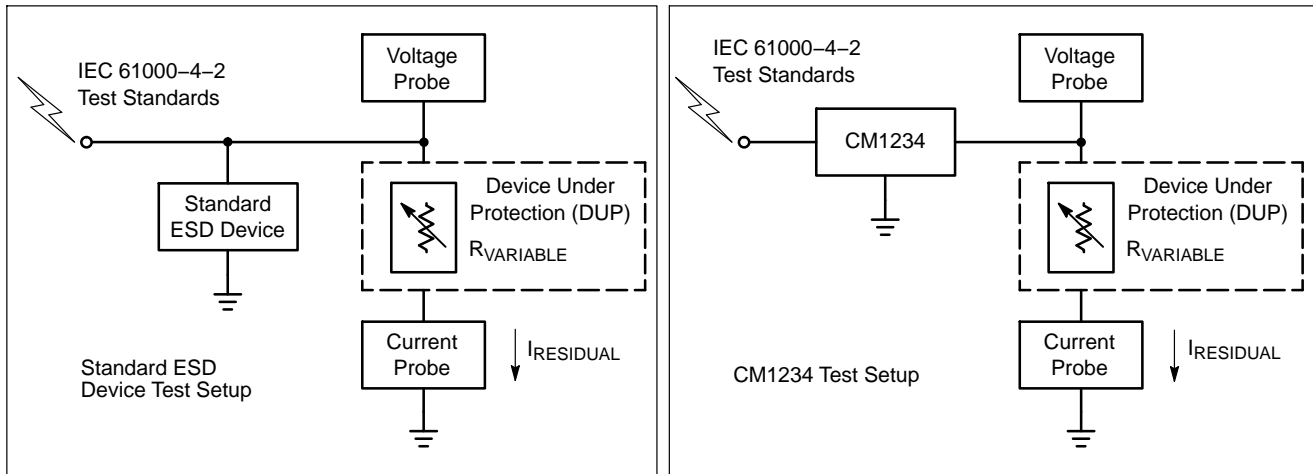
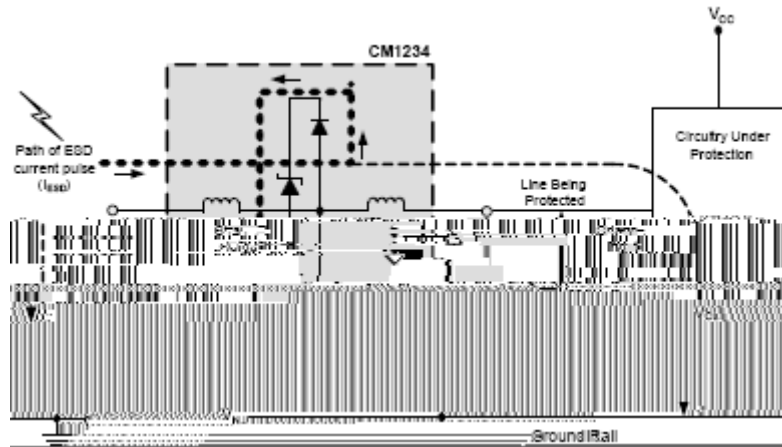


Figure 7. Test Setups: Standard Device (Left) and CM1234 (Right)

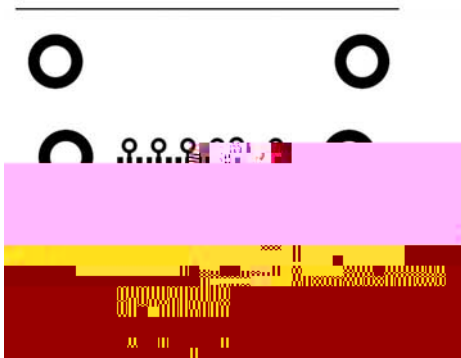
# CM1234

## CM1234 Application and Guidelines

As a general rule, the CM1234 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges with minimum PCB trace lengths to the ground planes and between the signal input and the ESD device to minimize stray series inductance.



**Figure 8. Application of Positive ESD Pulse Between Input Channel and Ground**



**Figure 9. Typical PCB Layout**

### Additional Information

See also ON Semiconductor Application Note “Design Considerations for ESD Protection,” in the Applications section at [www.onsemi.com](http://www.onsemi.com).

# CM1234

## Ordering Information

### PART NUMBERING INFORMATION

Pin	Package	Ordering Part Number (Lead-Free Finish)	Part Marking
16	WDFN-16	CM1234-08DE	CM1234-08

NOTE: Parts are shipped in Tape & Reel form unless otherwise specified.

### TAPE AND REEL SPECIFICATIONS †

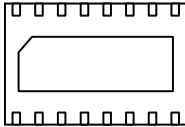
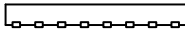
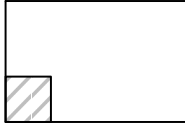
Part Number	Package Size (mm)	Pocket Size (mm) B <sub>0</sub> X A <sub>0</sub> X K <sub>0</sub>	Tape Width W	Reel Diameter	Qty per Reel	P <sub>0</sub>	P <sub>1</sub>
CM1234	6.00 X 4.00 X 0.75	6.30 X 4.30 X 1.10	12 mm	330 mm (13")	3000	4 mm	8 mm



**WDFN16, 6x4, 0.75P**  
**CASE 511AY**  
**ISSUE O**

DATE 21 JUL 2010

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.70	0.80

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