

# CM1443-04CP

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## 4-Channel EMI Filter Array with ESD Protection

### Features

- Four Channels of EMI Filtering for Data Ports
- Pi-Style EMI Filters in a Capacitor-Resistor-Capacitor (C-R-C) Network
- $\pm 15$  kV ESD Protection on Each Channel (IEC 61000-4-2 Level 4, Contact Discharge)
- $\pm 30$  kV ESD Protection on Each Channel (HBM)
- Chip Scale Package (CSP) Features Extremely Low Lead Inductance for Optimum Filter and ESD Performance
- 10-Bump; 0.4 mm Pitch, 1.560 x 1.053 mm Footprint
- <sup>TM</sup> Coating for Improved Reliability at Assembly
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- EMI Filtering and ESD Protection for Both Data and I/O Ports
- Wireless Handsets
- Handheld PCs / PDAs
- MP3 Players
- Notebooks
- Desktop PCs

### BLOCK DIAGRAM

CM1443-

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**Table 4. ELECTRICAL OPERATING CHARACTERISTICS** (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R	Resistance		80	100	120	$\Omega$
C <sub>T</sub>	Total Capacitance	At 2.5 V DC	14	17	21	pF
C <sub>S</sub>	Single Capacitor	At 2.5 V DC		8.5		pF
V <sub>DIODE</sub>	Diode Voltage (reverse bias)	I <sub>DIODE</sub> = 10 $\mu$ A	5.5			V
I <sub>LEAK</sub>	Diode Leakage Current (reverse bias)	V <sub>DIODE</sub> = 3.3 V		0.1	1.0	$\mu$ A
V <sub>SIG</sub>	Signal Voltage Positive Clamp Negative Clamp	I <sub>LOAD</sub> = 10 mA	5.6 -0.4	6.8 -0.8	9.0 -1.5	V
V <sub>ESD</sub>	In-system ESD Withstand Voltage a) Human Body Model, MIL-STD-883, Method 3015 b) Contact Discharge per IEC 61000-4-2 Level 4	(Notes 2 and 4)	$\pm$ 30 $\pm$ 15			kV
V <sub>CL</sub>	Clamping Voltage during ESD Discharge MIL-STD-883 (Method 3015), 8 kV Positive Transients Negative Transients	(Notes 2, 3 and 4)		+10 -5		V
f <sub>C</sub>	Cut-off Frequency Z <sub>SOURCE</sub> = 50 $\Omega$ , Z <sub>LOAD</sub> = 50 $\Omega$	R = 100 $\Omega$ , C <sub>S</sub> = 8.5 pF		220		MHz

1. T<sub>A</sub> = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Clamping voltage is measured at the opposite side of the EMI filter to the ESD pin. For example, if ESD is applied to Pin A1,



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## PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance ( $T_A = 25^\circ\text{C}$ , DC Bias = 0 V, 50  $\Omega$  Environment)

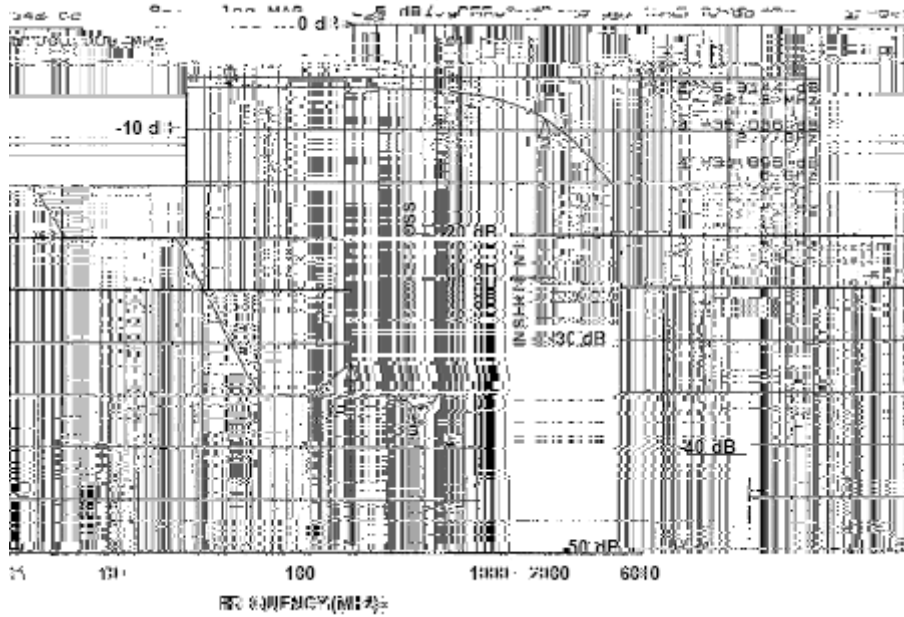


Figure 4. Insertion Loss vs. Frequency (A3-C3 to GND B2)

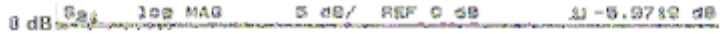


Figure 5. Insertion Loss vs. Frequency (A4-C4 to GND B2)

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## PERFORMANCE INFORMATION (Cont'd)

Typical Filter Performance ( $T_A = 25^\circ\text{C}$ , DC Bias = 0 V, 50  $\Omega$  Environment)

Figure 6. Comparison of Filter Response Curves for CM1443 vs. DC Bias

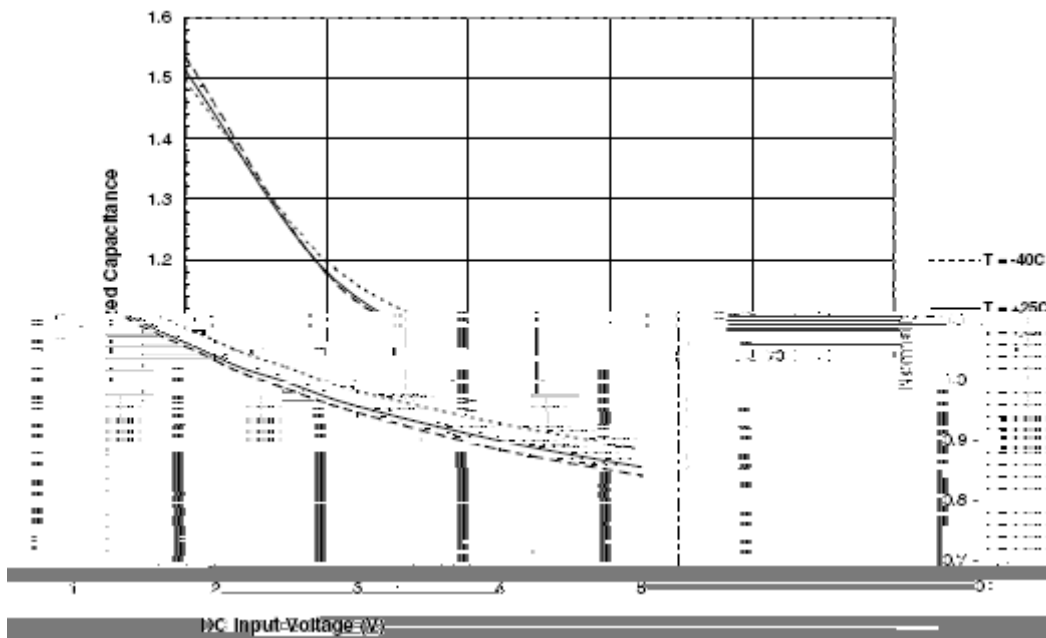
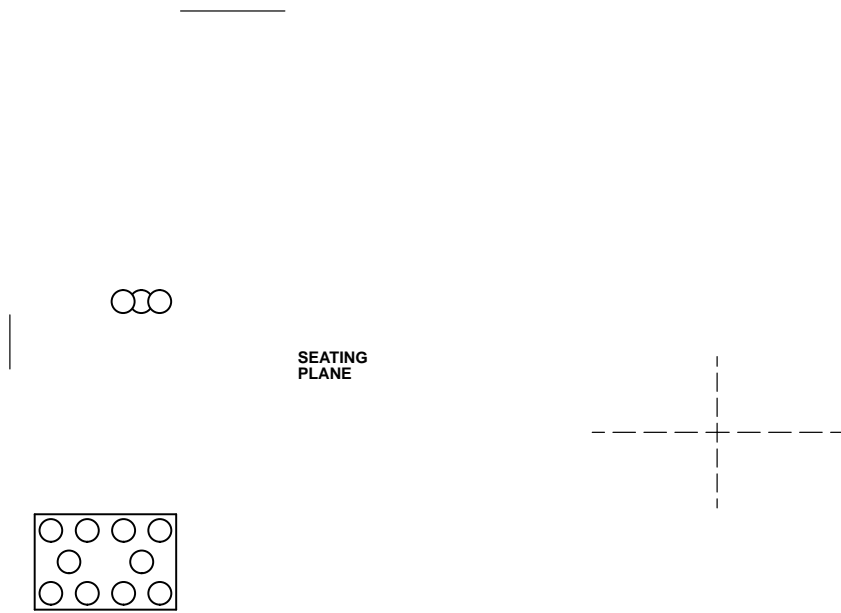


Figure 7. Filter Capacitance vs. Input Voltage over Temperature (normalized to capacitance at 2.5 VDC and 25°C)

WLCSP10, 1.56x1.05



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