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Product Description

The CM3202−00 is a dual−output low noise linear regulator designed to meet SSTL−2 and SSTL−3 specifications for DDR−SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFET's, the CM3202−00 can source up to 2 A of VDDQ continuous current, and source or sink up to 2 A VTT continuous current. The typical dropout voltage for VDDQ is 500 mV

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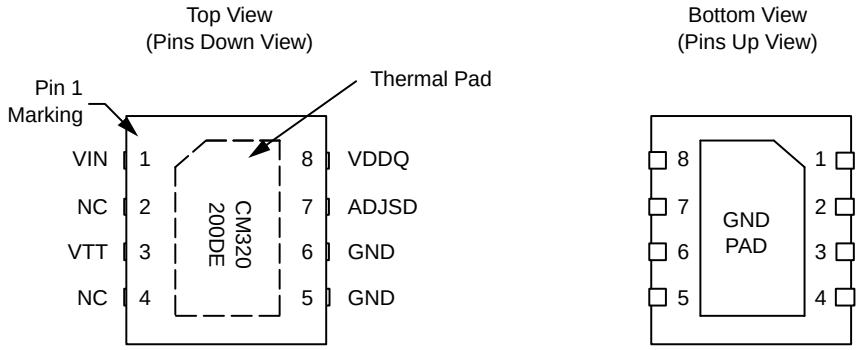
Publication Order Number:
CM3202−00/D

PACKAGE / PINOUT DIAGRAMS



8−Lead WDFN Package
CM3202−00DE

Table 1. PIN DESCRIPTIONS

Lead(s)	Name	Description
1	VIN	Input supply voltage pin. Bypass with a 220 μF capacitor to GND.
2	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
3	VTT	V_{TT} regulator output pin, which is preset to 50% of V_{DDQ}.
4	NC	Not internally connected. For better heat flow, connect to GND (exposed pad).
5	GND	Ground pin (analog).
6	GND	Ground pin (power).
7	ADJSD	This pin is for V_{DDQ} output voltage adjustment. It is available as long as V_{DDQ} is enabled. During Manual/Thermal shutdown, it is tightened to GND. The V_{DDQ} output voltage is set using an external resistor divider connected to ADJSD: $V_{DDQ} = 1.25\ V \times ((R1 + R2) / R2)$ Where R1 is the upper resistor and R2 is the ground−side resistor. In addition, the ADJSD pin functions as a Shutdown pin. When ADJSD voltage is higher than 2.7 V (SHDN_H), the circuit is in Shutdown mode. When ADJSD voltage is below 1.5 V (SHDN_L), both VDDQ and VTT are enabled. A low−leakage Schottky diode in series with ADJSD pin is recommended to avoid interference with the voltage adjustment setting.
8	VDDQ	V_{DDQ} regulator output voltage pin.
EPad	GND	The backside exposed pad which serves as the package heatsink. Must be connected to GND.

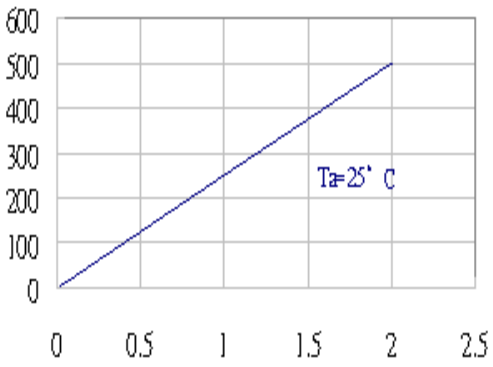
SPECIFICATIONS (Cont'd)

Table 4. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
General						
I_Q	Quiescent Current	I_{DDQ} = 0, I_{TT} = 0		8	15	mA
I_{SHDN}	Shutdown Current	V_{ADJSD} = 3.3 V (Shutdown)		0.1	0.5	mA
SHDN_H	ADJSD Logic High	(Note 2)	2.7			V
SHDN_L	ADJSD Logic Low				1.50	V
UVLO	Under−Voltage Lockout	Hysteresis = 100 mV	2.40	2.70	2.90	V
T_{OVER}	Thermal SHDN Threshold		150	170		°C
T_{HYS}	Thermal SHDN Hysteresis			50		°C
TEMPCO	V_{DDQ}, V_{TT} TEMPCO			150		ppm/°C
VDDQ Regulator						
$V_{DDQ\ DEF}$	VDDQ Output Voltage	I_{DDQ} = 100 mA	2.450	2.500	2.550	V
$V_{DDQ\ LOAD}$	VDDQ Load Regulation	10 mA ≤ I_{DDQ} ≤ 2 A (Note 3)		10	25	mV
$V_{DDQ\ LINE}$	VDDQ Line Regulation	3.1 V ≤ V_{IN} ≤ 3.6 V, I_{DDQ} = 0.1 A		5	25	mV
V_{DROP}	VDDQ Dropout Voltage	I_{DDQ} = 2 A (Note 4)		500		mV
I_{ADJ}	ADJSD Bias Current			0.8	3.0	μA
$I_{DDQ\ LIM}$	VDDQ Current Limit		2.0	2.5		A
VTT Regulator						
$V_{TT\ DEF}$	VTT Output Voltage	I_{TT} = 100 mA	1.225	1.250	1.275	V
$V_{TT\ LOAD}$	VTT Load Regulation	Source, 0 ≤ I_{TT} ≤ 2 A (Note 3) Sink, −2 A ≤ I_{TT} ≤ 0 (Note 3)	 −30	10 −10	30	mV
$V_{TT\ LINE}$	VTT Line Regulation	3.1 V ≤ V_{IN} ≤ 3.6 V, I_{TT} = 0.1 A		5	15	mV
$I_{TT\ LIM}$	ITT Current Limit	Source / Sink (Note 3)	±2.0	±2.5		A
$I_{VTT\ OFF}$	VTT Shutdown Leakage Current	Thermal Shutdown Enabled			10	μA

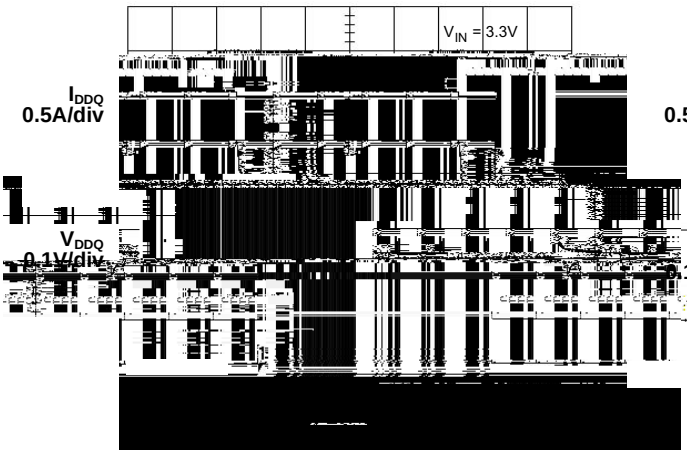
1. V_{IN} = 3.3 V, V_{DDQ} = 2.50 V, V_{TT} = 1.25 V (default values), C_{DDQ} = C_{TT} = 47 μF, T_A = 25°C unless otherwise specified.
2. he SHDN Logic High value is normally satisfied for full input voltage range by using a low leakage current (bellow 1 μA). Schottky diode at ADJSD control pin.
3. Load and line regulation are measured at constant junction temperature by using pulse testing with a low duty cycle. Changes in output voltage due to heating effects must be taken into account separately. Load and line regulation values are guaranteed up to the maximum

TYPICAL OPERATING CHARACTERISTICS

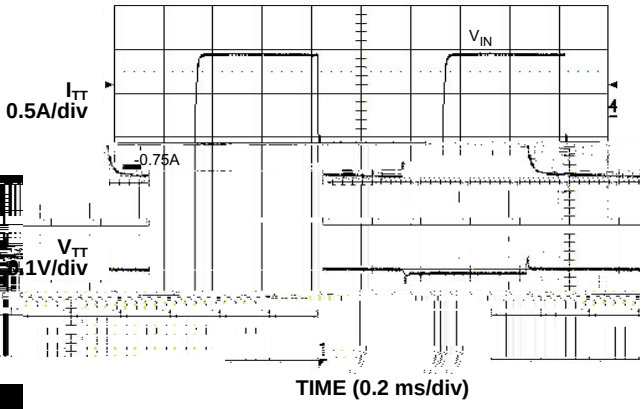


TYPICAL OPERATING CHARACTERISTICS (Cont'd)

VDDQ Transient Response



VTT Transient Response



APPLICATION INFORMATION

Powering DDR Memory

Double−Data−Rate (DDR) memory has provided a huge step in performance for personal computers, servers and graphic systems. As is apparent in its name, DDR operates at double the data rate of earlier RAM, with two memory accesses per cycle versus one. DDR SDRAM's transmit data at both the rising and falling edges of the memory bus clock.

DDR's use of Stub Series Terminated Logic (SSTL) topology improves noise immunity and power−supply rejection, while

APPLICATION INFORMATION (Cont'd)

The VTT power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{405\ mV}{Rt(25\ \Omega)} = 16.2\ mA$$

A typical 64 Mbyte SSTL−2 memory system, with 128 terminated lines, has a worst−case maximum V_{TT} supply current up to ±2.07 A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ±200 mA.

APPLICATION INFORMATION (Cont'd)

Adjusting VDDQ Output Voltage

The CM3202−00 internal bandgap reference is set at 1.25 V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

$$V_{DDQ} = V_{ADJ} \times \frac{R1 + R2}{R2}$$

where V_{ADJ} = 1.25 V. For best regulator stability, we recommend that R_1 and R_2 not exceed 10 kΩ each.

Shutdown

ADJSD also serves as a shutdown pin. When this is pulled high (SHDN_H), both the VDDQ and the VTT outputs tri−state and could sink/source less than 10 μA. During shutdown, the quiescent current is reduced to less than 0.5 mA, independent of output load.

It is recommended that a low leakage Schottky diode be placed between the ADJSD Pin and an external shutdown signal to prevent interference with the ADJ pin's normal operation. When the diode anode is pulled low, or left open, the CM3202−00 is again enabled.

APPLICATION INFORMATION (Cont'd)

PCB Layout Considerations

TheCM3202−00 has a heat spreader attached to the bottom of the WDFN8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad of dimensions just smaller than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during the manufacturing, the heat will be transferred between the two pads. See the Thermal Layout, the CM3202−00 shows the recommended PCB layout. Please be noted that there are four vias on either side to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias can be placed underneath the chip, but this can be resulted in blocking of the solder. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and not near other heat−dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202−00 to ambient, θ_{JA}, of approximately 55°C/W.

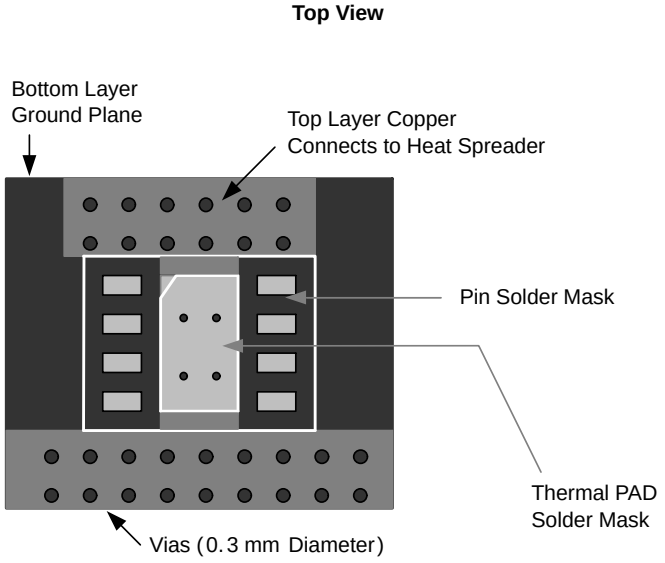
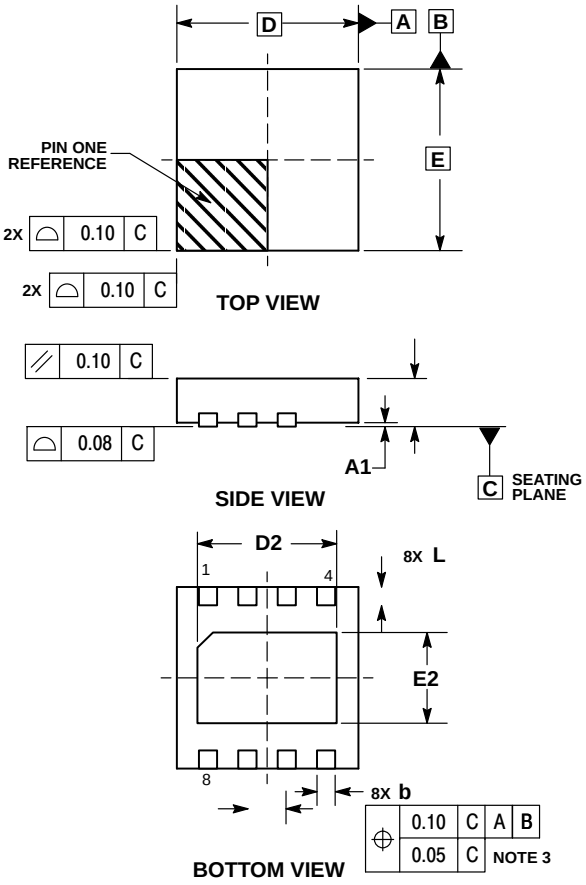


Figure 2. Thermal Layout for WDFN8 Package

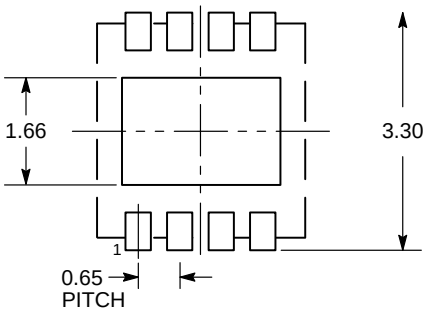
WDFN8 3x3, 0.65P
CASE 511BH
ISSUE O

DATE 21 JUL 2010

SCALE 2:1



SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
b	0.25	0.35
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.40	1.60
e	0.65 BSC	
L	0.20	0.40