DDR VDDQ and VTT Termination Voltage Regulator

Product Description

The CM3202–02 is a dual–output low noise linear regulator designed to meet SSTL–2 and SSTL–3 specifications for DDR–SDRAM V_{DDQ} supply and termination voltage V_{TT} supply. With integrated power MOSFETs the CM3202–02 can source up to 2 A of VDDQ continuous current, and source or sink up to 2 A VTT continuous current. The typical dropout voltage for VDDQ is 500 mV at 2 A load current.

The CM3202–02 provides excellent full load regulation and fast response to transient load changes. It also has built–in over–current limits and thermal shutdown at 170°C.

The CM3202–02 supports Suspend–To–RAM (STR) and ACPI compliance with Shutdown Mode which tri–states VTT to minimize quiescent system current.

The CM3202–02 is available in a space saving WDFN8 surface mount packages. Low thermal resistance allows them to withstand high power dissipation at 85°C ambient. The CM3202–02 can operate over the industrial ambient temperature range of -40°C to 85°C.

Features

- Two Linear Regulators
 - Maximum 2 A Current from VDDQ
 - Source and Sink Up to 2 A VTT Current
- 1.7 V to 2.8 V Adjustable VDDQ Output Voltage
- 0.85 V to 1.4 V VTT Output Voltage (Tracking at 50% of VDDQ)
- 500 mV Typical VDDQ Dropout Voltage at 2 A
- Excellent Load and Line Regulation, Low Noise
- Meets JEDEC DDR-I and DDR-II Memory Power Spec
- Linear Regulator Design Requires no Inductors and Has LowyComponExceCountr Spec

and V_{TT}

- Fast Transient Response
- Low Quiescent Current
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DDR Memory and Active Termination Buses
- Desktop Computers, Servers
- Residential and Enterprise Gateways
- DSL Modems



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WDFN8 DE SUFFIX CASE 511BH

MARKING DIAGRAM



CM320 202DE = CM3202-02DE

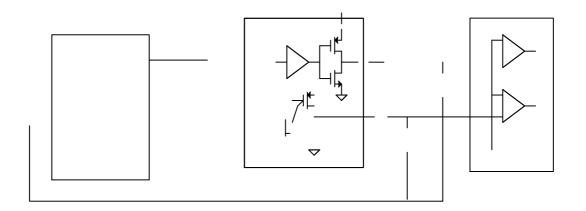
ORDERING INFORMATION

| Device | Package | Shipping [†] |
|-------------|--------------------|-----------------------|
| CM3202-02DE | WDFN8 (Pb-Free) | 3000/Tape & Reel |

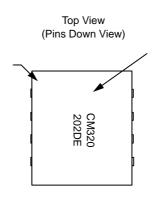
+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

DDQ

- Routers and Switches
- DVD Recorders
- 3D AGP Cards
- LCD TV and STB



PACKAGE / PINOUT DIAGRAMS



SPECIFICATIONS

Table 2. ABSOLUTE MAXIMUM RATINGS

| Parameter | Rating | Units |
|---|--|--------|
| VIN to GND | [GND – 0.3] to +6.0 | V |
| Pin Voltages V _{DDQ} , V _{TT} to GND ADJSD to GND | [GND – 0.3] to +6.0 [GND – 0.3] to +6.0 | V |
| Output Current VDDQ / VTT, continuous (Note 1) VDDQ / VTT, peak VDDQ Source + VTT Source | 2.0/±2.0 2.8/±2.8 3 | A |
| Temperature Operating Ambient Operating Junction Storage | -40 to +85 -40 to +170 -40 to +150 | °C |
| Thermal Resistance, R _{JA} (Note 2) | 55 | °C / W |
| Continuous Power Dissipation (Note 2) WDFN8, $T_A = 25^{\circ}C / 85^{\circ}C$ | 2.6 / 1.5 | W |
| ESD Protection (HBM) | 2000 | V |
| Lead Temperature (soldering, 10 sec) | 300 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

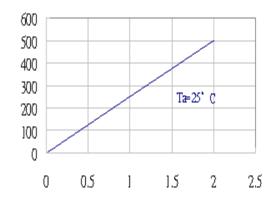
Despite the fact that the device is designed to handle large continuous/peak output currents, it is not capable of handling these under all conditions. Limited by the package thermal resistance, the maximum output current of the device cannot exceed the limit imposed by the maximum power dissipation value.

2. Measured with the package using a 4 in² / 2 layers PCB with thermal vias.

Table 3. STANDARD OPERATING CONDITIONS

| Parameter | Rating | Units | |
|--|------------------------------------|---------------------|--------|
| Ambient Operating Temperature Range | -40 to +85 | °C | |
| VDDQ Regulator Supply Voltage, VIN Load Current, Continuous Load Current, Peak (1 sec) CDDQ to GND3.0 to 3.6 £8 / | 3.0 to 3.6 0 to 2 2.5 220 | V A A220 0.3] | to +6. |

TYPICAL OPERATING CHARACTERISTICS



APPLICATION INFORMATION (Cont'd)

The VTT power requirement is proportional to the number of data lines and the resistance of the termination resistor, but does not vary with memory size. In a typical DDR data bus system each data line termination may momentarily consume 16.2 mA to achieve the 405 mV minimum over V_{TT} needed at the receiver:

$$I_{terminaton} = \frac{0 \ mV}{Rt(2 \ \Omega)} = 1 \ .2 \ mA$$

A typical 64 Mbyte SSTL–2 memory system, with 128 terminated lines, has a worst–case maximum V_{TT} supply current up to ± 2.07 A. However, a DDR memory system is dynamic, and the theoretical peak currents only occur for short durations, if they ever occur at all. These high current peaks can be handled by the V_{TT} external capacitor. In a real memory system, the continuous average V_{TT} current level in normal operation is less than ± 200 mA.

The VDDQ power supply, in addition to supplying current to the memory banks, could also supply current to controllers and other circuitry. The current level typically stays within a range of 0.5 A to 1 A, with peaks up to 2 A or more, depending on memory size and the computing operations being performed.

The tight tracking requirements and the need for V_{TT} to sink, as well as source, current provide unique challenges for powering DDR SDRAM.

CM3202–02 Regulator

The CM3202–02 dual output linear regulator provides all of the power requirements of DDR memory by combining two linear regulators into a single TDFN–8 package. VDDQ regulator can supply up to 2 A current, and the two–quadrant V_{TT} termination regulator has current sink and source capability to ± 2 A. The VDDQ linear regulator uses a PMOS pass element for a very low dropout voltage, typically 500 mV at a 2 A output. The output voltage of V_{DDQ} can be set by an external voltage divider. The use of regulators for both the upper and lower side of the VDDQ output allows a fast transient response to any change of the load, from high current to low current or inversely. The second output, V_{TT} , is regulated at V_{DDQ}

APPLICATION INFORMATION (Cont'd)

Adjusting VDDQ Output Voltage The CM3202–02 internal bandgap reference is set at 1.25 V. The V_{DDQ} voltage is adjustable by using a resistor divider, R1 and R2:

APPLICATION INFORMATION (Cont'd)

PCB Layout Considerations

The CM3202–02 has a heat spreader (exposed pad) attached to the bottom of the WDFN8 package in order for the heat to be transferred more easily from the package to the PCB. The heat spreader is a copper pad with slightly smaller dimensions than the package itself. By positioning the matching pad on the PCB top layer to connect to the spreader during manufacturing, the heat will be transferred between the two pads. Thermal Layout for WDFN8 package shows the CM3202–02 recommended PCB layout. Please note there are four vias to allow the heat to dissipate into the ground and power planes on the inner layers of the PCB. Vias must be placed underneath the chip but this can result in solder blockage. The ground and power planes need to be at least 2 square inches of copper by the vias. It also helps dissipation if the chip is positioned away from the edge of the PCB, and away from other heat–dissipating devices. A good thermal link from the PCB pad to the rest of the PCB will assure the best heat transfer from the CM3202–02 to ambient temperature.

Top View

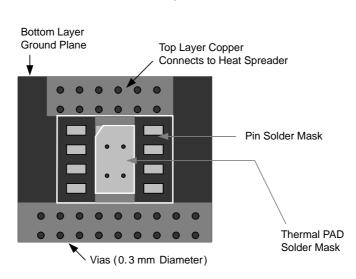
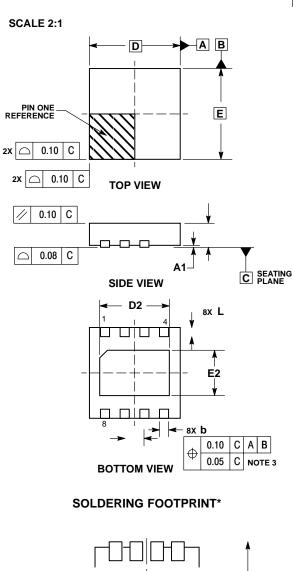
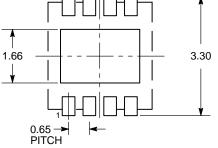


Figure 2. Thermal Layout for WDFN8 Package

WDFN8 3x3, 0.65P CASE 511BH ISSUE O

DATE 21 JUL 2010





*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

- NOTES: 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994. 2. CONTROLLING DIMENSION: MILLIMETERS. 3. DIMENSION 6 APPLIES TO PLATED TERMINAL AND 15 MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP. 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|-----|-------------|------|
| DIM | MIN | MAX |
| Α | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| | | |

| b | 0.25 | 0.35 |
|----|----------|------|
| D | 3.00 BSC | |
| D2 | 2.20 | 2.40 |
| E | 3.00 BSC | |
| E2 | 1.40 | 1.60 |
| е | 0.65 BSC | |
| | | |

L 0.20 0.40

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