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Alternator Voltage Regulator FET Driver

CS3361

The CS3361 integral alternator regulator integrated circuit provides the voltage regulation for automotive, 3–phase alternators.

It drives an external logic level N channel enhancement power FET for control of the alternator field current. In the event of a charge fault, a lamp output pin is provided to drive an external darlington transistor capable of switching on a fault indicator lamp. An overvoltage or no Stator signal condition activates the lamp output.

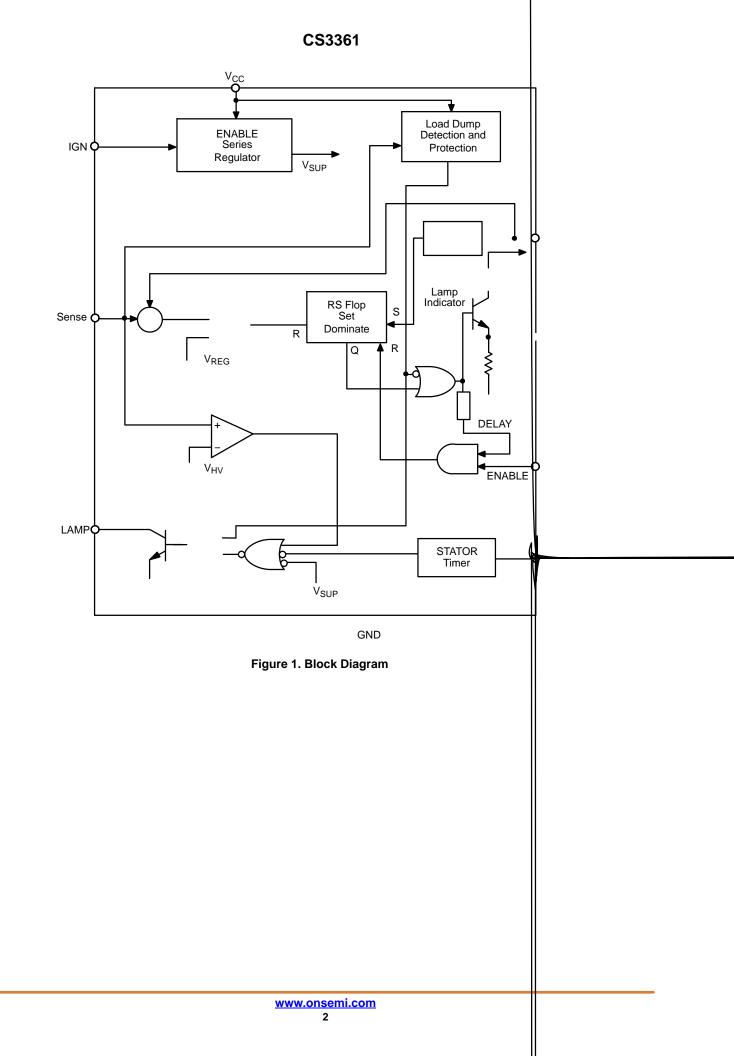
This IC has customized current sense circuitry enabling it to drive FET transistors. The CS3361 is available in an SOIC–14 package.

Features

- Drives Logic Level Power NFET
- 80 V Load Dump
- Temperature Compensated Regulation Voltage
- Shorted Field Protection Duty Cycle, Self Clearing
- This is a Pb-Free Device

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+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.



PACKAGE PIN DESCRIPTION

PIN NO.	PIN SYMBOL	FUNCTION
1	Driver	Output driver for external power switch.
2	GND	Ground.
3, 6, 7, 9, 13	NC	No Connection.
4	OSC	Timing capacitor for oscillator.
5	Lamp	Base driver for lamp driver indicates no stator signal or overvoltage condition.
8	IGN	Switched ignition power up.
10	Stator	Stator signal input for stator timer.
11	Sense	Battery sense voltage regulator comparator input and protection.
12	V _{CC}	Supply for IC.
14	SC	Short circuit sensing.

MAXIMUM RATINGS

Rating	Value	Unit
Storage Temperature Range, T _S	-55 to +165	°C
Junction Temperature Range	-40 to 150	°C
Continuous Supply	27	V
I _{CC} Load Dump (@ V _{CC} = 80 V _{peak})	400	mA
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 1)		°C

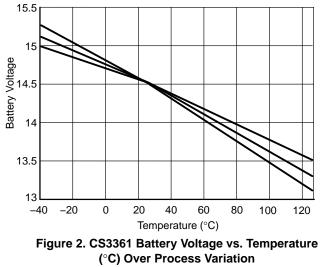
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality alityureliabi

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Characteristic	Test Conditions	Min	Тур	Max	Unit	
Supply	!	I		1	·	
Supply Current Enabled	-	-	-	10	mA	
Supply Current Disabled	-	-	-	50	μΑ	
Driver Stage						
Output High Voltage	-	5.5	-	12	V	
Output Low Voltage	I _{OL} = 25 μA	_	-	0.35	V	
Output High Current	V _{DD} = 1.2 V	-10	-6.0	-4.0	mA	
Minimum ON Time	C _{OSC} = 0.022 μF	200	-	_	μs	
Minimum Duty Cycle	-	-	6.0	10	%	
Short Circuit Duty Cycle	-	1.0	-	5.0	%	
Field Switch Turn On Rise Time	-	15	_	75	μs	
Field Switch Turn On Fall Time	_	15	_	75	μs	
Stator						
Input High Voltage	-	10	-	-	V	
Input Low Voltage	-		-	6.0	V	
Stator Time Out	High to Low	6.0	100	600	ms	
Lamp						
Output High Current	V _{LAMP} @ 3.0 V	_	-	50	μΑ	
Output Low Voltage	I _{LAMP} @ 30 mA	_	-	0.35	V	
Ignition						
Input High Voltage	I _{CC} > 1.0 mA	1.8	-	-	V	
Input Low Voltage	I _{CC} < 100 μA	_	-	0.5	V	
Oscillator						
Oscillator Frequency	C _{OSC} = 0.022 μF	90	-	210	Hz	
Rise Time/Fall Time	$C_{OSC} = 0.022 \mu\text{F}$	-	17	-	-	
Oscillator High Threshold	C _{OSC} = 0.022 μF	-	-	4.5	Vtsl5tt76	. 36 S

$\textbf{ELECTRICAL CHARACTERISTICS} (-40^{\circ}C < T_A < 125^{\circ}C, -40^{\circ}C < T_J < 150^{\circ}C, 9.0 \text{ V} \leq \text{V}_{CC} \leq 17 \text{ V}; \text{ unless otherwise specified.})$

TYPICAL PERFORMANCE CHARACTERISTICS



REGULATION WAVEFORMS

The CS3361 utilizes proportion control to maintain regulation. Waveforms depicting operation are shown in Figures 4, 5 and 6, where $V_{BAT/N}$ is the divided down voltage present on the Sense pin using R1 and R2 (Figure 7). A sawtooth waveform is generated internally. The amplitude of this waveform is listed in the electric parameter section as proportion control. The oscillator voltage is summed with $V_{BAT/N}$, and compared with the internal voltage regulator (V_{REG}) in the regulation comparator which controls the field through the output "Device Driver."

Figure 4 shows typical steady-state operation. A 50% duty cycle is maintained.

Figure 5 shows the effect of a drop in voltage on ($V_{BAT/N}$ + V_{OSC}). Notice the duty cycle increase to the field drive.

Figure 6 shows the effect of an increase in voltage (above the regulation voltage) on ($V_{BAT/N} + V_{OSC}$). Notice the decrease in field drive.

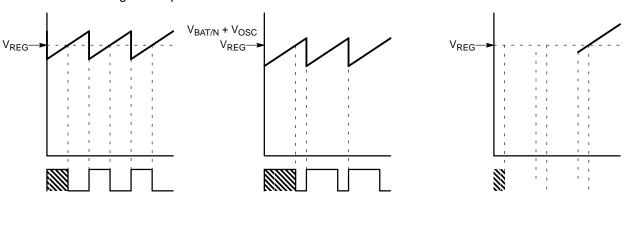


Figure 4. 50% Duty Cycle, Steady State Figure 5. > 50% Duty Cycle, Increased Load

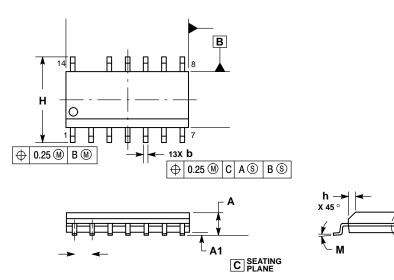
Figure 6. < 50% Duty Cycle, Decreased Load



SOIC 14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016





- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION & DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

SIDE.

GENERIC **MARKING DIAGRAM***

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XXXXX	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

STYLES ON PAGE 2

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STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE

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