5112

1.4 A
5.0 , 100 A
AB

The CS5112 is a dual output power supply integrated circuit. It contains a 5.0 V ± 2%, 100 mA linear regulator, a watchdog timer, a linear output voltage monitor to provide a Power On Reset (POR) and a 1.4 A current mode PWM switching regulator.

The 5.0 V linear regulator is comprised of an error amplifier, reference, and supervisory functions. It has low internal supply current consumption and provides 1.2 V (typical) dropout voltage at maximum load current.

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ELECTRICAL CHARACTERISTICS (5.0 V ≤ V_{IN} ≤ 26 V and −40°C ≤ T_J ≤ 150°C, C_{OUT} = 100 μF (ESR ≤ 8.0 Ω), C_{Delay} = 0.1 μF, R_{BIAS} = 64.9 kΩ, C_{OSC} = 390 pF, C

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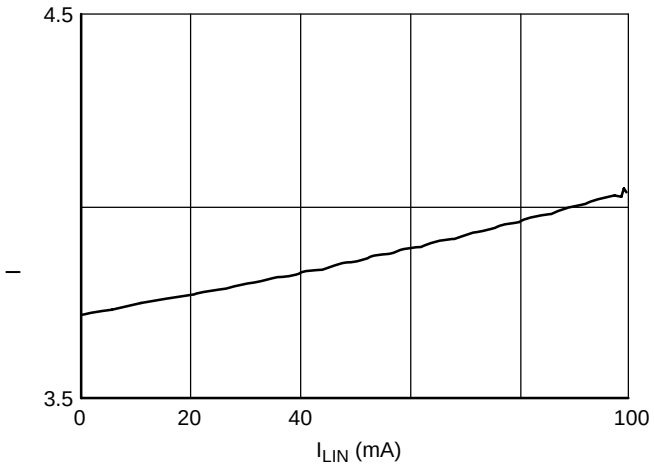
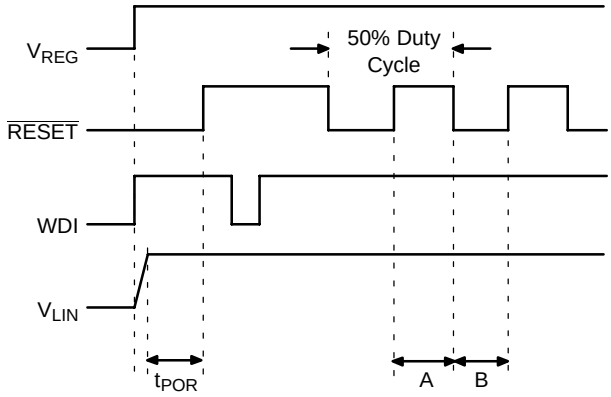
Characteristic	Test Conditions	Min	Typ	Max	Unit
Switcher Section (continued)					
Switcher Max Duty Cycle	V_{SW} = 5.0 V with 50 Ω Load, V_{FB1} = V_{FB2} = 1.0 V	72	85	95	%
Current Sense Amp Gain	I_{SW} = 2.3 A	−	7.0	−	V/V
Error Amp DC Gain	−	−	67	−	dB
Error Amp Transconductance	−	−	2700	−	μA/V
$\overline{\text{ENABLE}}$ Input					
VIL	−	0.8	1.24	−	V
VIH	−	−	1.3	2.0	V
Hysteresis	−	−	60	−	mV
Input Impedance	−	10	20	40	kΩ
Select Input					
VIL (Selects V_{FB1})	4.9 ≤ V_{LIN} ≤ 5.1	0.8	1.25	−	V
VIH (Selects V_{FB2})	4.9 ≤ V_{LIN} ≤ 5.1	−	1.25	2.0	V
SELECT Pullup	SELECT = 0 V	10	24	50	kΩ
Floating Input Voltage	−	3.5	4.5		

TYPICAL PERFORMANCE CHARACTERISTICS



CIRCUIT DESCRIPTION



A: Watchdog waiting for low−going transition on WDI
B: $\overline{RESET}$ stays low for t_{WDI} time

Figure 8. Timing Diagram When WDI Fails to Appear Within the Preset Time Interval, t_{WDI}

The $\overline{RESET}$ signal frequency is given by:

f

CS5112

APPLICATION NOTES

DESIGN PROCEDURE FOR BOOST TOPOLOGY

This section outlines a procedure for designing a boost switching power supply operating in the discontinuous mode.

Step 1

Determine the output power required by the load.

$$P_{OUT} = I_{OUT}V_{OUT} \quad (1)$$

Step 2

Choose C_{OSC} based on the target oscillator frequency with an external resistor value, R_{BIAS} = 64.9 kΩ. (See Figure 5).

Step 3

Next select the output voltage feedback sense resistor

The V_{OUT}/V_{EA} transfer function has a pole at:

$$f_p = 1/(\pi R_{LOAD} C_{OUT}) \quad (14)$$

and a zero due to the output capacitor's ESR at:

$$f_z = 1/(2\pi ESR(C_{OUT})) \quad (15)$$

Since the error amplifier reference voltage is 1.25 V, the output voltage must be divided down or attenuated before being applied to the input of the error amplifier. The feedback resistor divider attenuation is:

$$\frac{1.25\ V}{V_{OUT}}$$

The error amplifier in the CS5112 is an operational transconductance amplifier (OTA), with a gain given by:

$$G_{OTA} = gm Z_{OUT} \quad (16)$$

where:

$$gm = \frac{\Delta I_{OUT}}{\Delta V_{IN}} \quad (17)$$

For the CS5112, gm = 2700 μA/V typical.

One possible error amplifier compensation scheme is shown in Figure 14. This gives the error amplifier a gain plot as shown in Figure 15.

For the error amplifier gain shown in Figure 15, a low frequency pole is generated by the error amplifier output impedance and C_1. This is shown by the line AB with a −20 dB/decade slope in Figure 15. The slope changes to zero at point B due to the zero at:

$$f_z = 1/(2\pi R_4 C_1) \quad (18)$$

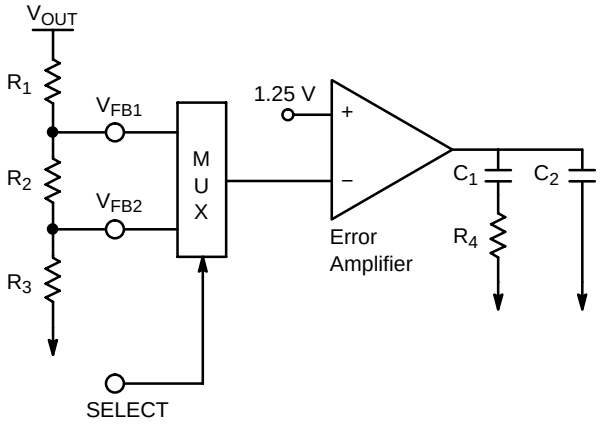


Figure 14. RC Network Used to Compensate the Error Amplifier (OTA)

A pole at point C:

$$f_p = 1/(\pi R_4 C_2) \quad (19)$$

offsets the zero set by the ESR of the output capacitors.

An alternative scheme uses a single capacitor as shown in Figure 16, to roll the gain off at a relatively low frequency.

Step 9

Finally the watchdog timer period and Power on Reset time is determined by:

$$t_{Delay} = 1.353 \times C_{Delay} R_{BIAS} \quad (20)$$

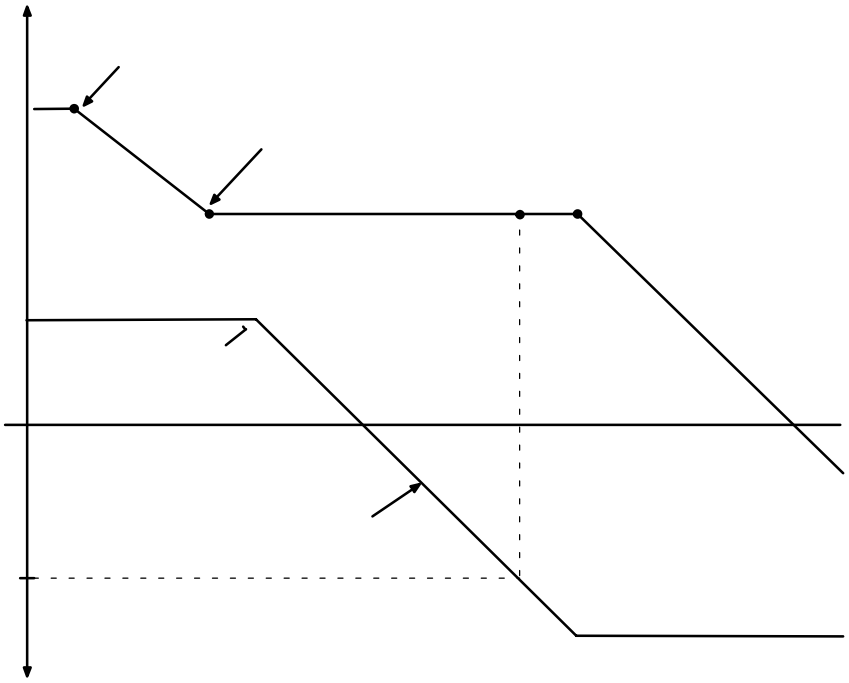
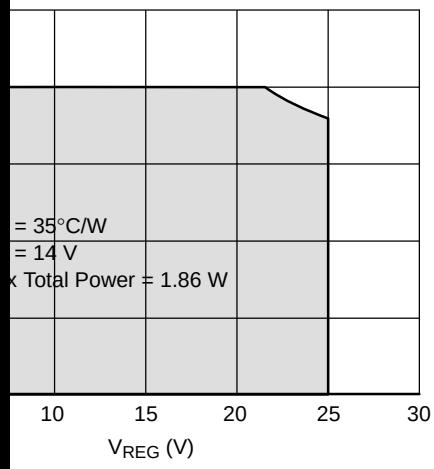


Figure 15. Bode Plot of Error Amplifier (OTA) Gain and Modulator Gain Added to the Feedback Resistor Divider AttenuationcB*248.4 309. 7h3(9).970.h 28/F2dn40 29 6297h3(9).448.44

UT VOLTAGE



CS5112 as a Function of and Voltages.

Table 1.

V_{REG} (V)	V_{IN} (V)	I_{LIN} (mA)	Linear Power Dissipation (W)	Worst Case Switcher Power Available (θ_{JA} = 55°C/W) (W)	Worst Case Switcher Power Available (θ_{JA} = 35°C/W) (W)
20	14	25	0.44	0.74	1.42
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
20	14	75	1.22		