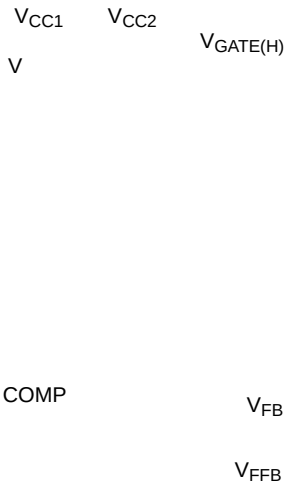


Figure 1. Application Diagram, Switching Power Supply for Core Logic − Pentium® II Processor

05 ref46.8 0 52 27. 16.52..96 Tm(1 8 0T59.76 550.56 0.36 164386966516136 582.52 29.8

ELECTRICAL CHARACTERISTICS (0

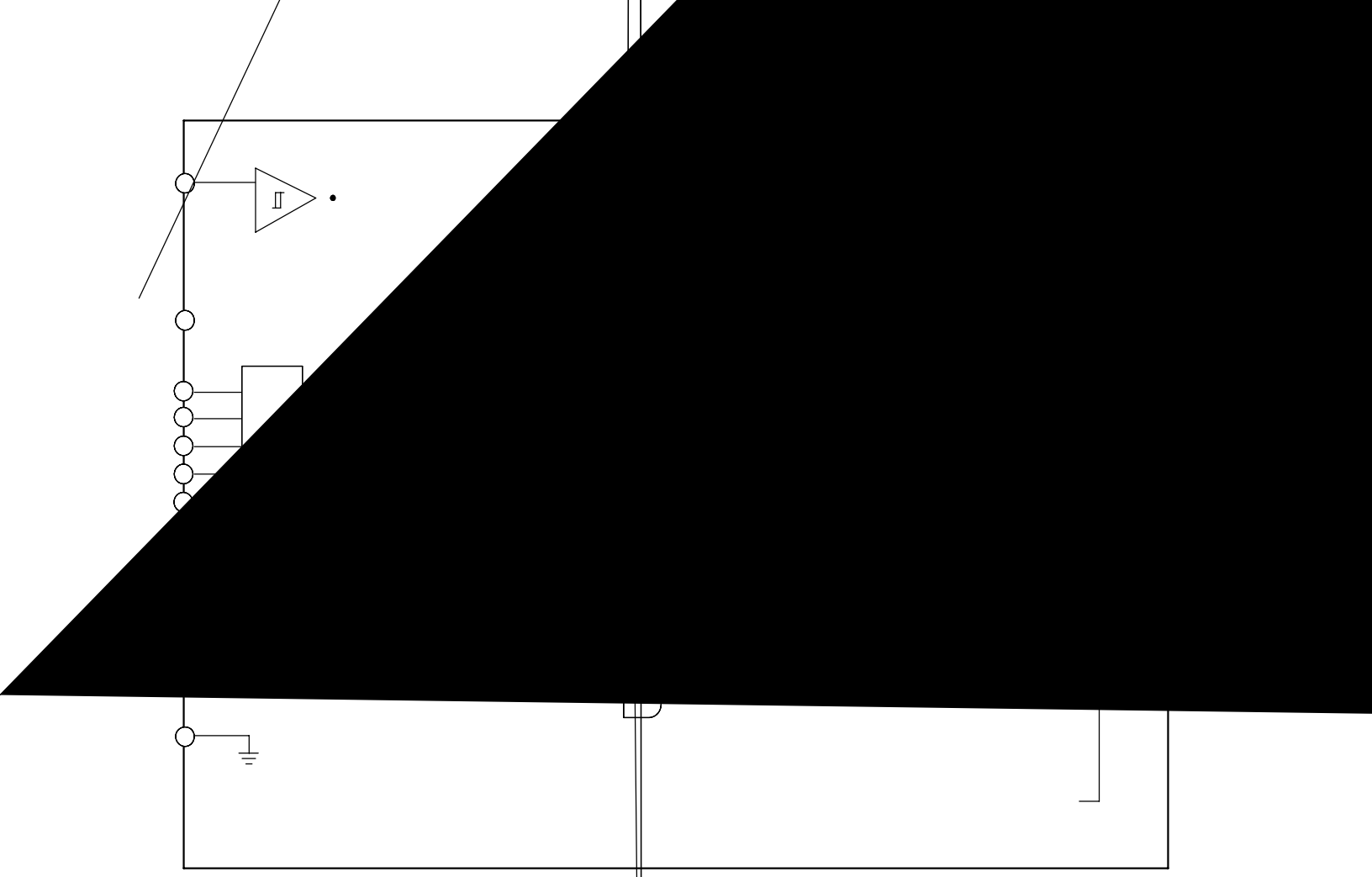


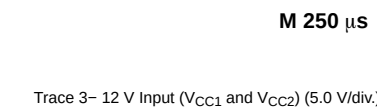
Figure 2. Block Diagram

The V^2 control method is illustrated in Figure 3. The output voltage is used to generate both the error signal and the ramp signal. Since the ramp signal is simply the output voltage, it is affected by any change in the output regardless of the origin of that change. The ramp signal also contains the DC portion of the output voltage, which allows the control circuit to drive the main switch to 0% or 100% duty cycle as required.

A change in line voltage changes the current ramp in the inductor, affecting the ramp signal, which causes the V^2 control scheme to compensate the duty cycle. Since the change in inductor current modifies the ramp signal, as in current mode control, the V^2 control scheme has the same advantages in line transient response.

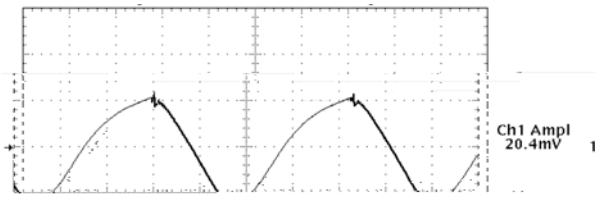
A change in load current will have an affect on the output voltage, altering the ramp signal. A load step immediately changes the state of the comparator output, which controls the main switch. Load transient response is determined only by the comparator response time and the transition speed of the main switch. The reaction time to an output load step has no relation to the crossover frequency of the error signal loop, as in traditional control methods.

The error signal loop can have a low crossover frequency, since transient response is handled by the ramp signal loop. The main purpose of this ‘slow’ feedback loop is to provide DC accuracy. Noise immunity is significantly improved, since the error amplifier bandwidth can be rolled off at a low frequency. Enhanced noise immunity improves main-23s728 Tw[t023023a.2(e19.8(s)-16TD-0.n)(y)17.22e27(i)c0.0023 Tw,-3.Hc-0.TD-0.n50.02-



Trace 3− 12 V Input (V_{CC1} and V_{CC2}) (5.0 V/div.)

Figure 4. CS5157H Demonstration Board Startup in Response to Increasing 12 V and 5.0 V Input Voltages. Extended Off Time is Followed by Normal Off Time Operation when Output Voltage Achieves Regulation to the Error Amplifier Output.



M 1.00 μs

Trace 1− Regulator Output Voltage (10 mV/div.)
Trace 2− Inductor Switching Node (5.0 V/div.)

Figure 8. Peak−to−Peak Ripple on V_{OUT} = 2.8 V, I_{OUT} = 13 A (Heavy Load)

Transient Response

The CS5157H V^2 control loop's 100 ns reaction time provides unprecedented transient response to changes in input voltage or output current. Pulse by pulse adjustment of duty cycle is provided to quickly ramp the inductor current

Short Circuit Protection

A lossless hiccup mode short circuit protection feature is provided, requiring only the Soft−Start capacitor to implement. If a short circuit condition occurs (V_{FFB} < 1.0 V), the V_{FFB} low comparator sets the FAULT latch. This causes the MOSFET to shut off, disconnecting the regulator from it's input voltage. The Soft−Start capacitor is then slowly discharged by a 2.0

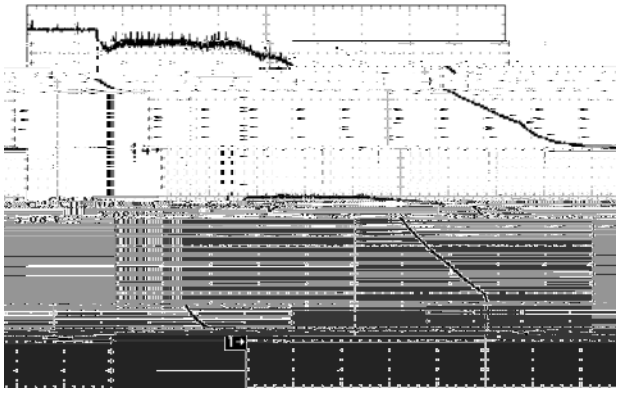


Figure 15. OVP Response to an Input−to−Output Short Circuit by Pulling the Input Voltage to Ground

External Output Enable Circuit

On/off control of the regulator can be implemented through the addition of two additional discrete components (see Figure 16). This circuit operates by pulling the Soft−Start pin high, and the V_{FFB} pin low, emulating a short circuit condition.

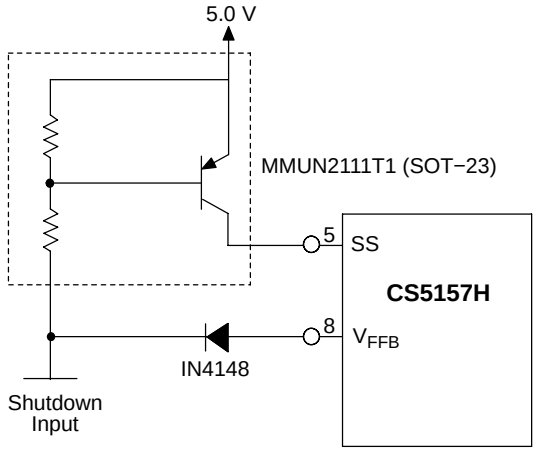


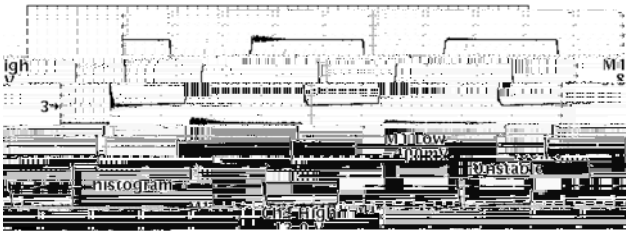
Figure 16. Implementing Shutdown with the CS5157H

External Power Good Circuit

An optional Power Good signal can be generated through the use of four additional external components (see

capacitive load they present to the controller IC. For the typical application where $V_{CC1} = V_{CC2} = 12$ V and 5.0 V is used as the source for the regulator output current, the following gate drive is provided;

$V_{GATE(H)} = 12\ V - 5.0\ V = 7.0\ V,\ V_{GATE(L)} = 12\ V$ (see Figure 19.)



M 1.00 μs

Trace 3 = $V_{GATE(H)}$ (10 V/div.)
Math 1 = $V_{GATE(H)} - 5.0\ V_{IN}$
Trace 4 = $V_{GATE(L)}$ (10 V/div.)
Trace 2− Inductor Switching Nodes (5.0 V/div.)

Figure 19. CS5157H Gate Drive Waveforms Depicting Rail to Rail Swing

The most important aspect of MOSFET performance is RDS_{ON}, which effects regulator efficiency and MOSFET thermal management requirements.

A heatsink may be added to TO−220 components to reduce their thermal impedance. A number of PC board layout techniques such as thermal vias and additional copper foil area can be used to improve the power handling capability of surface mount components.

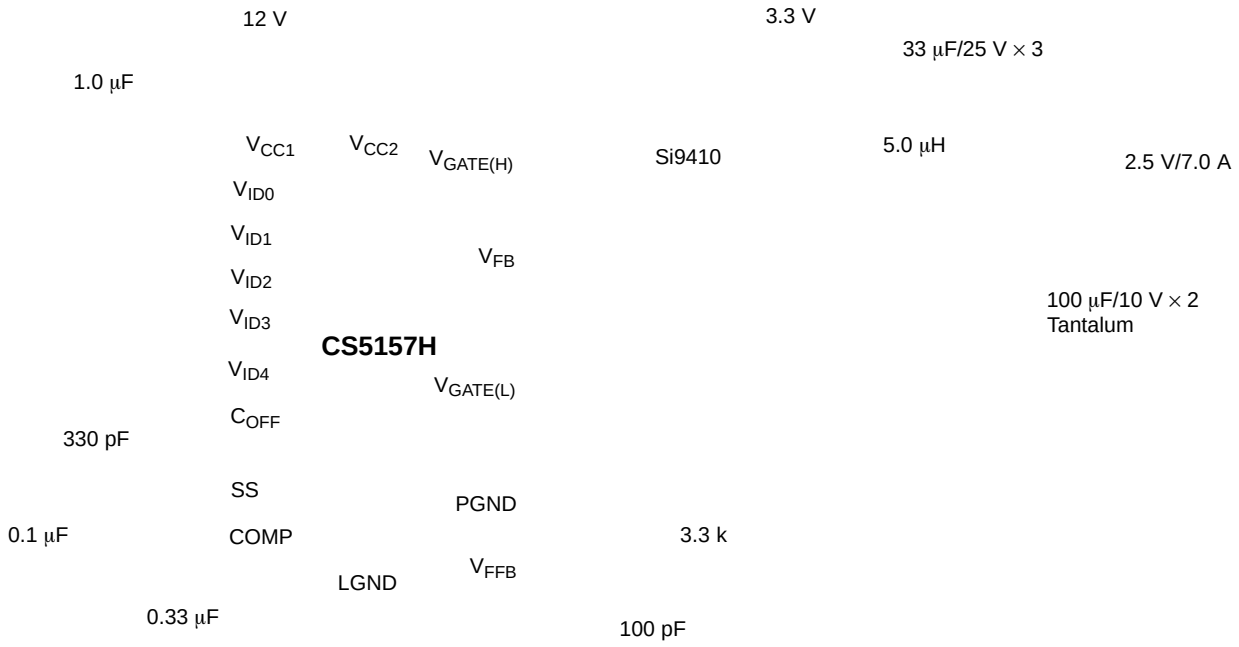

12 V
1.0 μF
3.3 V
33 μF/25 V × 3
5.0 μH
2.5 V/7.0 A
100 μF/10 V × 2
Tantalum
Si9410
VCC1
VCC2
VGATE(H)
VID0
VID1
VID2
VID3
VID4
COFF
330 pF
SS
0.1 μF
COMP
0.33 μF
VFB
CS5157H
VGATE(L)
PGND
LGND
VFFB
3.3 k
100 pF

Figure 25. Additional Application Diagram, 5.0 V to 3.3 V/10 A Converter with Current Sharing

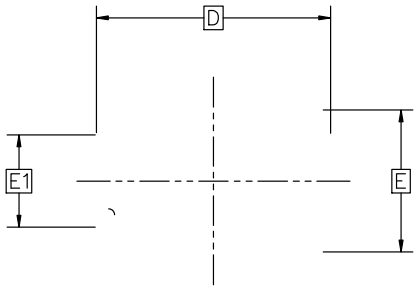
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE

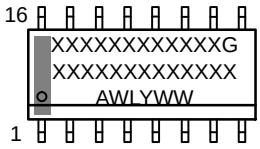


TOP VIEW

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

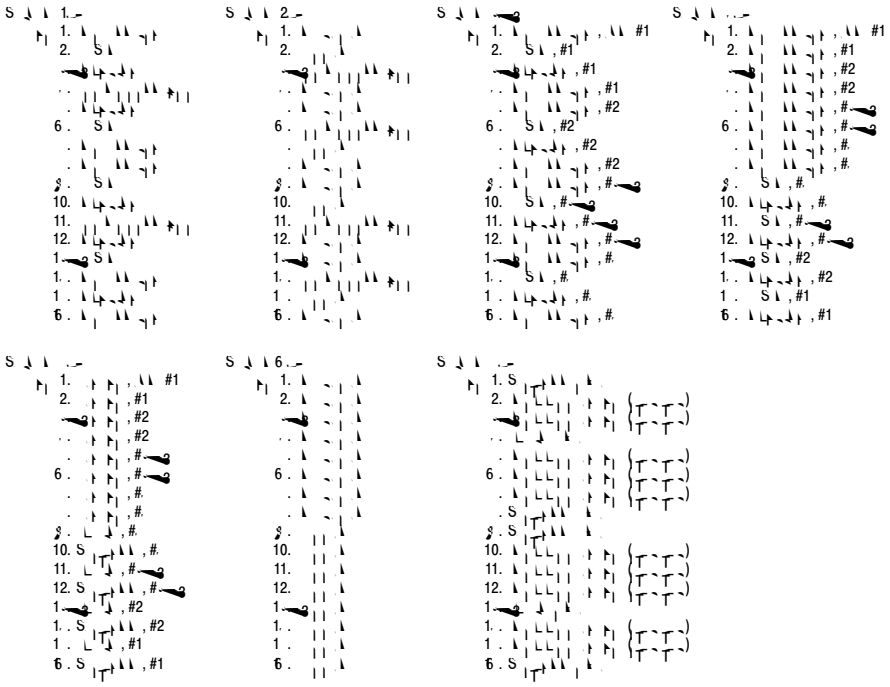
DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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