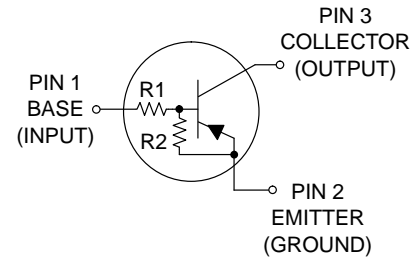
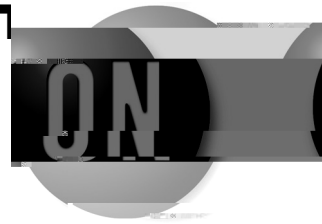


# M (1)TT3 TDN2T4 SS,NLT T(DT)N1

# ITDN2T4 5



		<b>5</b>	
<b>olltor</b> –Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current – Continuous	$I_C$	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	40	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	10	Vdc

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.



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Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1) (Note 2)	$P_D$	246 400	mW
Derate above $25^\circ\text{C}$	(Note 1) (Note 2)		2.0 3.2	
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$	508 311	$^\circ\text{C/W}$
Thermal Resistance, Junction to Lead	(Note 1) (Note 2)	$R_{\theta JL}$	174 208	$^\circ\text{C/W}$
Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

- -

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1) (Note 2)	$P_D$	202 310	mW
Derate above $25^\circ\text{C}$	(Note 1) (Note 2)		1.6 2.5	
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$	618 403	$^\circ\text{C/W}$
Thermal Resistance, Junction to Lead	(Note 1) (Note 2)	$R_{\theta JL}$	280 332	$^\circ\text{C/W}$
Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

-

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1) (Note 2)	$P_D$	200 300	mW
Derate above $25^\circ\text{C}$	(Note 1) (Note 2)		1.6 2.4	
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$	600 400	$^\circ\text{C/W}$
Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

-

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 1) (Note 2)	$P_D$	260 600	mW
Derate above $25^\circ\text{C}$	(Note 1) (Note 2)		2.0 4.8	
Thermal Resistance, Junction to Ambient	(Note 1) (Note 2)	$R_{\theta JA}$	480 205	$^\circ\text{C/W}$
Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

-

Total Device Dissipation $T_A = 25^\circ\text{C}$	(Note 3) (Note 4)	$P_D$	
Derate above $25^\circ\text{C}$	(Note 3) (Note 4)		



(T<sub>A</sub> = 25°C, unless otherwise noted)

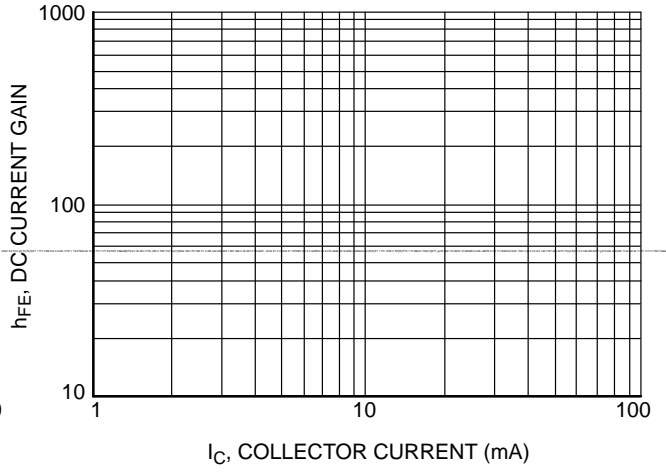
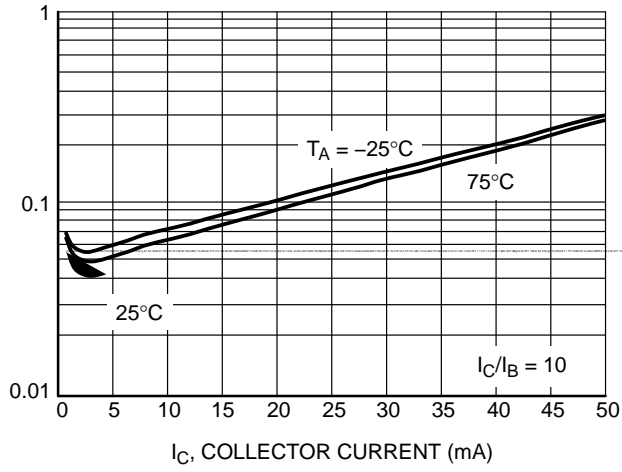
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Collector–Base Cutoff Current (V <sub>CB</sub> = 50 V, I <sub>E</sub> = 0)	I <sub>CBO</sub>	–	–	100	nAdc
Collector–Emitter Cutoff Current (V <sub>CE</sub> = 50 V, I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	500	nAdc
Emitter–Base Cutoff Current (V <sub>EB</sub> = 6.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	0.13	mAdc
Collector–Base Breakdown Voltage (I <sub>C</sub> = 10 μA, I <sub>E</sub> = 0)	V <sub>(BR)CBO</sub>	50	–	–	Vdc
Collector–Emitter Breakdown Voltage (Note 5) (I <sub>C</sub> = 2.0 mA, I <sub>B</sub> = 0)	V <sub>(BR)CEO</sub>	50	–	–	Vdc

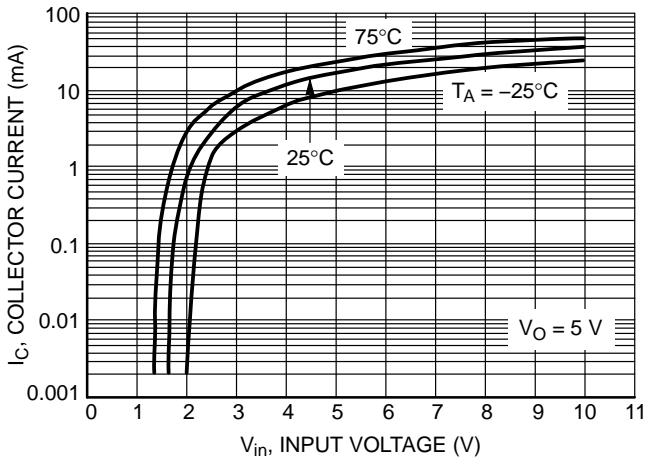
DC Current Gain (Note 5) (I <sub>C</sub> = 5.0 mA, V <sub>CE</sub> = 10 V)	h <sub>FE</sub>	80	140	–	
Collector – Emitter Saturation Voltage (Note 5) (I <sub>C</sub> = 10 mA, I <sub>B</sub> = 0.3 mA)	V <sub>CE(sat)</sub>	–	–	0.25	Vdc
Input Voltage (off) (V <sub>CE</sub> = 5.0 V, I <sub>C</sub> = 100 μA)	V <sub>i(off)</sub>	–	1.8	1.2	Vdc
Input Voltage (on) (V <sub>CE</sub> = 0.3 V, I <sub>C</sub> = 2.0 mA)	V <sub>i(on)</sub>	4.0	2.4	–	Vdc
Output Voltage (on) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 4.0 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OL</sub>	–	–	0.2	Vdc
Output Voltage (off) (V <sub>CC</sub> = 5.0 V, V <sub>B</sub> = 0.5 V, R <sub>L</sub> = 1.0 kΩ)	V <sub>OH</sub>	4.9	–	–	Vdc
Input Resistor	R <sub>1</sub>	32.9	47	61.1	kΩ
Resistor Ratio	R <sub>1</sub> /R <sub>2</sub>	1.7	2.1	2.6	

5. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

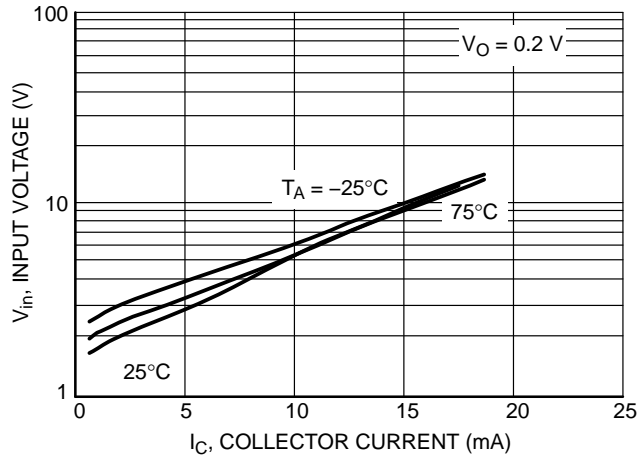
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



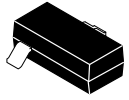
$C_{ob}$ , CAPACITANCE (pF)



$V_R$ , REVERSE BIAS VOLTAGE (V)







SCALE 4:1

SOT 23 (TO 236) 2.90x1.30x1.00 1.90P  
CASE 318  
ISSUE AU

DATE 14 AUG 2024

**SOT 23 (TO 236) 2.90x1.30x1.00 1.90P**  
**CASE 318**  
**ISSUE AU**

DATE 14 AUG 2024

STYLE 6:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 7:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 8:  
PIN 1. ANODE  
2. NO CONNECTION  
3. CATHODE

STYLE 9:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 10:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE

STYLE 11:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 12:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 13:  
PIN 1. SOURCE  
2. DRAIN  
3. GATE

STYLE 14:  
PIN 1. CATHODE  
2. GATE  
3. ANODE

STYLE 15:  
PIN 1. GATE  
2. CATHODE  
3. ANODE

STYLE 16:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE

STYLE 17:  
PIN 1. NO CONNECTION  
2. ANODE  
3. CATHODE

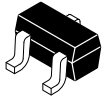
STYLE 18:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. ANODE

STYLE 19:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE-ANODE

STYLE 22:  
PIN 1. RETURN  
2. OUTPUT  
3. INPUT

STYLE 23:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE  
3.



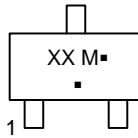


SCALE 4:1

**SC-70 (SOT-323)**  
CASE 419  
ISSUE R

DATE 11 OCT 2022

**GENERIC  
MARKING DIAGRAM**



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-

STYLE 1:  
CANCELLED

STYLE 2:  
PIN 1. ANODE  
2. N.C.  
3. CATHODE

STYLE 3:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 6:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 8:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

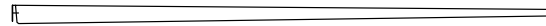
STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. ANODE-CATHODE

STYLE 11:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE



-

RECOMMEND



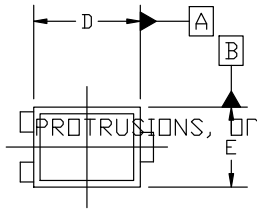


**SOT-1123 0.80x0.60x0.37, 0.35P**  
**CASE 524AA**  
**ISSUE D**

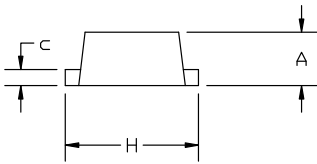
DATE 18 JAN 2024

NOTES:

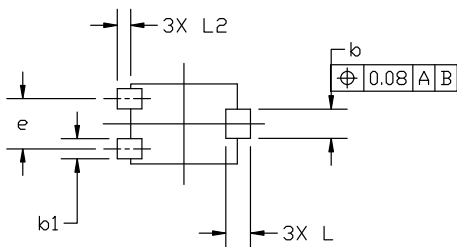
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS, ASH,



TOP VIEW



SIDE VIEW

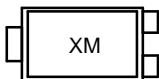


BOTTOM VIEW

← GATE BURRS.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.15	0.22	0.2
			0.5
e	0.35	0.38	0.40
H	0.950	1.000	1.050
L	0.185 REF		
L2	0.05	0.10	0.15

**GENERIC MARKING DIAGRAM\***



- X = Specific Device Code
- M = Date Code

RECOMMENDED MOUNTING FOOTPRINT

\*

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:  
 PIN 1. BASE  
 2. EMITTER  
 3. COLLECTOR

STYLE 2:  
 PIN 1. ANODE  
 2. N/C  
 3. CATHODE

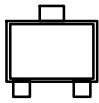
STYLE 3:  
 PIN 1. ANODE  
 2. ANODE  
 3. CATHODE

STYLE 4:  
 PIN 1. CATHODE  
 2. CATHODE  
 3. ANODE

STYLE 5:  
 PIN 1. GATE  
 2. SOURCE  
 3. DRAIN

SOT-723 1.20x0.80x0.50, 0.40P

GENERIC  
MARKING



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