

λ 2 = 100 Ω, = 100

NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb Free, Halogen Free/BFR Free and are RoHS Compliant

Rating	Symbol	Max	Unit
Collector-Base Voltage	V _{CBO}	50	Vdc
Collector-Emitter Voltage	V _{CEO}	50	Vdc
Collector Current – Continuous	Ι _C	100	mAdc
Input Forward Voltage	V _{IN(fwd)}	40	Vdc
Input Reverse Voltage	V _{IN(rev)}	10	Vdc

MAXIMUM RATINGS (T_A = 25° C)

Stresses

MUN2236, MMUN2236L, MUN5236, DTC115EE, DTC115EM3

Table 3. ELECTRICAL CHARACTERISTICS (T_A = 25°

MUN2236, MMUN2236L, MUN5236, DTC115EE, DTC115EM3



TYPICAL CHARACTERISTICS MUN2236, MMUN2236L, MUN5236, NSVMUN5236, DTC115EE, DTC115EM3

Figure 4. Output Capacitance

Figure 5. Output Current versus Input Voltage



Figure 6. Input Voltage versus Output Current



SOT 23 (TO 236) 2.90x1.30x1.00 1.90P CASE 318 ISSUE AU

DATE 14 AUG 2024

SOT 23 (TO 236) 2.90x1.30x1.00 1.90P CASE 318 ISSUE AU

DATE 14 AUG 2024

	STYLE 6: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 7: PIN 1. EMITTER 2. BASE 3. COLLECTOR	STYLE 8: PIN 1. ANODE 2. NO CONNECTION 3. CATHODE		
STYLE 9:	STYLE 10:	STYLE 11:	STYLE 12:	STYLE 13:	STYLE 14:
PIN 1. ANODE	PIN 1. DRAIN	PIN 1. ANODE	PIN 1. CATHODE	PIN 1. SOURCE	PIN 1. CATHODE
2. ANODE	2. SOURCE	2. CATHODE	2. CATHODE	2. DRAIN	2. GATE
3. CATHODE	3. GATE	3. CATHODE-ANODE	3. ANODE	3. GATE	3. ANODE
STYLE 15:	STYLE 16:	STYLE 17:	STYLE 18:	STYLE 19:	
PIN 1. GATE	PIN 1. ANODE	PIN 1. NO CONNECTION	PIN 1. NO CONNECTION	PIN 1. CATHODE	
2. CATHODE	2. CATHODE	2. ANODE	2. CATHODE	2. ANODE	
3. ANODE	3. CATHODE	3. CATHODE	3. ANODE	3. CATHODE-ANODE	
	STYLE 22: PIN 1. RETURN 2. OUTPUT 3. INPUT	STYLE 23: PIN 1. ANODE 2. ANODE 3. CATHODE 3.			



SC-70 (SOT-323) CASE 419 ISSUE R

DATE 11 OCT 2022

GENERIC MARKING DIAGRAM



ΧХ = Specific Device Code

М = Date Code •

= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-

STYLE 1: CANCELLED	STYLE 2: PIN 1. ANODE 2. N.C. 3. CATHODE	STYLE 3: PIN 1. BASE 2. EMITTER 3. COLLECTOR	STYLE 4: PIN 1. CATHODE 2. CATHODE 3. ANODE	STYLE 5: PIN 1. ANODE 2. ANODE 3. CATHODE	
STYLE 6:	Style 7:	STYLE 8:	STYLE 9:	STYLE 10:	STYLE 11:
PIN 1. EMITTER	Pin 1. Base	PIN 1. GATE	PIN 1. ANODE	PIN 1. CATHODE	PIN 1. CATHODE
2. BASE	2. Emitter	2. SOURCE	2. CATHODE	2. ANODE	2. CATHODE
3. COLLECTOR	3. Collector	3. DRAIN	3. CATHODE-ANODE	3. ANODE-CATHODE	3. CATHODE



SC75–3 1.60x0.80x0.80, 1.00P CASE 463 ISSUE H

DATE 01 FEB 2024

RECOMMEND

SOT-723 1.20x0.80x0.50, 0.40P CASE 631AA ISSUE E

DATE 24 JAN 2024

GENERIC MARKING



= Specific Device Code = Date Code ΧХ

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