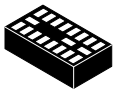
Audio Processor for Digital Hearing Aids

EZAIRO 7111 HYBRID



E7111−0
ZZZZZZ
NNNNN

(Top View)

E7111−0 = Specific Device Code
ZZZZZZ = Assembly Lot Code
NNNNN = Serial Number

Ezairo® 7111 is an open−programmable DSP−based hybrid specifically designed for use in high−performance hearing aid and hearing implant devices. The Ezairo 7111 hybrid includes the Ezairo 7100 System−on−Chip (SoC), with its high−precision quad−core architecture that delivers 375 MIPS, without sacrificing power consumption.

The highly integrated Ezairo 7100 includes an optimized, dual−Harvard CFX Digital Signal Processor (DSP) core and HEAR Configurable Accelerator signal processing engine. It also features an Arm® Cortex®−M3 Processor Subsystem that supports various types of protocols for wireless communication. This block combines an open−programmable controller with hardware accelerators for audio coding and error correction support.

Ezairo 7100 also includes a programmable Filter Engine that enables time domain filtering and supports an ultra−low−delay audio path. When combined with non−volatile memory and wireless transceivers, Ezairo 7100 forms a complete hardware platform.

The Ezairo 7111 hybrid contains the Ezairo 7100 SoC, 2 Mb EEPROM storage and the necessary passive components to directly interface with the transducers required in a hearing aid.

		†
E7111−0-102A19-AG	SIP19 (RoHS Compliant)	250 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

The Ezairo Pre Suite provides a complete framework to easily develop Ezairo−based hearing aids and fitting software. Included in the Ezairo Pre Suite is a firmware bundle, configuration software, and a cross−platform Software Development Kit (SDK) to develop your own fitting software.

To develop your own firmware on Ezairo 7111, the Ezairo 7100 Evaluation and Development Kit (EDK) includes optimized hardware, programming interface, and a comprehensive Integrated Development Environment (IDE).

Note: This datasheet describes all features of the Ezairo 7111 hybrid module. Not all of these features are available using the Ezairo Preconfigured Suite.

Publication Order Number:

- **Programmable Flexibility**: the open−programmable DSP−based system can be customized to the specific signal processing needs of manufacturers. Algorithms and features can be modified or completely new concepts implemented without having to modify the chip.
- **Fully Integrated Hybrid**: includes the Ezairo 100 SoC, 2 Mbit EEPROM storage and the necessary passive components to directly interface with the transducers required in a hearing aid.
- **Quad−core Architecture**: includes a CFX DSP, a HEAR Configurable Accelerator, an Arm Cortex−M3 Processor Subsystem and a programmable Filter Engine. The system also includes an efficient input/output controller (IOC), system memories, input and output stages along with a full complement of peripherals and interfaces.
- **CFX DSP**: a highly cycle−efficient, programmable core that uses a 24−bit fixed−point, dual−MAC, dual−Harvard architecture.
- **HEAR Configurable Accelerator**: a highly optimized signal processing engine designed to perform common signal processing operations and complex standard filterbanks.
- **Arm Cortex−M3 Processor Subsystem**: a complete subsystem that supports efficient data transfer to and from a wireless transceiver. The subsystem includes hardwired CODECS (G.722, CVSD) and Error Correction support (Reed−Solomon, Hamming), as well as a fully programmable Arm Cortex−M3 processor and dedicated interfaces. It is compatible with various wireless technologies (NFMI, RF).
- **Programmable Filter Engine**: a filtering system that allows applying a various range of pre− or post−processing filtering, such as IIR, FIR and biquad filters.
- **Configurable System Clock Speeds**: 1.28 MHz, 1.92 MHz, 2.56 MHz, 3.84 MHz, 5.12 MHz, 6.4 MHz, 7.68 MHz, 8.96 MHz, 9.60 MHz, 10.24 MHz* (default clock calibration), 12.80 MHz and 15.36 MHz to optimize the computing performance versus power consumption ratio. The calibration for these 12 clock speeds are stored in the manufacturing area of the EEPROM.
- **Ultra−low Delay**: programmable Filter Engine supports an ultra−low−delay audio path of 0.044 ms (44 μs) for superior performance of features such as occlusion management.
- **Ultra−high Fidelity**: 85 dB system dynamic range with up to 110 dB input signal dynamic range, exceptionally−low system noise and low group delay.
- **Ultra−low Power Consumption**: <0.7 mA @ 10.24 MHz system clock (executing a tight MAC−loop in the CFX DSP core plus a typical hearing aid filterbank on the HEAR Configurable Accelerator).
- **High Output Level**: output levels of ~139 dB SPL possible with low impedance receiver (measured using IEC 711 coupler).
- **Diverse Memory Architecture**: a total of 40 kwords of program memory and 44 kwords of data memory, shared between the four cores included on the Ezairo 7100 chip.
- **Data Security**: sensitive program data can be encrypted for storage in EEPROM to prevent unauthorized parties from gaining access to proprietary algorithm intellectual property.
- **Signal Detection** Unit: ultra−low−power detection system for signals on any analog inputs.
- **High Throughput Communication Interface**: fast I^2C−based interface for quick download, debugging and general communication.
- **Highly Configurable Interfaces**: two PCM interfaces, two I^2C interfaces, two SPI interfaces, a UART interface as well as multiple GPIOs can be used to stream configuration, control or signal data into and out of the Ezairo 7111 hybrid.
- **On−chip PLL**: support for communication synchronization with wireless transceiver.
- **Glueless MMI**: link to various analog and digital user interfaces such as analog or digital volume control potentiometers, push buttons for program selection and microphone/telecoil switching.
- **Fitting Support**: support for Microcard, HI−PRO 2, HI−PRO USB, QuickCom, and NOAHlink, including NOAHlink’s audio streaming feature.
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

VBAT	Power supply voltage		2	V
VBATOD	Output drivers power supply voltage		2	V
Vin	Voltage at any input pin	GNDC−0.3	VDDO + 0.3	V
GNDC, GNDA	Digital and Analog Grounds	0	–	V
T functional	Functional temperature range (Note 1)	−40	85	°C
T operational	Operational temperature range (Note 1)	0	50	°C
T storage	Storage temperature range	−40	85	°C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V)				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Electrical Specification may exceed listed tolerances when out of the temperature range 0°C to 50°C.

The tests were performed at 20°C with a 1.25 V supply voltage and 4.7 Ω series resistor to simulate a nominal hearing aid battery. The system clock (SYS_CLK) was set to 5.12 MHz and an audio input sampling frequency of 16 kHz was used.

Parameters marked as screened are tested on each chip.

Supply Voltage	VBAT	Supply voltage measured at the VBAT pin	1.05	1.25	2.0	V	
Current consumption	I_{VBAT}	Filterbank: 30% load CFX: 100% load SYS_CLK: 10.24 MHz	–	700	–	μA	
		Ezairo Pre Suite firmware bundle running at 10.24 MHz, all algorithms active, no transducers connected.	–	1090	–	μA	
Stand by current	Istb	Using ON's macro		40	120	μA	

Regulated voltage output	VREG	Trimmed bandgap I_{load} = 100 μA	0.96	0.97	0.98	V	√
Regulator PSRR	$VREG_{PSRR}$	1 kHz, VBAT = 1.25 V	76	80	–	dB	
Load current	I_{LOAD}		–	–	2	mA	
Load regulation	$LOAD_{REG}$	5 μA < I_{load} < 2 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	I_{load} = 1 mA	–	2	5	mV/V	

Output voltage trimming range	VDDA	Control register configured, typical values	1.8	2.0	2.1	V	√
Regulator PSRR	$VDDA_{PSRR}$	1 kHz, VBAT = 1.25 V	40	50	–	dB	
Load current	I_{LOAD}		–	–	1	mA	
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; 100 μA < I_{load} < 1 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	1.2 V < VBAT < 1.86 V; I_{load} = 100 μA	–	6	20	mV/V	

Output voltage trimming range	VDBL	Control register configured, typical values, unloaded	1.6	2.0	2.2	V	√
Regulator PSRR	$VDBL_{PSRR}$	1 kHz, VBAT = 1.25 V	30	40	–	dB	
Load current	I_{LOAD}	ITRIM (A_CP_VDBL_CTRL) = 0x7	–	–	15	mA	
Load regulation	$LOAD_{REG}$	VBAT = 1.2 V; 100 μA < I_{load} < 3 mA	–	4	10	mV/mA	
Line regulation	$LINE_{REG}$	VBAT > 1.2 V; I_{load} = 100 μA	–	6			

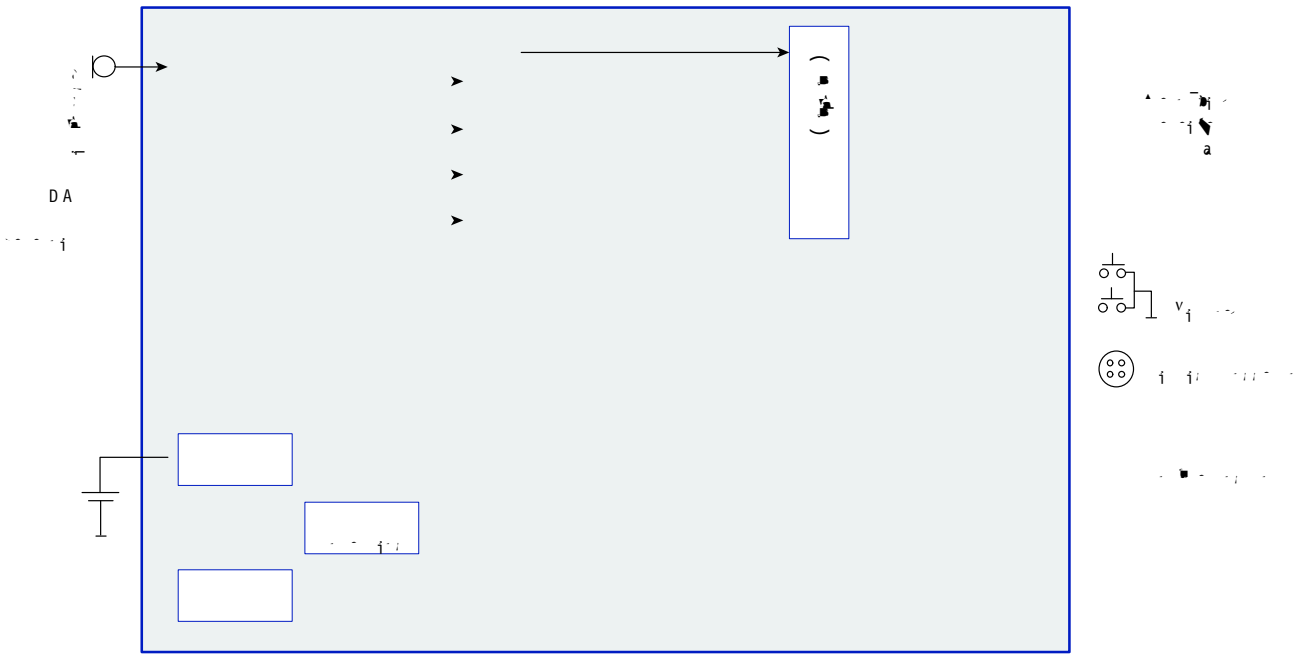
Preamplifier gain	SDU_{PAG}	3dB steps	0	–	36	dB	√
Equivalent IRN	SDU_{IRN}	Non–weighted, 30 dB gain, 100 Hz – 10 kHz	–	–	20	µVrms	√
Input impedance	SDU_{R}		370	500	725	kΩ	√
Low Pass Filter Bandwidth	SDU_{LPF}			50			

1.28 to 5.12	0.73
5.13 to 10.24	0.82 (Note 6)
10.25 to 12.80	0.85
12.81 to 15.36	0.88 (Note 7)

6. The default VDDC calibration entry, stored in the manufacturing area of the EEPROM at address 0x0064, should be used for operation at 0.82 V.
7. An alternate VDDC calibration entry, stored in the manufacturing area of the EEPROM at address 0x00E8, should be used for operation at 0.88 V.

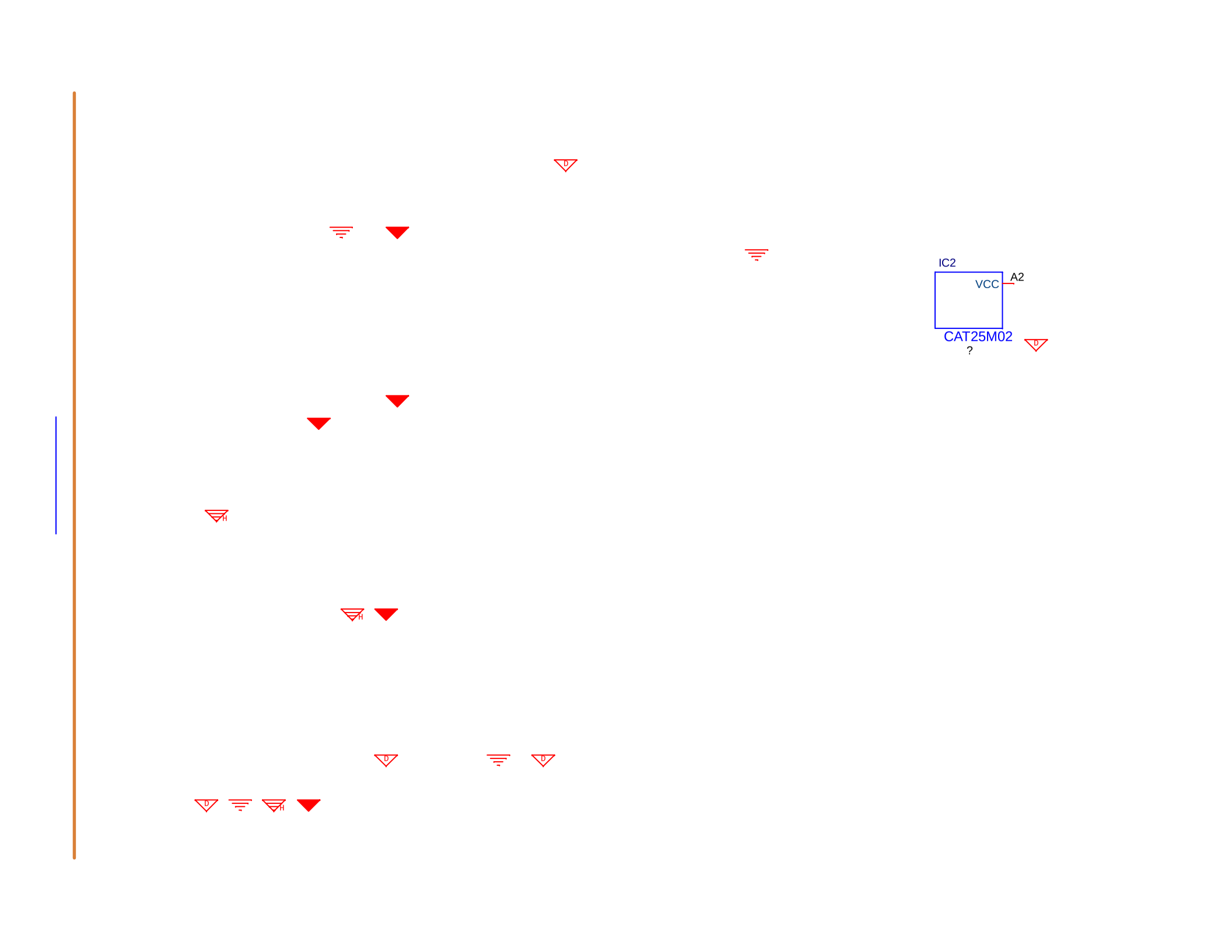
- Ultra−miniature form factor: suitable for all hearing aid styles including CIC, ITE, RITE, BTE, and mini−BTE.
- Can easily be soldered by hand.
- Re−flowable: the Ezairo 7111 hybrid is re−flowable onto FR4 and other substrates.
- Bump metallization: SAC305 (Sn96.5/Ag3.0/Cu0.5)
- RoHS compliant: the Ezairo 7111 hybrid complies with the RoHS directive.

Figure 1 is a simplified diagram of the hybrid system that shows the major internal functional blocks and possible external peripherals.



A total of 19 pads are present on the Ezairo 7111 hybrid. These pads are the interfaces between the hybrid and the other components in the hearing aid. They are listed in Table 4 along with the internal connections.

A1	AI0	Analog Input 0: Microphone or Telecoil Input
A2	MIC_VREG	Regulated voltage for microphone
A3	GND_MIC	Input Transducer Ground
A4	DIO24	Digital Input Output 24
A5	DIO23	Digital Input Output 23
A6	DIO22	Digital Input Output 22
A8	VBAT	Power Supply
B1	AI1	Analog Input 1: Microphone or Telecoil Input
B3	AI3	Analog Input 3: Direct Analog Input
B8	RCVR_BAT	Output Stage Power Supply
C1	AI2	


IC2
VCC
A2
CAT25M02
?

The Ezairo 7100 system is an asymmetric quad−core architecture, mixed−signal system−on−chip designed specifically for audio processing. It centers around four processing cores: the CFX Digital Signal Processor (DSP), the HEAR Configurable Accelerator, the Arm Cortex−M3 Processor Subsystem, and the Filter Engine.

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The CFX DSP core is used to configure the system and the other cores, and it coordinates the flow of signal data progressing through the system. The CFX DSP can also be used for custom signal processing applications that can’t be handled by the HEAR or the Filter Engine.

The CFX DSP is a user−programmable general−purpose DSP core that uses a 24−bit fixed−

- Arm Cortex−M3 processor PCM interface

System identification is used to identify different system components. This information can be retrieved using the Promira Serial Platform from TotalPhase, Inc. Or the Communications Accelerator Adaptor (CAA) and some protocol software provided by ON Semiconductor (see CAA instruction manual). For the Ezairo 7100 chip, the key identifier components and values are as follows:

- Chip Family: 0x06
- Chip Version:0x01
- Chip Revision: 0x0200

The hybrid ID can be found in the manufacturing area of the EEPROM at address 0x00F1 to 0x00F2 (2 bytes => 16 bits)

- Hybrid ID: 0x00B0

CAUTION: ESD sensitive device. Permanent damage may occur on devices subjected to high−energy electrostatic discharges. Proper ESD precautions in handling, packaging and testing are recommended to avoid performance degradation or loss of functionality.

For more information on which development tools best suit your product development, contact your local sales representative or authorized distributor.

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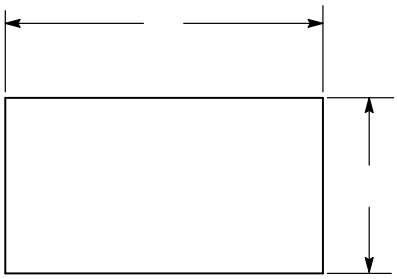

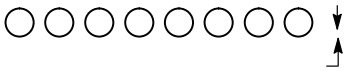

SEATING PLANE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BUMPS.

	MILLIMETERS	
DIM	MIN	MAX
A	---	
A1		