LV25810PEB

http://onsemi.com

Overview

LV25810PEB is a DSP tuner LSI which adopts Low-IF. This IC has realized not only the significant reduction of external parts compare to the existing model by integration, but also the reconfiguration of specification according to customers' need by setting and controlling the software of microcontroller, in which constant is programmable. Therefore, this IC curbs the total cost and realizes a tuner which corresponds to on-board type.

This LSI implements serial bus (I^2C) I/F, which realizes reduction of communication line with microcontroller. In mass production, it is effective to prevent troubles related to line layout, and to reduce area of the system main board.

Recommended operating supply voltage at Ta=25∀C

Parameter	Symbol	Pin name	Min.	Typ.	Max.	unit
Supply voltage	Vcc1	VCC_OSC, VCC_IF, VCC_AM ,VCC_FM	–	5.0	–	V
Supply voltage	Vcc2	VDD33, PLLVDD, XVDD, AVDD33, DACVDD	–	3.3	–	V
Supply voltage	Vcc3	VDD15	–	1.5	–	V

Electrical characteristics at Ta=25°C, FM fr=98.1MHz

AM fr=1MHz, After tuning AM RF Synchronization

Parameter	Symbol	Pin name	Conditions	Min.	Typ.	Max.	unit
Current consumption (5V AM)	I5V_AM		No input signal, AM Mode	72.25	85	97.75	mA
Current consumption (3.3V AM)	I33V_AM		No input signal, AM Mode	68	80	92	mA
Current consumption (1.5V AM)	I15V_AM		No input signal, AM Mode	93.5	110	126.5	mA
Local frequency 3rd and 5th spurious rejection ratio	AM_HRR3 AM_HRR5		Freq. Setting = 1000kHz, AM_HRR3: 3230kHz, with RF input, AM_HRR5: 5230kHz, with RF input				

Package Dimensions

unit : mm

Pin overview

I : Input pin, O : Output Pin, B : Bi-Directional Pin, A : Analogue Pin, P : Power Supply
Output Level1: Initial condition (After finishing reset procedure), Output Level2 : During reset procedure

Pin No.	Pin name	I/O	Output Level1	Output Level2

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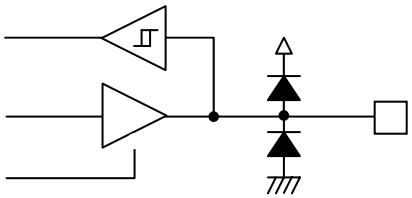
Pin	Function	Equivalent circuit	Remarks
27	I2C_SDA		Digital Input/Output (5V tolerant)
34	VDD33	-	Digital Power Supply (3.3V)
35	REFV		Reference Voltage output
36	DVSS	-	Digital GND
37	VDD15	-	Digital Power Supply (1.5V)
38	PLLVDD	-	PLL Power Supply (3.3V)
39	PLLVSS	-	PLL GND
40	DACVSS	-	GND for Audio DAC
41 43	DACROUT DACLOUT		DAC Output
42	DACREF		Reference Voltage Output for AudioDAC
44	DACVDD	-	VDD for Audio DAC (3.3V)

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Pin	Function	Equivalent circuit	Remarks
45 46	XIN XOUT		Oscillator circuit
47	XVDD	-	VDD for Crystal OSC (3.3V)
48	XVSS	-	GND for Crystal GND
49	AVSSVREF	-	Reference GND for IF ADC
50 51	AVREFI AVREFQ		ADC

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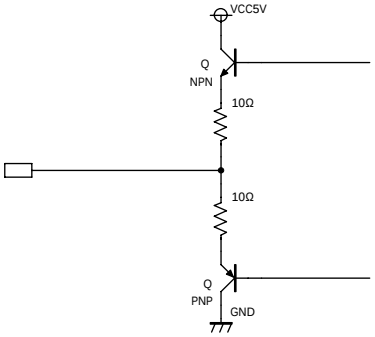
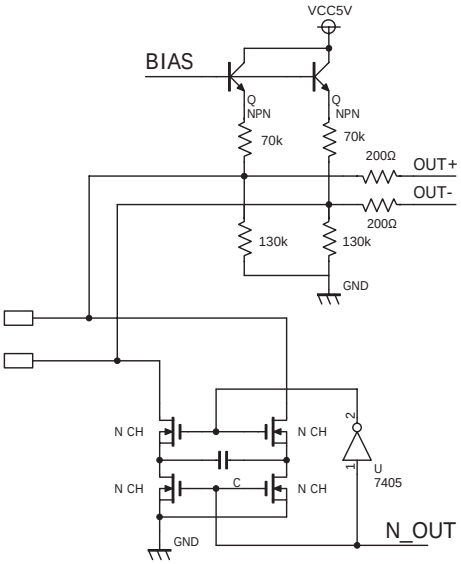
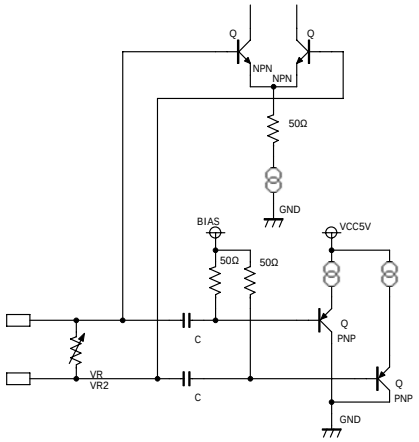
Pin	Function	Equivalent circuit	Remarks
64 65	AM LNA out+ AM LNA out-		¢ AM LNA output
66	GND_AM	-	¢ GND for AM
67 68	AM_CB_IN- AM_CB_IN+		¢ AM capacitor-bank input
69 70	FM_IN+ FM_IN-		¢ FM LNA input Č Input RF signal.
71	VCC_FM	-	¢ 5V supply for FM

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Pin	Function	Equivalent circuit	Remarks
72 73	WB_IN+ WB_IN-		¢ LNA input for weatherband (WB) ¢ Buffered-Output for sub-tuner Č

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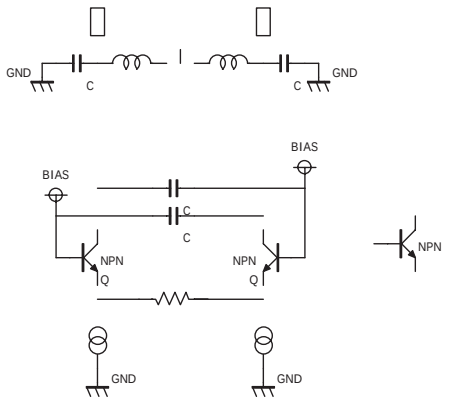
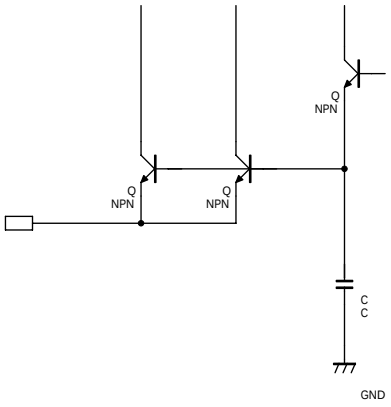
Pin	Function	Equivalent circuit	Remarks
78 80	VCO1 VCO2		¢ VCO oscillation Č Do not connect any other circuit.
79	VCO_BIAS		¢ VCO BIAS pin Č For the stabilization of the VCO bias voltage level with external capacitor .

The Power Supply / Shut Down Procedure

The power supply / shutdown order to each Power pins and the specified pins are as follows.
These order and timings must be kept absolutely.

1) To start the system

RSTB pin must be kept the “L” level during 5ms after latter either the 1.5V System is activated or the waiting time of the OSC being stable.

2) To Shut Down the System

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit

Host I/F

I^2C I/F

The I^2C interface supports 100kbs Standard mode and 400kbps High-Speed mode, and the unit of data transfer is 8 bits. The details of data read and data write are written in software control manual.
I2C slave address is 0x1D.

Data Write

Data write can be accepted during the status of “BUSY” output level is “L”. The command and data during the status of “BUSY” output level is “H” cannot be acceptable.

WatchDog Timer

To detect the runaway of internal DSP, LV25810 has the WatchDog Timer (WDT) output pin.
When the DSP runaway, the WDT overflows and the DSP status can be confirmed by the output of BUSY and SP_ERR pin

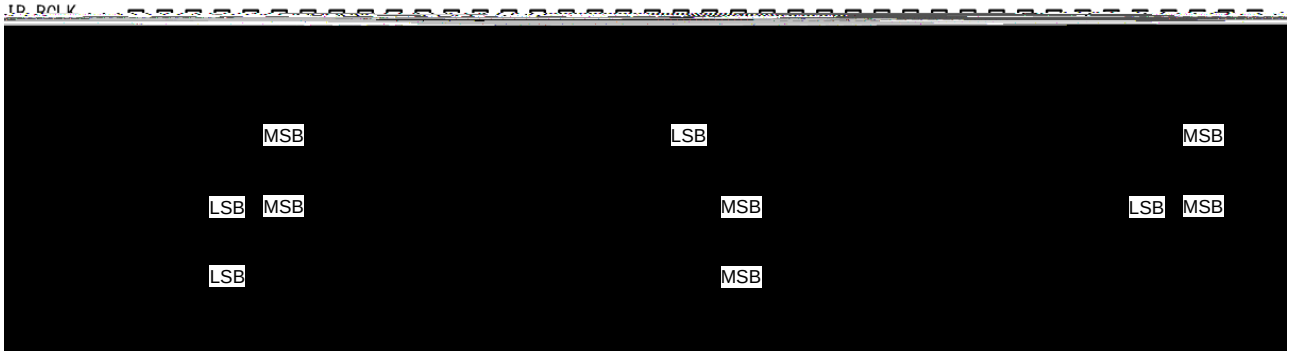
Pin		Status
BUSY	SP_ERR	
0	0	Command Waiting
1	0	Commanad transfer finished
0	1	Communication Error
1	1	DSP Runaway (WDT Overflow)

When both of BUSY and SP_ERR output level are “H”, the operation state of the DSP is abnormal.
If this occurs, the host CPU must reset and reboot the LV25810.

IBOC I/F

IBOC Decoder output is ready.
Fs : 650kHz
BCLK : 10.4MHz
Data Length : 16 bits

IBOC I/F Timing Chart



Timing Specifications

IB_QDATA
IB_IDATA

Parameter	Symbol	Min.	Typ.	Max.	Unit
IB_BCLK frequency	fBCLK		10.4		MHz
IB_WS Output Delay Time	tWD	0		10	ns
IB_QDATA, IB_IDATA Output Delay time	tDD	0		15	ns

Audio Output

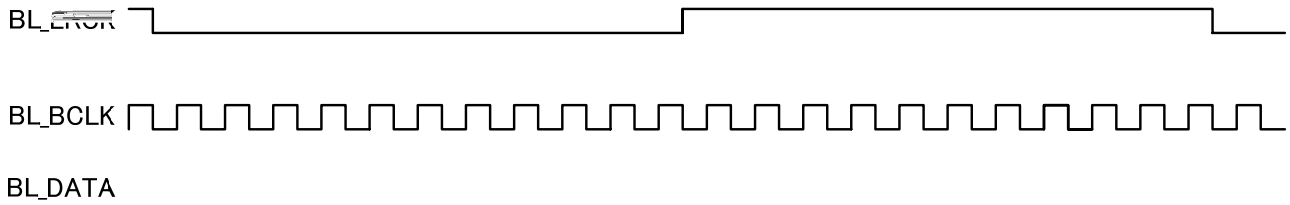
Audio output (I2S format) is available.
fs : 54.167kHz
BCLK : 64fs
Data Length : 24 bits

Audio Output Timing Chart

IBOC BLEND Input

Audio Input (I^2S format) for IBOC BLEND is available.
fs : 44.1kHz
BCLK : 32fs to 64fs
Data Length : 16 bits

Timing Chart I

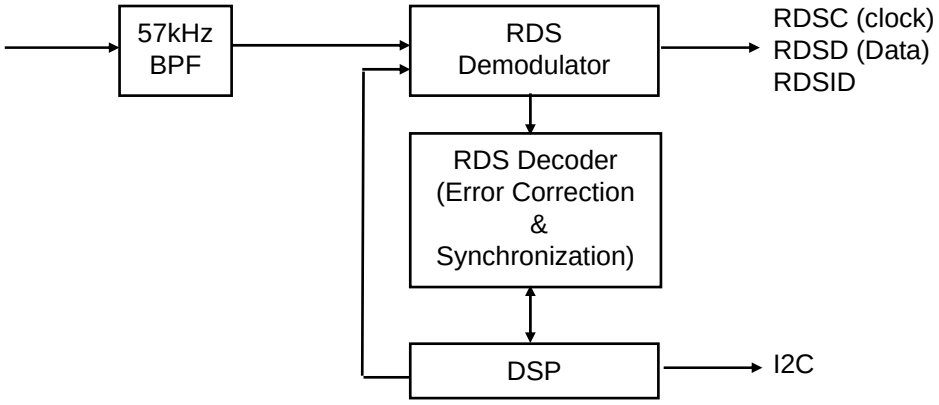


RDS Demodulation Function

The RDS (Radio Data System) for EBU (Europe Broadcasting Union) and the RBDS (Radio Broadcast Data System) for NSRC (National Radio System Committee (US)) demodulator system is available.
This system includes both the RDS demodulator, which outputs the RDS data directly to the RDSC, RDSD, RDSID pin and the RDS decoder, which contains the error corrector function and data transfer function to the main microcontroller.
The setting method is written in the software control manual.

(1) Block Diagram of RDS demodulation function

RDS demodulation function has following 4 blocks.
57kHZ BPF for RDS carrier signal,
RDS demodulator for by-phase demodulation,
RDS decoder for the error correction and data synchronization,
DSP for whole RDS system control
The block diagram is as follows.



a) 57kHz BPF block

This block contains the band-path filter to get the 57kHz signal, which is the 3rd harmonics of RDS sub-carrier signal (19kHz). The sufficient characteristics of the RDS demodulation is provided with the digital filter.

b) RDS Demodulator block

To demodulate the RDS signal, this block contains the comparator block, by-phase clock regeneration block, and the criterion circuit for data reliability.

The comparator block has the zero cross linear complement function and zero cross detection function.
This block lets the most suitable comparison position for the carrier signal from BPF block with doing the linear complementation.

The bi-phase clock regeneration block has digital PLL, DATA module, and ARI detector. The PLL regenerates the carrier signal and ARI detector detects the ARI signal. The data latch timing is defined depending on the state of the ARI and the RDS data is decoded in DATA module.

The DATA module generates the RDS clock (RDSC) , RDS output data (RDSD), and RDS output data judgement (RDSID) signals.

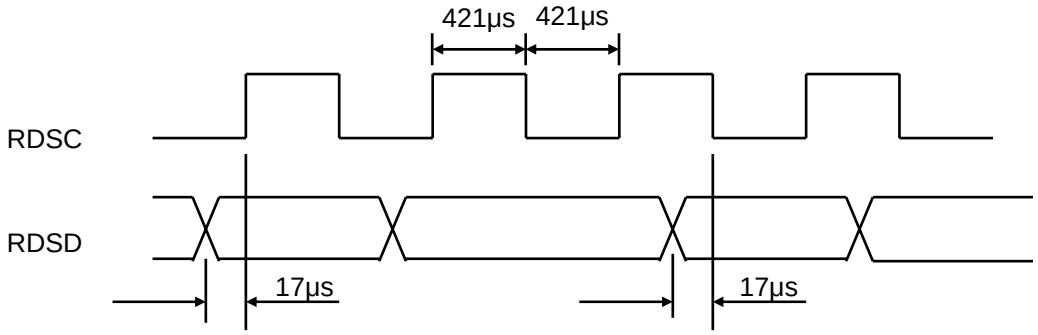
c) RDS Decoder Block (Error correction block)

RDS decoder block has the syndrome-register, the offset word detection function, the synchronism detection function, and the error detection function. The RDS data is processed the syndrome-register, and the offset word is detected with the offset detector by the output signal from the syndrome-register. The synchronization pull-in process is executed in synchronism detection function depending on the content of the off-set word. The selection of whether RDS or RDIS is controlled from DSP.
The intersymbol distance about the RDS data which may be wrong is measured and the soft-detection error correction is executed.

d) DSP

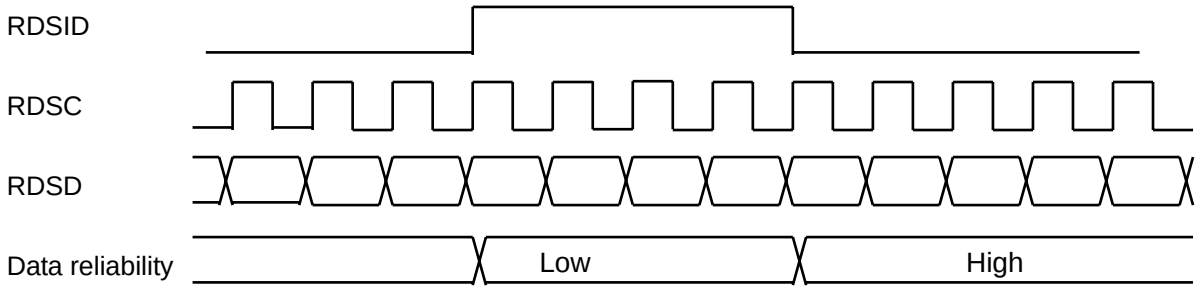
This DSP controls all of the RDS functions by the instructions from the main microcontroller.
The demodulation data and the error collection data is transferred to the main microcontroller via DSP.

(2) RDSC, RDSD output timing



(3) RDSID output timing

RDSID output indicates the reliability of the RDS data.
When the RDS data is reliable, the RDIS output level becomes “L”.

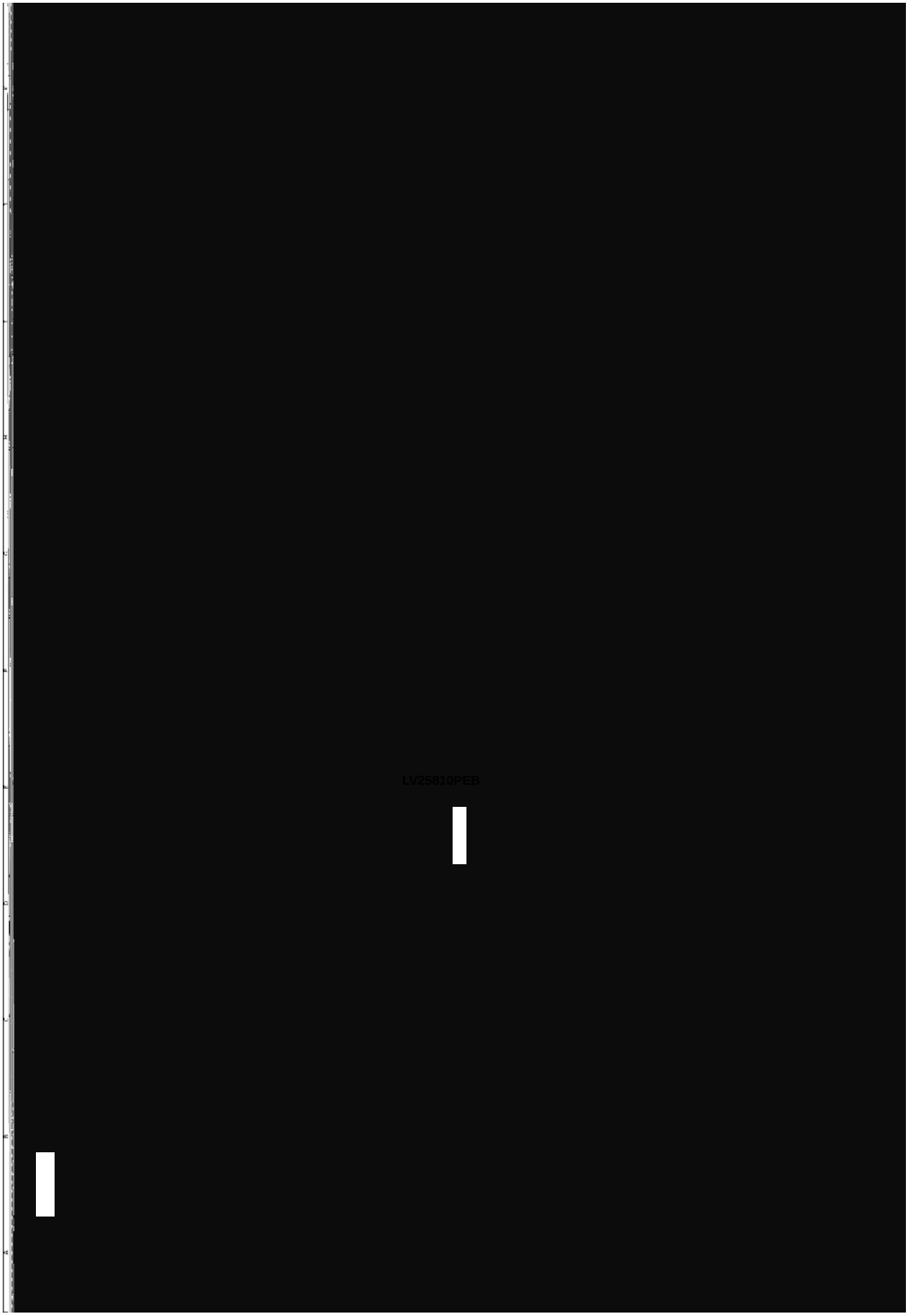


Controllable Items

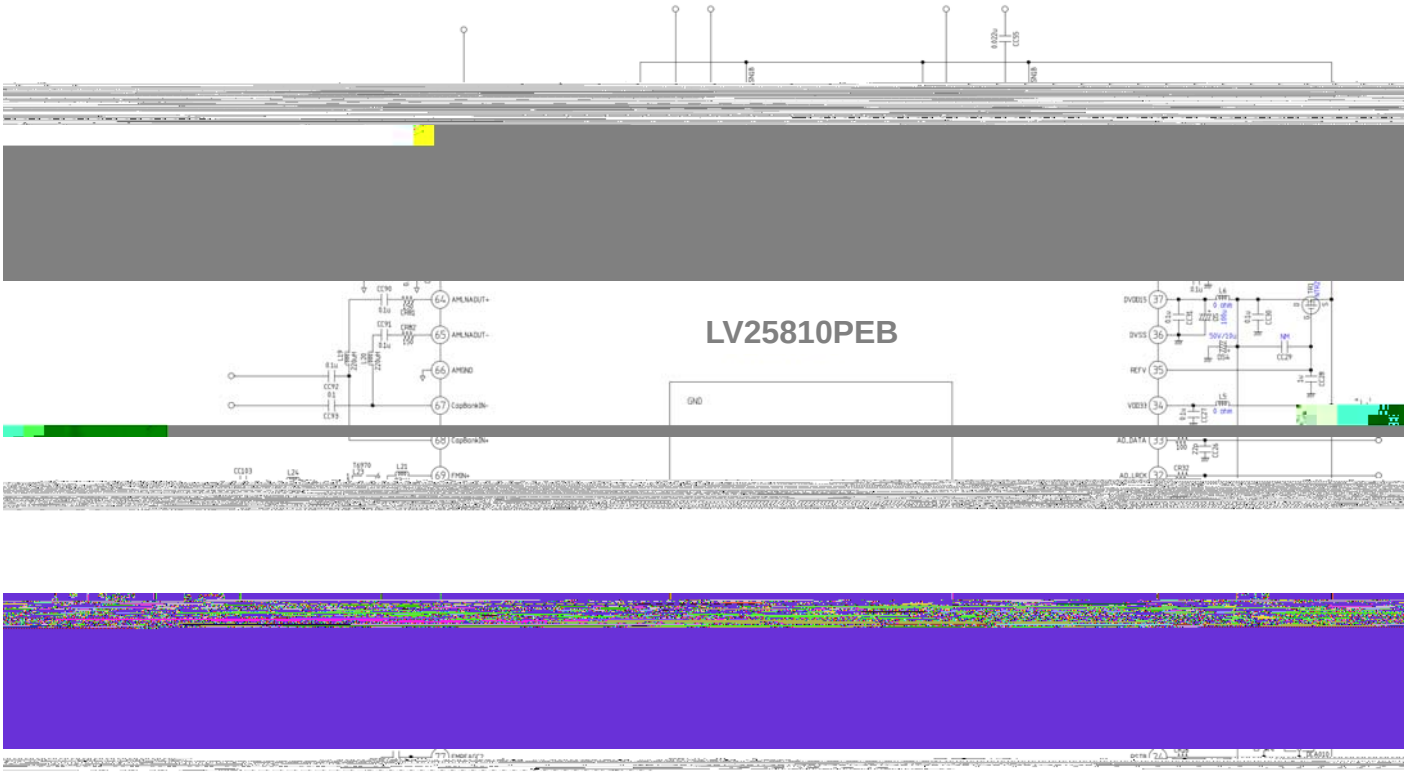
The following items are controllable. Details are shown in the software control manual.

- IF-BPF (Band Pass Filter)
- Local OSC
- AM RF Synchronization (Correct the difference of the AM CAP BANK)
- Image (Correct the amplitude error and phase error of the IQ signal)
- IF Offset (Correct the frequency mismatch of the IF signal)
- S-meter DC
- Separations

Application circuit



Measurement circuit



FM LNA+ RF AGC, WB LNA+ RF AGC (Including the IF-AFC)

When there is a FM (WB) RF signal at the ANT input, the output of MIX amplifier is about 25 dB. It attenuates by 3dB per steps by switching the LNA, a total of 22 steps in Attenuation. RF_AGC_1 operates when antenna input level is bout 75dBuV. RF_AGC_0 is the AGC for the LNA to improve the sensitivity and operates when antenna input level is about 60dBuV. A 65MHz~108MHz band pass filter in formed by the LC Antenna input.
(Details are shown in software control manual.)

Signal processing Image

AM LNA+RF AGC (Including the IF-AGC)

The AM RF signal of the ANT input approximately 23 dB is feed into to the MIX.
LNA gain is controlled by 3dB per step, a total of 21 steps attenuation. RF AGC operates when antenna input is about 80dBuV.
In case of receiving the LW (144kHz – 281kHz), the RF signal output from LNA is input into the mixer via LPF. In case of receiving the MW (520kHz -1710kHz), the RF signal output from LNA is tuned by the capacitor bank and is input into the mixer.
In case of receiving the SW (2MHz – 30MHz), the RF signal output from LNA is input into the mixer via HPF.
The input LC antenna circuit makes 144 kHz – 30 MHz BPF.
(Details are shown in the software control manual.)

Signal Processing image

PLL

The LO_OSC frequency divider (P_CTR) output is compared with the reference frequency (R_CTR) so that they will have a zero phase difference. It makes output voltage of VT.

Local Oscillator

LO oscillator consists of the internal varactor and the

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LV25810PEB-6156H	QFP80(14X14) (Pb-Free / Halogen Free)	60 / Tray Foam