December, 2023 − Rev. 2

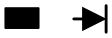

Figure 1. Application Schematic with FAD3171MXA as High Side and FAD3151MXA as Low Side drivers

PIN FUNCTION DESCRIPTION

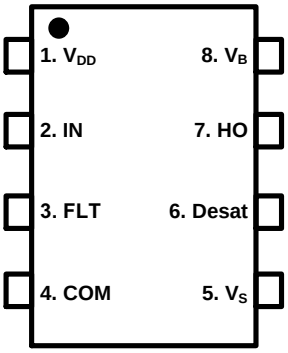

Figure 3. Pin Connection
(Top View)

PIN FUNCTION DESCRIPTION

Pin #	Pin Name	Description
1	V_{DD}	Power supply for logic stage
2	IN	Input command
3	FLT	Bi−directional fault pin
4		

ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_S = 0 V unless otherwise noted, T_A = −40°C to 125°C. Voltage potentials are referenced to COM unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit

TYPICAL CHARACTERISTICS

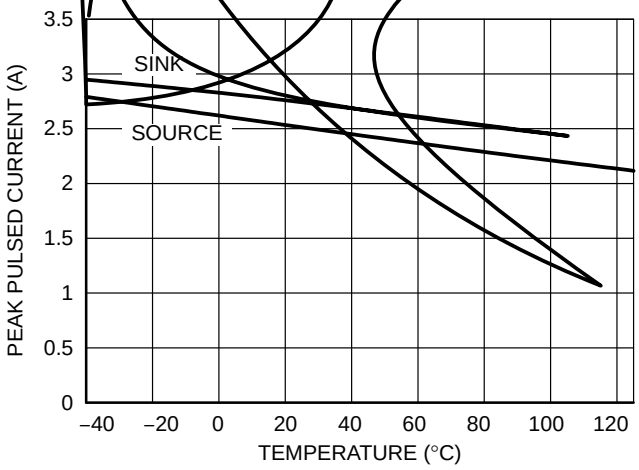

Figure 10. Peak Pulsed Current vs. Temperature

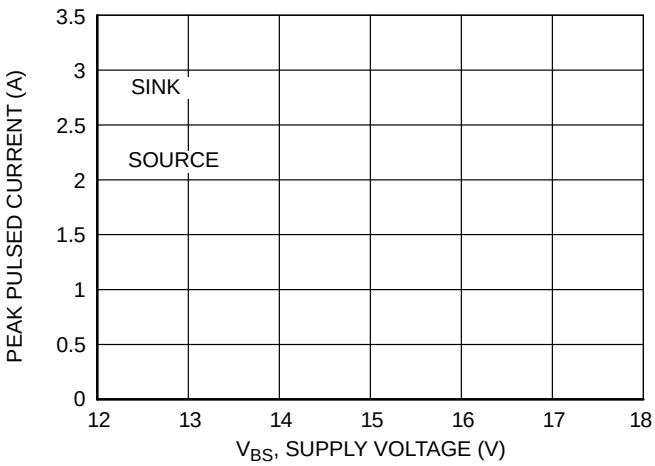

Figure 11. Peak Pulsed Current vs. VBS Voltage

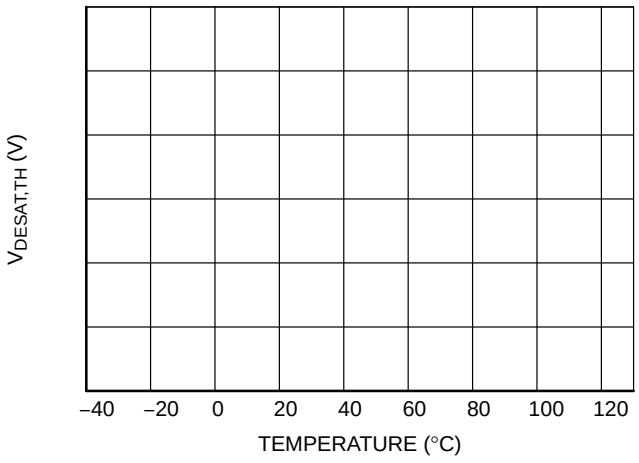

Figure 12. Desat Threshold vs. Temperature

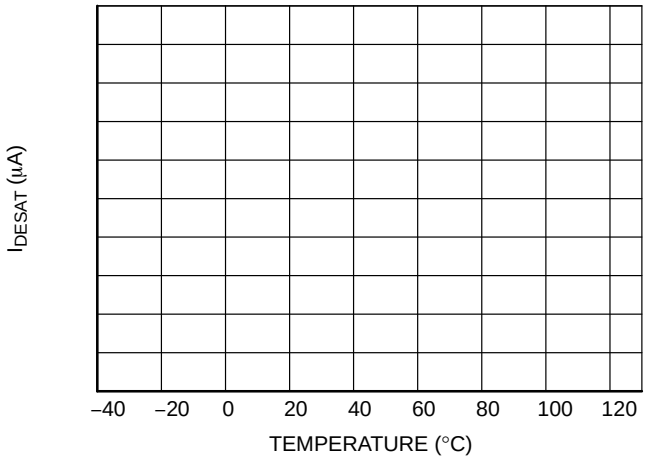

Figure 13. Desat Current vs. Temperature

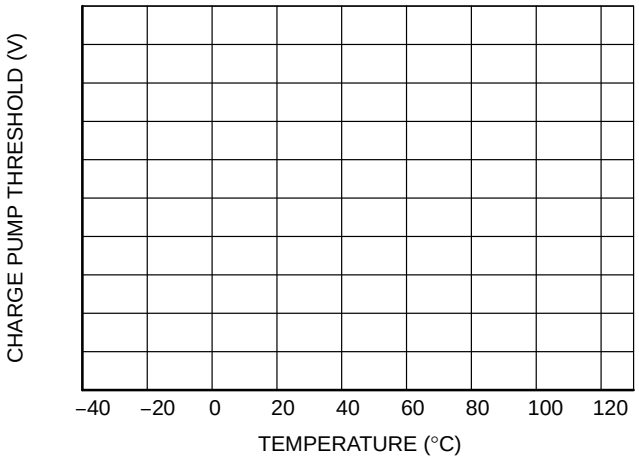

Figure 14. Charge Pump Turn On/Turn Off Threshold vs. Temperature

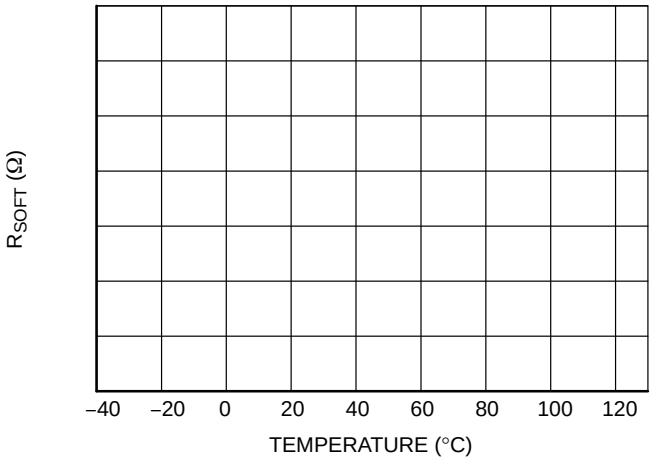

Figure 15. Soft Shutdown Resistance vs. Temperature

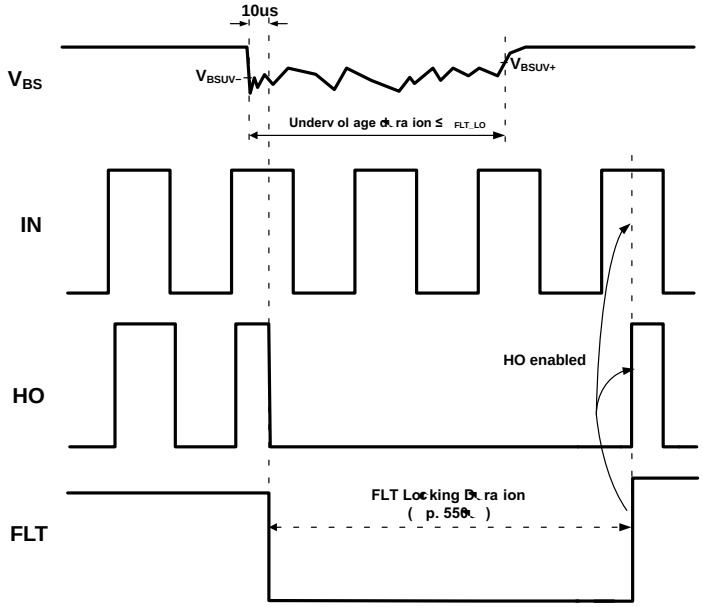

Figure 17. Under−Voltage Condition Shorter than FLT Locking Duration

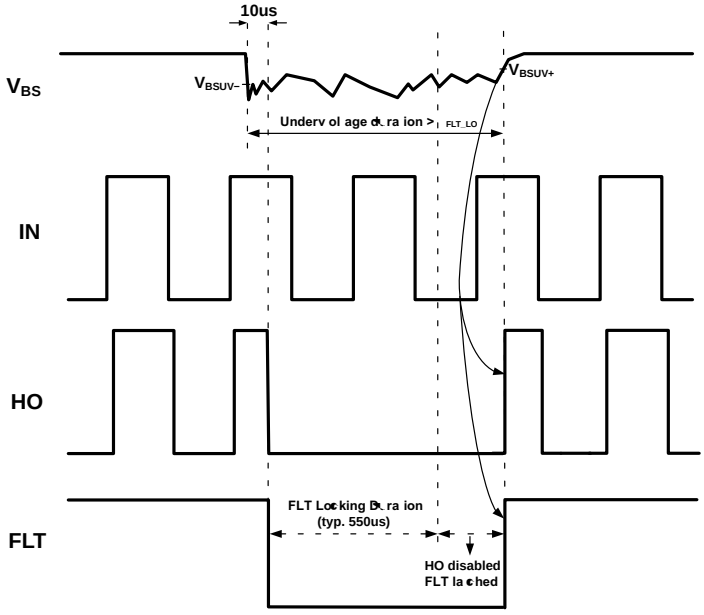

Figure 18. Under−Voltage Condition Longer than FLT Locking Duration

Desaturation Protection with Soft Shutdown

The gate driver has a desaturation detection circuit that monitors the drain to source V_{DS} voltage of the power MOSFET through the desaturation detection pin. As shown in the simplified block diagram in Figure 2, the desaturation circuit comprises of:

- An internal current source that provides a continuous current toward the power stage to monitor the V_{DS} voltage. The desat current source (I_{DESAT}) is supplied from the V_B pin and is continuously active as soon as the V_{DD} is higher than the $UVLO_{VDD+}$, independent of the status of the input logic.
- An internal comparator that compares the voltage at the desat pin (V_{DESAT}) with the defined desat threshold ($V_{DESAT,TH}$) of 3 V (typ.). When V_{DESAT} exceeds $V_{DESAT,TH}$, the comparator simultaneously turns off the output ‘slowly’ and triggers a fault condition by pulling down the fault pin internally.

As shown in application schematic in Figure 1, the desat diode D_1, resistor R_1, blanking capacitor C_{BL}, and P−channel JFET P_1 are the minimum external components required to operate the desaturation protection scheme. The driver needs an external pull down transistor P_1 to discharge I_{DESAT} and C_{BL} as soon as the driver output turns off.

Otherwise, the blanking capacitor will continue to charge up and eventually trigger desat. The presence of a normally on P1 also enhances noise immunity of desat blanking capacitor against false triggering during the turn on event of complementary power switch. The external desat components can be modified to adjust the blanking time and the desat detection threshold for a given application. It is recommended to refer to the Application Note for more details.

If the power switch is turned−off rapidly during a heavy−load condition, the high currents may generate a voltage overshoot across the power switch that could potentially damage it. In order to protect the devices, the driver has a soft shutdown feature, which activates upon desat detection. The output is then driven low through a large turn−off resistance (R_{SOFT}) which provides a significantly higher resistive path for the gate capacitance to discharge than during the regular turn−off process. As a result, the possibility of an abrupt overvoltage spike on the power switches is reduced.

When the voltage at the desaturation pin exceeds the defined desat threshold, following protection sequence is performed:

- The gate driver initiates a soft shutdown. The driver will provide a high resistive path through R_{SOFT} for gate capacitance to discharge slowly [see Figure 19]. The fall rate of HO is determined by the time constant of the RC discharge path.
- The driver also triggers an internal fault and pulls down the fault pin for the period equivalent to Fault Locking duration (typ. 550 μs).

NOTE: If the desat condition persists even after the fault locking duration, and if the input signal is still provided, the driver output will reappear for a period equivalent to the blanking time, after which the desat protection will retrigger the soft shutdown and turn off the output again.

Figure 19. Desaturation Protection and Soft Shutdown

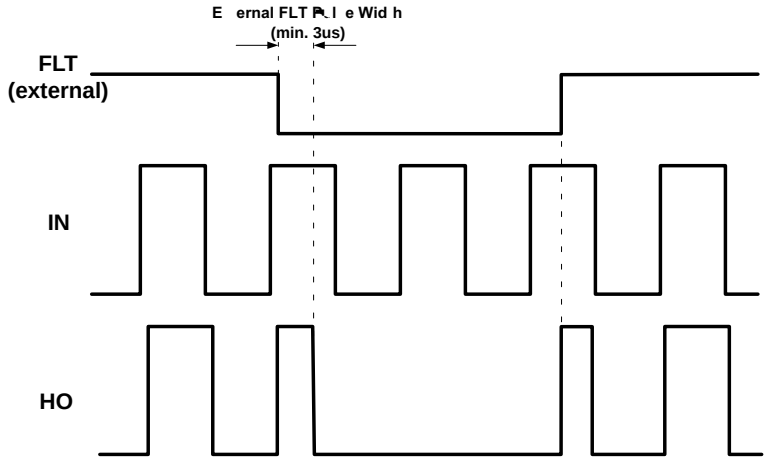

Figure 20. External fault Triggering Condition

Charge Pump for 100% Duty Cycle Operation

The FAD3171MXA driver contains an internal charge pump that enables 100% duty−cycle operation of high−side power switches. When the high−side switch is kept on for a long duration, the bootstrap capacitor could slowly discharge and may eventually trigger the under−voltage lockout protection and turn off the driver output. Therefore, the purpose of the charge pump is to supply the V_{BS} quiescent current necessary for the high−side gate driver to operate under 100% duty cycle and to compensate for additional leakage current on the gate path.

It should be ensured that the total leakage current in the gate path does not exceed the maximum output current capability of the charge pump $I_{CP,OUT}$. For example, in Figure 21, when the gate is continuously high, the pull−down resistance R_2 will continuously sink a current and for this reason, its value should be high enough to minimize the total leakage current drawn from the charge pump. Considering a maximum output current of 150 μA at $V_{BS} = CP_{ON} = 15$ V, the value of R_2 should be higher than 100 kΩ to maintain a steady charge pump output.

The charge pump deactivates as soon as:

- The V_{BS} voltage rises back to a value higher the charge pump turn off threshold (CP_{OFF}).
- The V_{DD} is lower than the V_{DD} under voltage negative−going threshold (V_{DDUV-}).

In order to ensure that the charge pump and the UVLO function do not interfere with each other, the charge pump turn−on threshold (CP_{ON}) is designed to be higher than the V_{BSUV-} threshold. As a result, the driver output is higher than the V_{BSUV-} threshold during charge pump mode. If the load on the charge pump exceeds $I_{CP,OUT}$, the voltage across the V_B−V_S pins will slowly decrease and eventually trigger

PACKAGE DIMENSIONS

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017

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