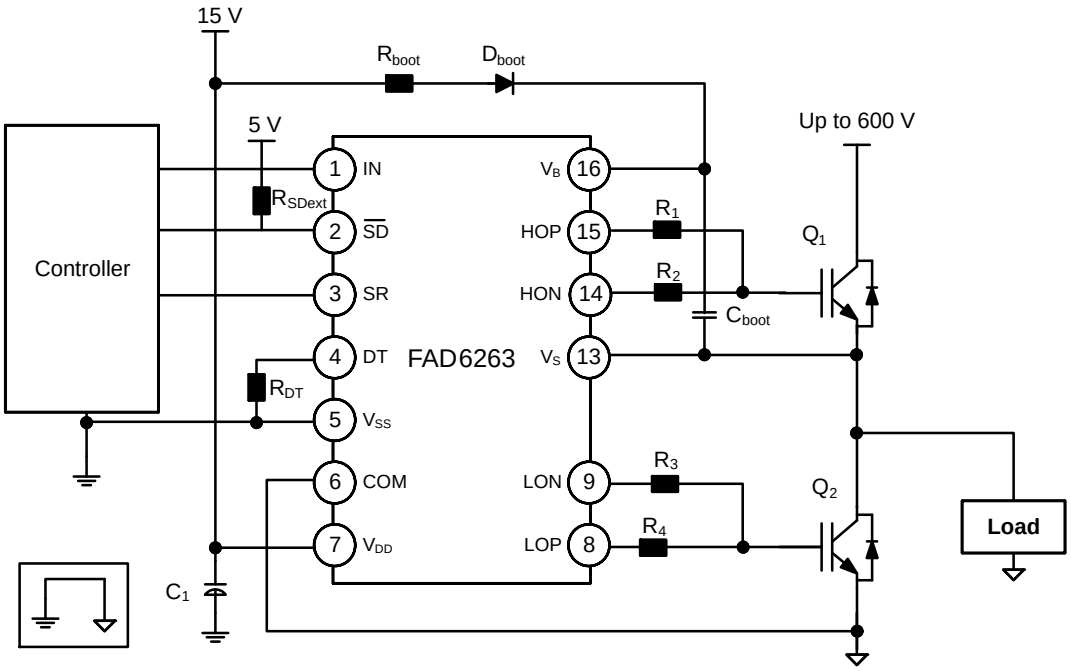
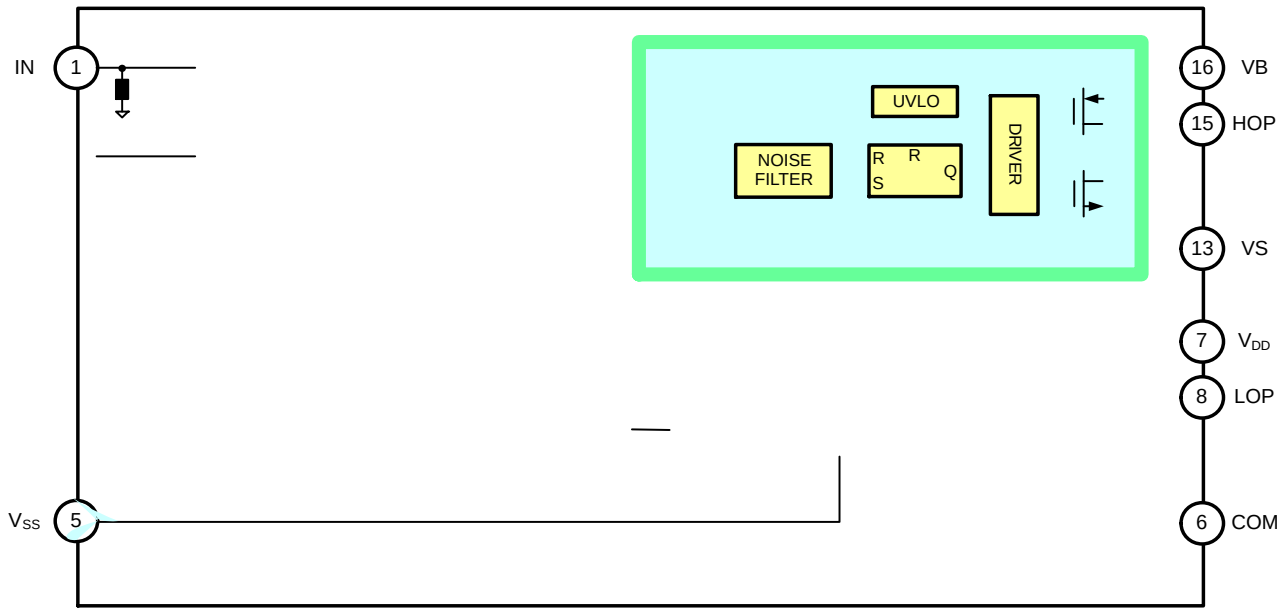


Figure 1. Application Schematic − SOIC16



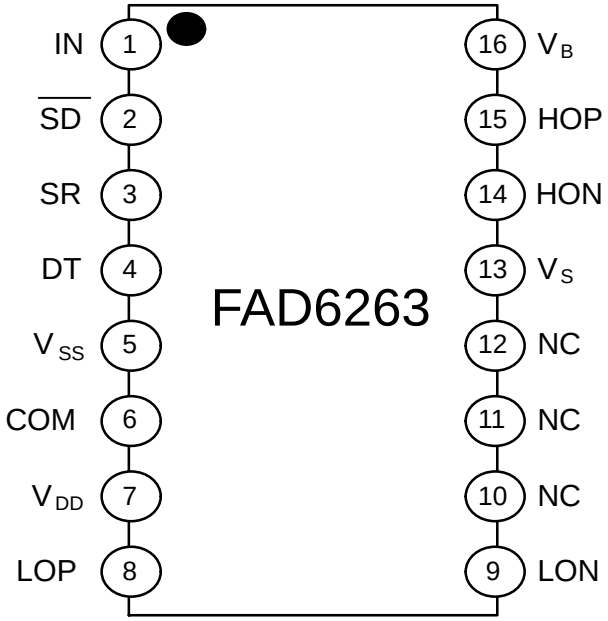


Figure 3. Pin Connection (Top View)

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
1	IN	Logic Input for Complementary Outputs
2	$\overline{SD}$	Logic Input Shutdown (Active Low)
3	SR	Shutdown Reset
4	DT	Dead−Time Control with External Resistor (referenced to VSS)
5	VSS	Logic Ground
6	COM	Power Ground, Low−Side Driver Return
7	VDD	Low−Side and Logic Power Supply Voltage
8	LOP	Low−Side Driver Output (Pull Up)
9	LON	Low−Side Driver Output (Pull Down)
10	NC	No Electrical Connection (Note 1)
11	NC	No Electrical Connection (Note 1)
12	NC	No Electrical Connection (Note 1)
13	VS	High−Side Floating Supply Return
14	HON	High−Side Driver Output (Pull Down)
15	HOP	High−Side Driver Output (Pull Up)
16	VB	High−Side Floating Supply

1. The lead and the silicon die are not electrically connected. Printed circuit board traces are allowable.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
High−Side Floating Supply Voltage	V		

Table 4. ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_{SS} = COM = 0 V, DT = V_{SS} and T_A = −40°C to 125°C unless otherwise noted.)

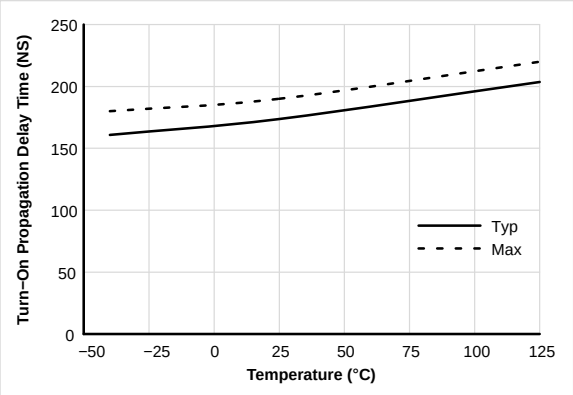
Parameter	Test Condition	Symbol

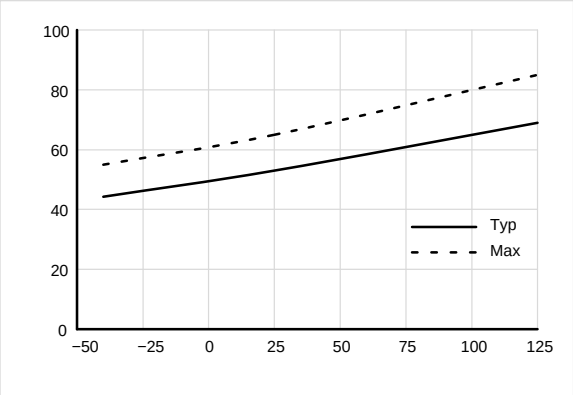
Table 4. ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{DD}, V_{BS}) = 15 V, V_{SS} = COM = 0 V, DT = V_{SS} and T_A = −40°C to 125°C unless otherwise noted.)

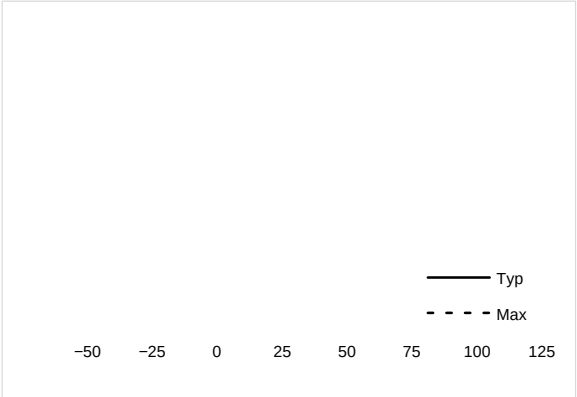
Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
DYNAMIC SECTION						
Turn−On Propagation Delay (Note 10)	V_S = 0 V, R_{DT} = 0 Ω, C_L = 1000 pF	t_{ON}		155	230	ns
Turn−Off Propagation Delay (Note 11)	V_S = 0 V, C_L = 1000 pF	t_{OFF}		55	90	ns
Delay Matching HO and LO Turn−On		Mt_{ON}			25	ns
Delay Matching HO and LO Turn−Off		Mt_{OFF}			20	ns
Turn−On Rise Time	V_S = 0 V, C_L = 1000 pF	t_R		10	23	ns
Turn−Off Fall Time		t_F		10	20	ns
Dead−Time: LO Turn−Off to HO Turn−On,						

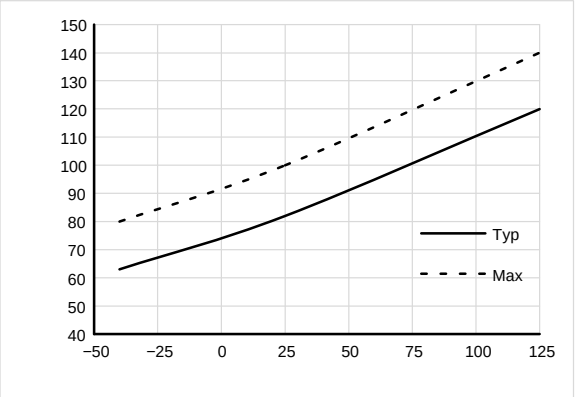
TYPICAL PERFORMANCE CHARACTERISTICS

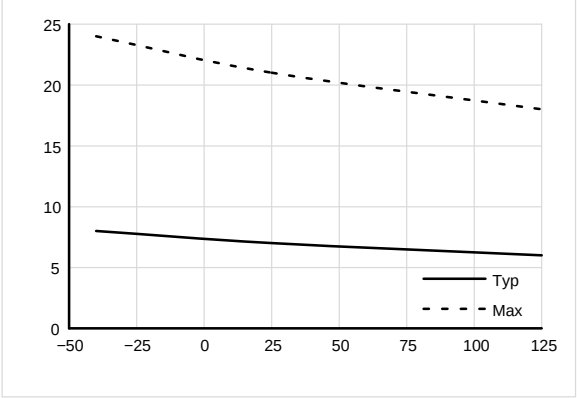


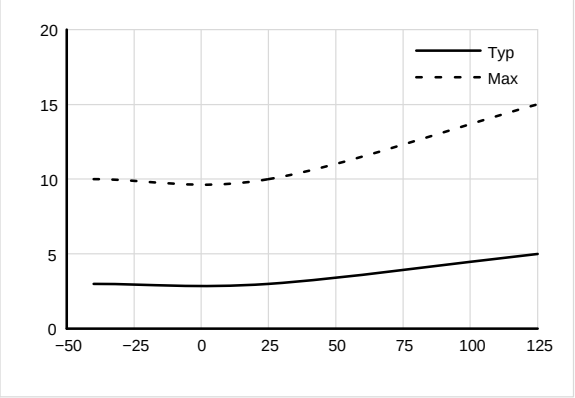


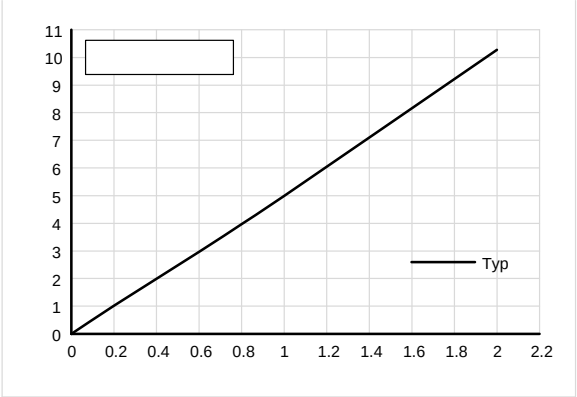
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

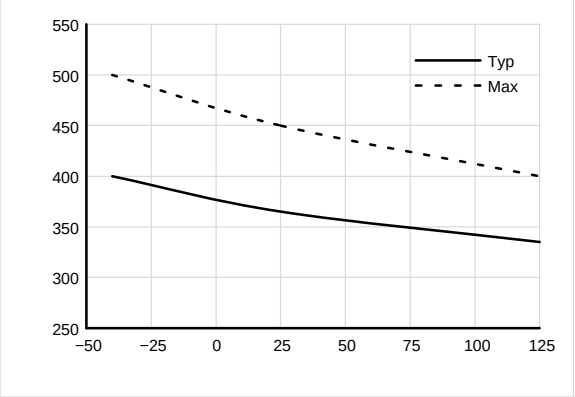






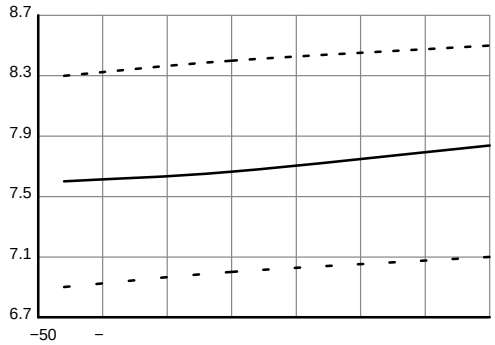




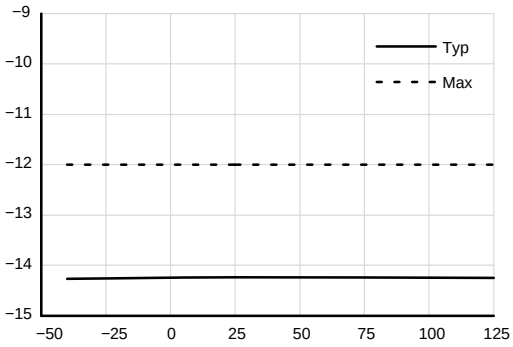


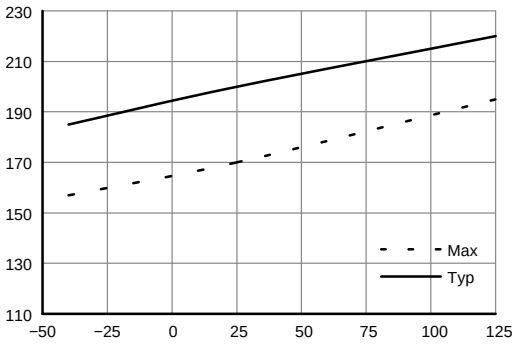
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

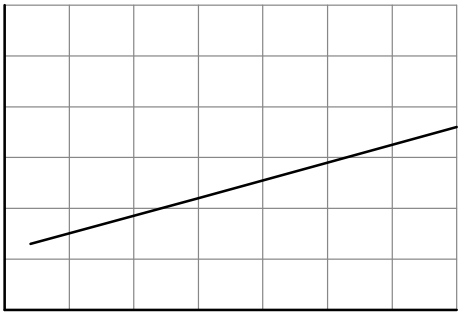
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)







SWITCHING TIME DEFINITIONS

Figure 33. Switching Time and Dead−

APPLICATIONS DESCRIPTION

Power On Reset (POR) Sequence

The purpose of the POR sequence is to ensure that the logic circuitry has reached a stable state after Vdd has ramped up before the gate driver can be operated:

1. Ramp up V_{DD} to the target operating voltage.
2. Wait for t_{POR} to allow the internal logic to settle.
3. Apply a SR pulse for t_{SRMIN} to ensure that the LO output is activated.
4. Provide a sufficient time for the bootstrap capacitor to charge. It is recommended to keep IN low until the bootstrap capacitor is properly charged.
5. Operate the device as intended.

The POR sequence is illustrated in Figure 35.

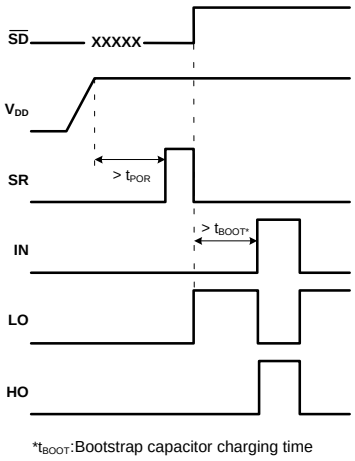


Figure 35. POR Sequence

Shutdown Input ($\overline{SD}$) and Shutdown Reset (SR) Pin

The function of $\overline{SD}$ pin is to enable or disable driver outputs. If the $\overline{SD}$ pin is pulled down externally for t_{SDMIN}, the driver outputs are disabled and the $\overline{SD}$ pin is kept low/latched by the internal pulldown transistor (after $t > t_{SDMIN}$). The function of SR pin is to reset the $\overline{SD}$ pin from its internal latched state. For this, a pulse width of t_{SRMIN} has to be provided to the SR pin. This section describes how to use the $\overline{SD}$ and the SR pins to shutdown the driver outputs, i.e., how to pull down all outputs independently from the input signal, and how to reactivate them.

When the SR pin is in a pulled down state, the $\overline{SD}$ pin is used to trigger a shutdown of the driver outputs and the SR pin is then used to reactivate the outputs. The shutdown (or turn off) sequence when the SR pin is in a pulled down state is described below. Please refer to Figure 36 for details.

- To shutdown the outputs, pull down the $\overline{SD}$ pin externally for a minimum duration of t_{SDMIN}.
- After being pulled down externally, the $\overline{SD}$ pin is kept low/latched by the internal pull down transistor. The equivalent Rdson resistance of the internal pull down transistor in latch mode is around 300 Ω.
- The output of the driver remains turned off (or in a shutdown mode) as long as the $\overline{SD}$ pin is internally pulled down.
- The $\overline{SD}$ pin is released and the outputs are reactivated only when the SR pin is pulled up for a minimum duration of t_{SRMIN}.

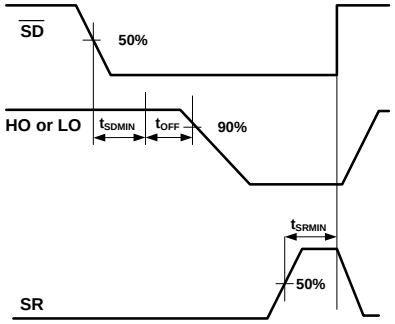


Figure 36. Shutdown with SR Pin Pulled Down − Timing Waveform Definition

Operating and Reset Signal

Important notes: Once the SD pin is pulled down, it should not be externally pulled up, otherwise:

- The driver outputs HO and LO will be reactivated for the duration that $\overline{SD}$ is forced high.
- The $\overline{SD}$ pin will draw additional current through its internal pull down circuit which will needlessly add to the total power dissipation of the IC. With equivalent Rdson resistance of 300 Ω, the internal pull down transistor in latched mode can dissipate additional 83 mW if the $\overline{SD}$ pin is externally forced to 5 V.

To prevent this condition, it is recommended not to force an external state to the $\overline{SD}$ pin after it has latched to a low state. The $\overline{SD}$ pin must have an option to be pulled up by the external pull up resistor RSDext only after a pulse of t_{SRMIN} is provided to the SR pin. This ensures that the internal pull down circuit in the $\overline{SD}$ pin is turned off before the $\overline{SD}$ pin is externally pulled up. To do so, the $\overline{SD}$

Alternate Operating Mode with SR Pin Pulled Up and $\overline{SD}$ Pin Used as Enable

When the SR pin is kept pulled up as shown in Figure 37, the $\overline{SD}$ pin operates like an Enable pin. With the SR pin in a pulled up state:

- When the $\overline{SD}$ pin is pulled down, the outputs are also pulled down (or turned off), irrespective of the status of the input pin.
- When the $\overline{SD}$ pin is pulled up, the outputs are also activated and respond to the input pin.

NOTE: As long as the SR pin is pulled up, the $\overline{SD}$ pin does not draw any current through its internal pull down transistor. The internal pull down transistor remains off when the SR pin is pulled up.

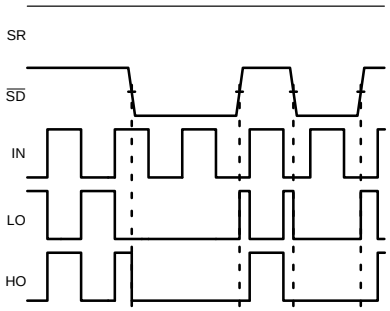


Figure 37. Shutdown with SR Pin Pulled Up

Adjustable Dead time

The dead time between turn off and turn on of the opposite outputs can be adjusted with an external resistor. The relation between the resistor value and the dead time is defined in the Figure 14.

A floating DT pin would not allow any output to turn on. This pin must be connected to ground with a proper resistor.

UVLO

Two independent Under Voltage Lock Out circuitries monitor the V_{BS} voltage and the V_{DD} to V_{SS} voltage.

- If the V_{BS} voltage drops below the negative going threshold voltage, then the output of the high side is pulled down.
- If the V_{DD} voltage drops below the negative going threshold voltage, then the output of the low side as well as the output of the high side is pulled down.

In both cases, the outputs will be reactivated at the next positive edge of the input after the V_{BS}/V_{DD} voltages reach the positive going threshold voltage.

Note that an under voltage lockout event has no impact to the Shutdown functionality and it does not need a signal on the SR pin to reactivate the output.

Pull Up and Pull Down Outputs

The turn on and turn off speed can be defined separately without the need for a diode in the gate resistance path.

HOP and LOP are the pull up output stages that command the turn on of the power switch. The value of R1 and R3 consequently impact the turn on speed.

HON and LON are the pull down output stages that command the turn off of the power switch. The value of R2 and R4 consequently impact the turn off speed.

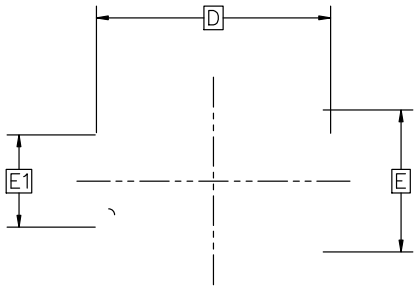
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.1[illegible]

nm TOTAL IN EXCESS OF THE

b DIMENSION AT MAXIMUM MATE

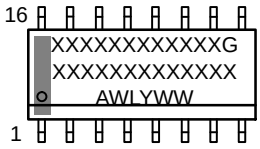


TOP VIEW

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

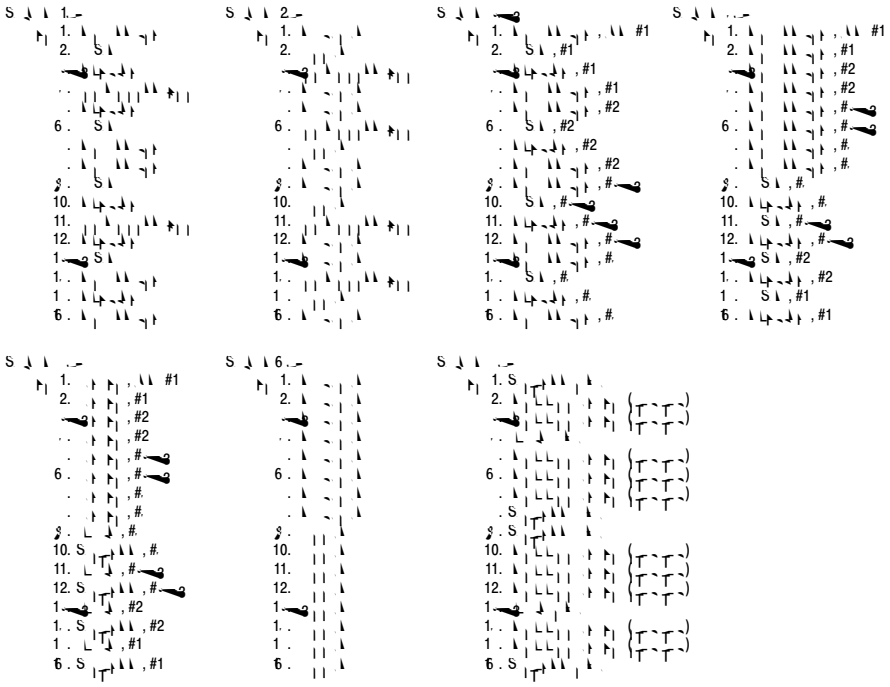
DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



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