B C S a APM16 S M a a S -B PFC S C D

FAM65CR51ADZ1, FAM65CR51ADZ2

Integrated SIP or DIP Boost Converter Stage Power Module for On−board Charger (OBC) in EV or PHEV

Publication Order Number:

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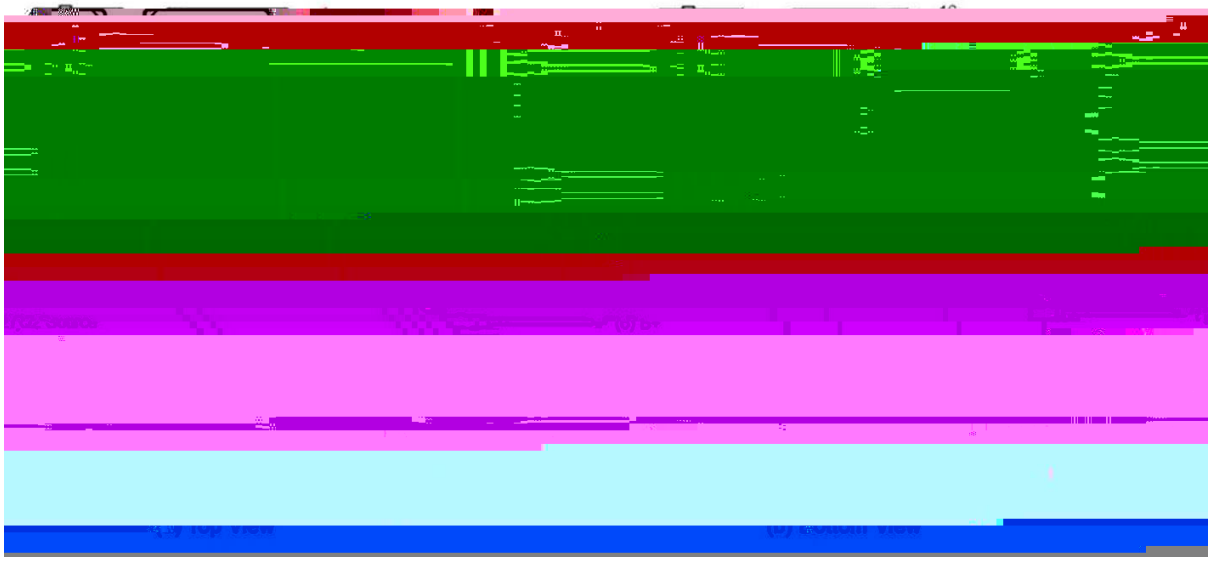
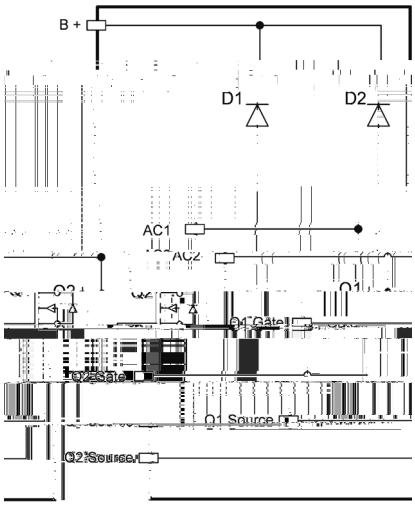
FAM65CR51ADZ1	APM16−CDA	Y−Shape	Al2O3	Yes	−40˚C ~ 125˚C	Tube
FAM65CR51ADZ2	APM16−CDB	L−Shape	Al2O3	Yes	−40˚C ~ 125˚C	Tube





(T_J = 25°C, Unless Otherwise Specified)

V_{DS} (Q1~Q2)	Drain−to−Source Voltage	650	V
V_{GS} (Q1~Q2)	Gate−to−Source Voltage	20	V
I_D (Q1~Q2)	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V) (Note 1)	41	A
	Drain Current Continuous (T_C = 100°C, V_{GS} = 10 V) (Note 1)	25	A
E_{AS} (Q1~Q2)	Single Pulse Avalanche Energy (Note 2)	623	mJ
P_D	Power Dissipation (Note 1)	189	W
T_J	Maximum Junction Temperature	−55 to +150	°C
T_C	Maximum Case Temperature	−40 to +125	°C
T_{STG}	Storage Temperature	−40 to +125	°C

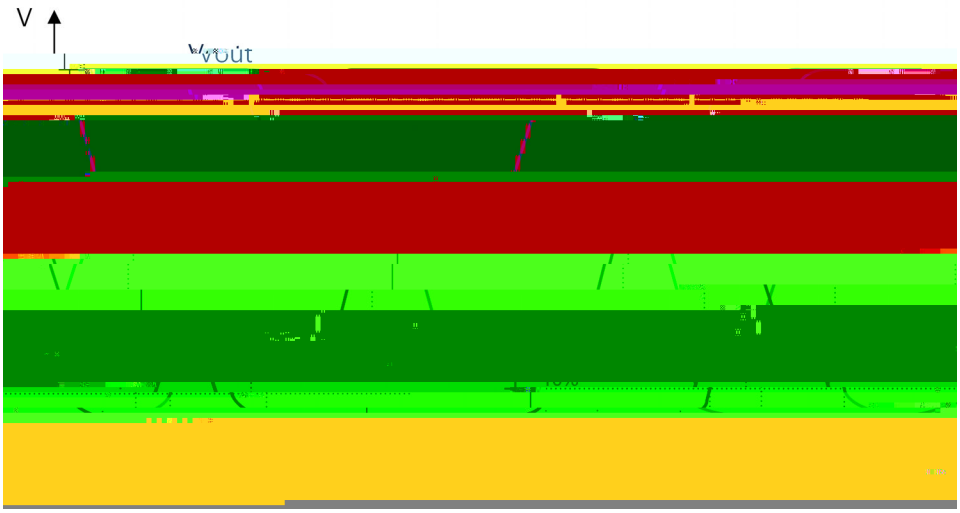
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum continuous current and power, without switching losses, to reach T_J = 150°C respectively at T_C = 25°C and T_C = 100°C; defined by design based on MOSFET $R_{DS(ON)}$ and $R_{\theta JC}$ and not subject to production test
2. Starting T_J = 25°C, I_{AS} = 6.5 A, R_G = 25 Ω

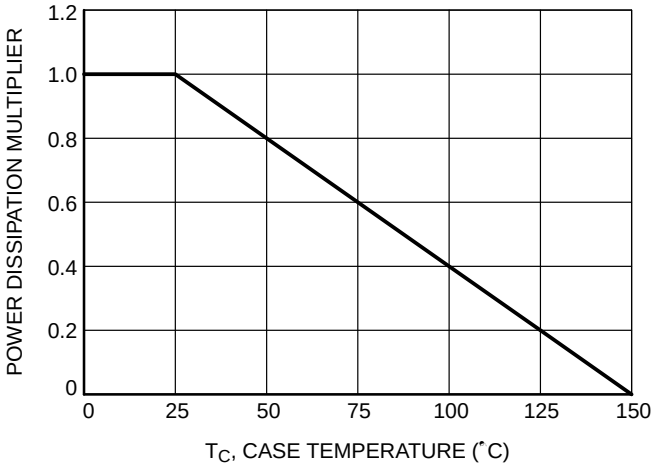
0.63 mm Al2O3 alumina with 0.3 mm copper on both sides.

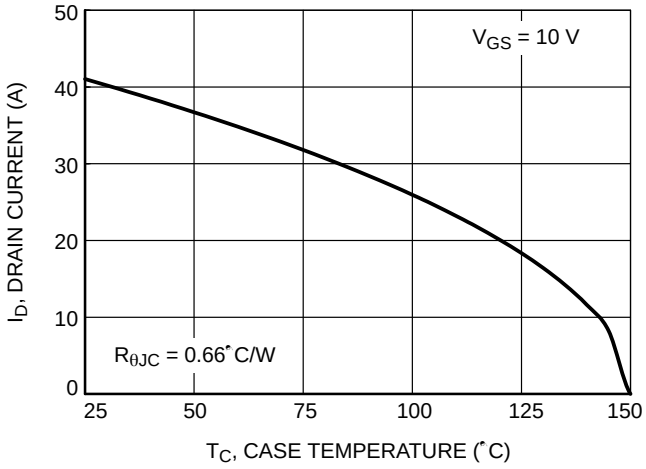
Reference to Table 3: Parameter of MOSFET Electrical Specifications

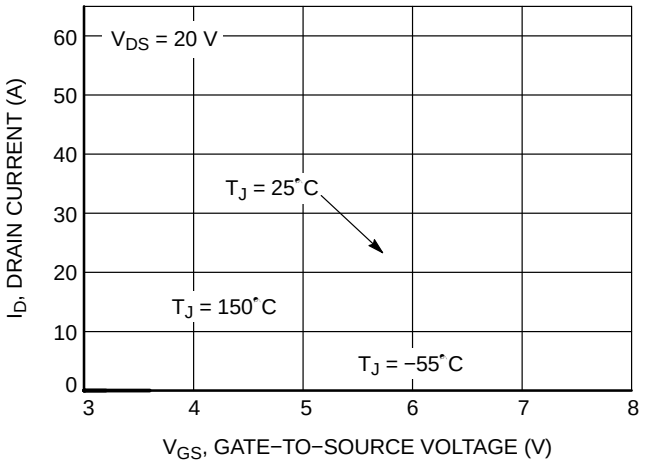
BV_{DSS}	Q1, Q2 MOSFET Drain−to−Source Breakdown Voltage The maximum drain−to−source voltage the MOSFET can endure without the avalanche breakdown of the body− drain P−N junction in off state. The measurement conditions are to be found in Table 3. The typ. Temperature behavior is described in Figure 13
$V_{GS(th)}$	Q1, Q2 MOSFET Gate to Source Threshold Voltage The gate−to−source voltage measurement is triggered by a threshold ID current given in conditions at Table 4. The typ. Temperature behavior can be found in Figure 10
$R_{DS(ON)}$	

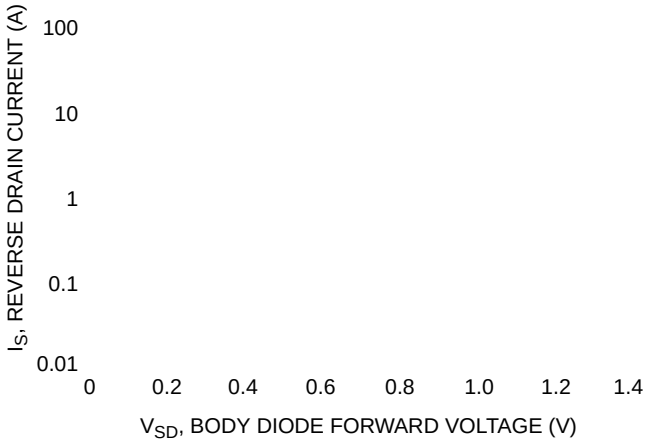


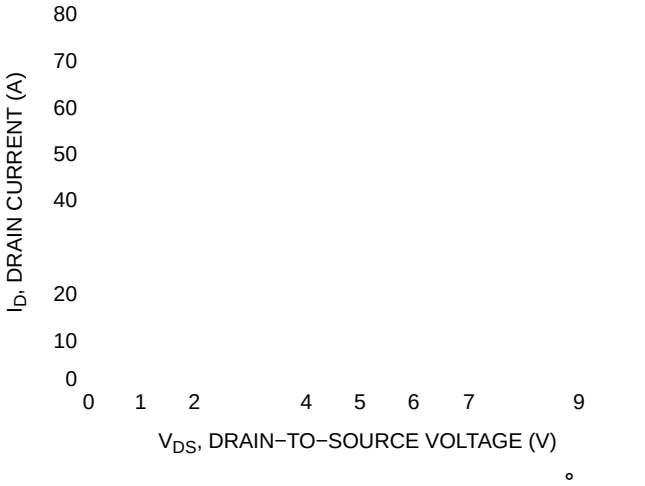
Turn−On Delay ($t_{d(on)}$)	This is the time needed to charge the input capacitance, Ciss, before the load current ID starts flowing. The measurement conditions are described in the Table 3. For signal definition please check Figure 3 above.
Rise Time (t_r)	The rise time is the time to discharge output capacitance, Coss. After that time the MOSFET conducts the given load current ID

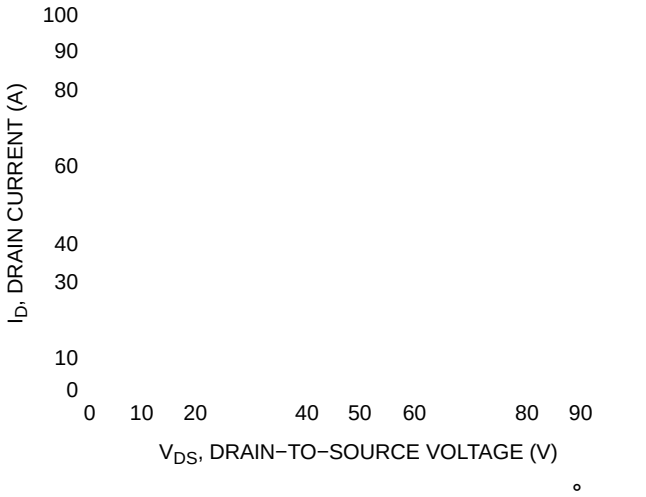

POWER DISSIPATION MULTIPLIER
1.2
1.0
0.8
0.6
0.4
0.2
0
0
25
50
75
100
125
150
T_C, CASE TEMPERATURE (°C)

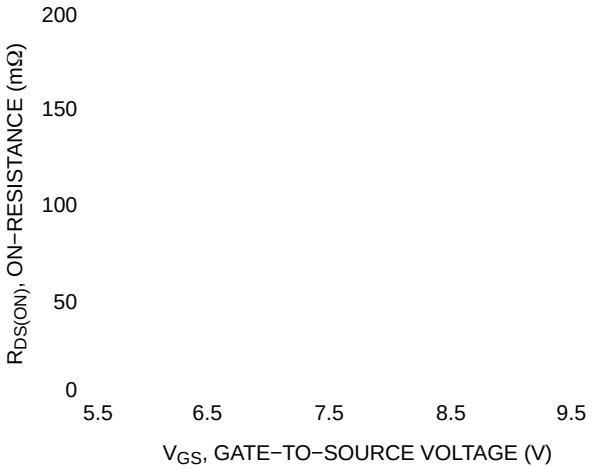

I_D, DRAIN CURRENT (A)
50
40
30
20
10
0
V_{GS} = 10 V
$R_{\theta JC}$ = 0.66°C/W
25
50
75
100
125
150
T_C, CASE TEMPERATURE (°C)

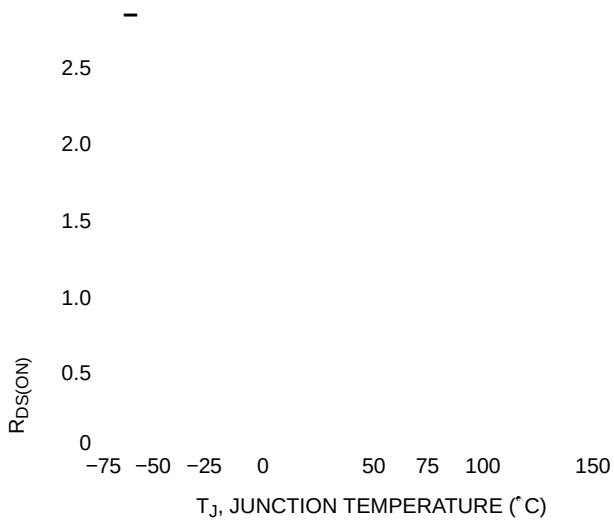

I_D, DRAIN CURRENT (A)
60
50
40
30
20
10
0
V_{DS} = 20 V
T_J = 25°C
T_J = 150°C
T_J = −55°C
3
4
5
6
7
8
V_{GS}, GATE−TO−SOURCE VOLTAGE (V)

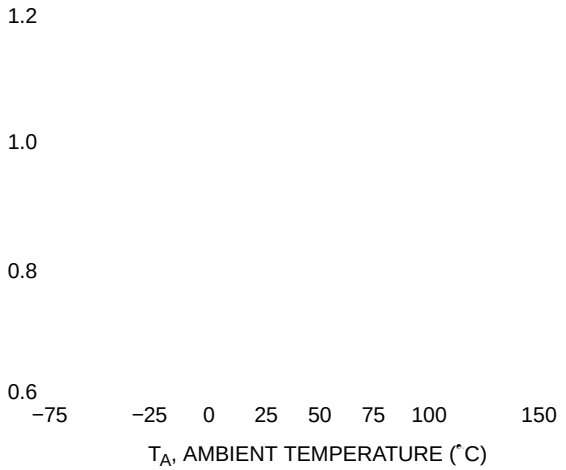

I_S, REVERSE DRAIN CURRENT (A)
100
10
1
0.1
0.01
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
V_{SD}, BODY DIODE FORWARD VOLTAGE (V)

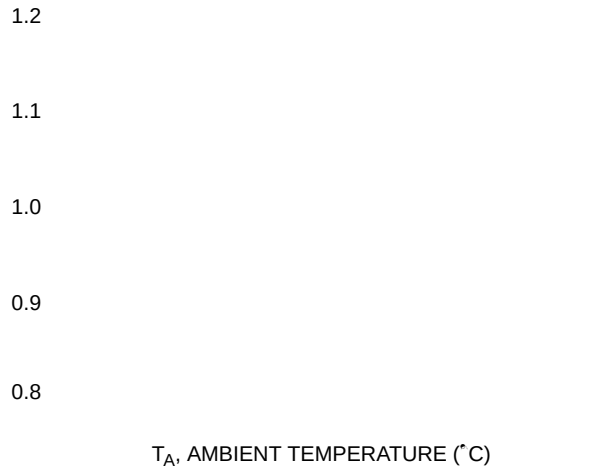

I_D, DRAIN CURRENT (A)
80
70
60
50
40
20
10
0
0
1
2
4
5
6
7
9
V_{DS}, DRAIN−TO−SOURCE VOLTAGE (V)

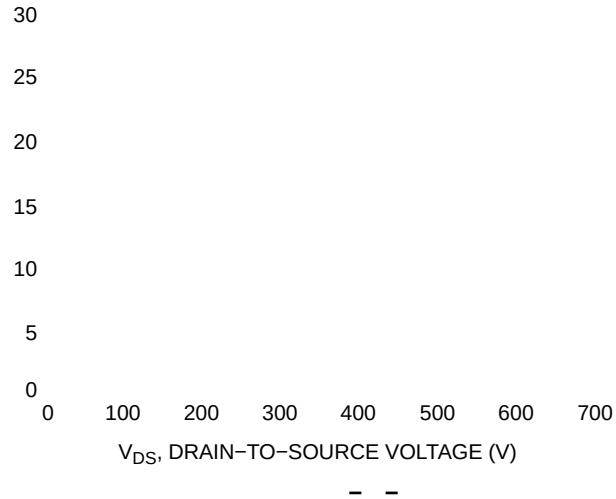

I_D, DRAIN CURRENT (A)
100
90
80
60
40
30
10
0
0
10
20
40
50
60
80
90
V_{DS}, DRAIN−TO−SOURCE VOLTAGE (V)

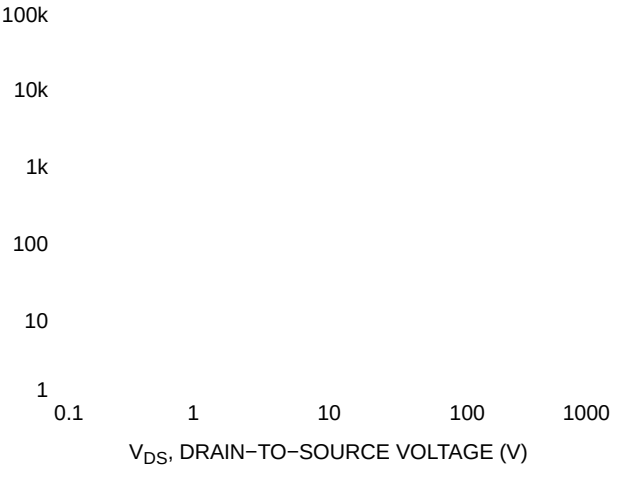

200
150
100
50
0
$R_{DS(ON)}$, ON−RESISTANCE (mΩ)
5.5
6.5
7.5
8.5
9.5
V_{GS}, GATE−TO−SOURCE VOLTAGE (V)

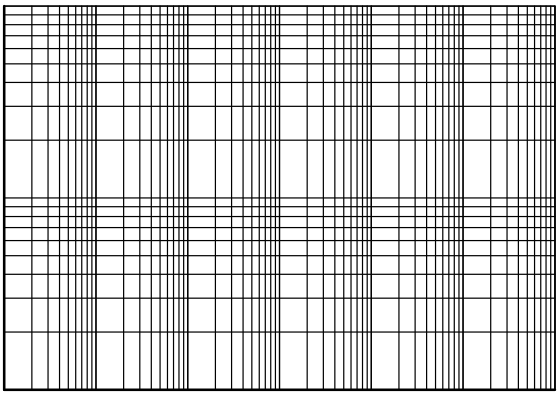

2.5
2.0
1.5
1.0
0.5
0
$R_{DS(ON)}$
−75
−50
−25
0
50
75
100
150
T_J, JUNCTION TEMPERATURE (°C)

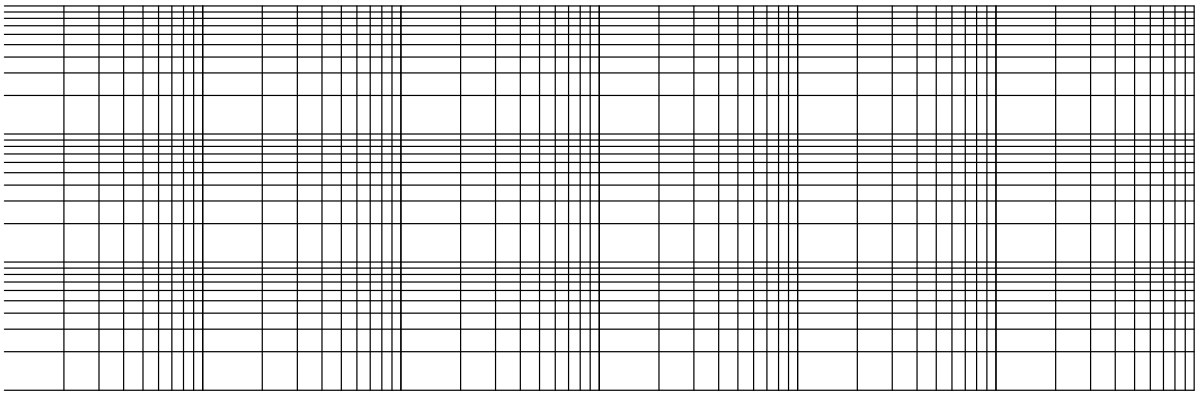

1.2
1.0
0.8
0.6
−75
−25
0
25
50
75
100
150
T_A, AMBIENT TEMPERATURE (°C)


1.2
1.1
1.0
0.9
0.8
T_A, AMBIENT TEMPERATURE (°C)


30
25
20
15
10
5
0
0
100
200
300
400
500
600
700
V_{DS}, DRAIN−TO−SOURCE VOLTAGE (V)


100k
10k
1k
100
10
1
0.1
1
10
100
1000
V_{DS}, DRAIN−TO−SOURCE VOLTAGE (V)





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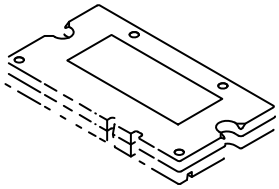
APMCD−A16 / 12LD, AUTOMOTIVE MODULE

1. DIMENSIONING

SION: MILLIMETERS

GENERIC
MARKING DIAGRAM*



APMCD−B16 / 12LD, AUTOMOTIVE MODULE
CASE MODGK
ISSUE D

DATE 04 NOV 2021

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.