nse

INTERNAL EQUIVALENT CIRCUIT

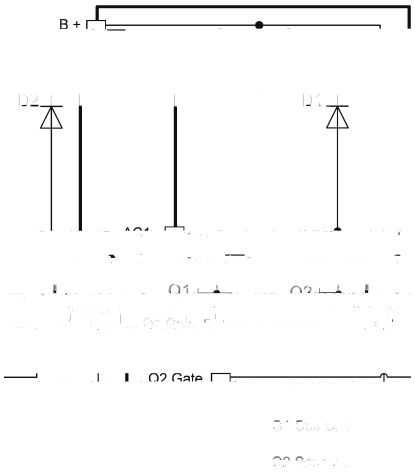


Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS OF MOSFET (T_J = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Max	Unit
V_{DS} (Q1~Q2)	Drain−to−Source Voltage	650	V
V_{GS} (Q1~Q2)	Gate−to−Source Voltage	±20	V
I_D (Q1~Q2)	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V) (Note 1)	33	A
	Drain Current Continuous (T_C = 100°C, V_{GS} = 10 V) (Note 1)	23	A
E_{AS} (Q1~Q2)	Single Pulse Avalanche Energy (Note 2)	623	mJ
P_D	Power Dissipation (Note 1)	160	W
T_J	Maximum Junction Temperature	−55 to +150	°C
T_C	Maximum Case Temperature	−40 to +125	°C°

Table 3. ELECTRICAL SPECIFICATIONS OF MOSFET (T_J = 25°C, Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0 V	650	−	−	V
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 3.3 mA	3.0	−	5.0	V
$R_{DS(ON)}$ Q1	Q1 Low Side MOSFET	V_{GS} = 10 V, I_D = 20 A	−	44	51	mΩ
$R_{DS(ON)}$ Q2	Q2 Low Side MOSFET		−	44	51	mΩ
$R_{DS(ON)}$ Q1	Q1 Low Side MOSFET	V_{GS} = 10 V, I_D = 20 A, T_J = 125°C (Note 3)	−	79	−	mΩ
$R_{DS(ON)}$ Q2	Q2 Low Side MOSFET		−	79	−	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 20 A (Note 3)	−	30	−	S
I_{GSS}	Gate−to−Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	−100	−	+100	nA
I_{DSS}	Drain−to−Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V	−	−	10	μA
DYNAMIC CHARACTERISTICS (Note 3)						
C_{iss}	Input Capacitance	V_{DS} = 400 V V_{GS} = 0 V f = 1 MHz	−	4864	−	pF
C_{oss}	Output Capacitance		−	109	−	pF
C_{rss}	Reverse Transfer Capacitance		−	16	−	pF
$C_{oss(eff)}$	Effective Output Capacitance	V_{DS} = 0 to 520 V V_{GS} = 0 V	−	652	−	pF
R_g	Gate Resistance	f = 1 MHz	−	2	−	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DS} = 380 V I_D = 20 A V_{GS} = 0 to 10 V	−	123	−	nC
Q_{gs}	Gate−to−Source Gate Charge		−	37.5	−	nC
Q_{gd}	Gate−to−Drain “Miller” Charge		−	49	−	nC
SWITCHING CHARACTERISTICS (Note 3)						
t_{on}	Turn−on Time	V_{DS} = 400 V I_D = 20 A V_{GS}				

PARAMETER DEFINITIONS

Reference to Table 3: Parameter of MOSFET Electrical Specifications

BV_{DSS}	Q1, Q2 MOSFET Drain−to−Source Breakdown Voltage The maximum drain−to−source voltage the MOSFET can endure without the avalanche breakdown of the body− drain P−N junction in off state. The measurement conditions are to be found in Table 3. The typ. Temperature behavior is described in Figure 14
$V_{GS(th)}$	Q1, Q2 MOSFET Gate to Source Threshold Voltage The gate−to−source voltage measurement is triggered by a threshold ID current given in conditions at Table 4. The typ. Temperature behavior can be found in Figure 11
$R_{DS(ON)}$	Q1, Q2 MOSFET On Resistance $R_{DS(on)}$ is the total resistance between the source and the drain during the on state. The measurement conditions are to be found in Table 3. The typ behavior can be found in Figure 12 and Figure 13 as well as Figure 18
g_{FS}	Q1, Q2 MOSFET Forward Transconductance Transconductance is the gain in the MOSFET, expressed in the Equation below. It describes the change in drain current by the change in the gate−source bias voltage: $g_{fs} = [\ \Delta I_{DS} / \Delta V_{GS}\ ]_{VDS}$
I_{GSS}	Q1, Q2 MOSFET Gate−to−Source Leakage Current The current flowing from Gate to Source at the maximum allowed V_{GS} The measurement conditions are described in the Table 3.
I_{DSS}	Q1, Q2 MOSFET Drain−to−Source Leakage Current Drain – Source current is measured in off state while providing the maximum allowed drain−to-source voltage and the gate is shorted to the source. I_{DSS} has a positive temperature coefficient.

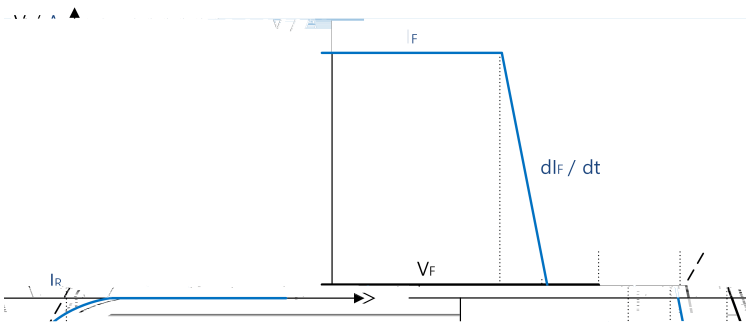


Figure 4. Dynamic Parameters of Silicon Diode (not in scale)

Reference to Table 5: Parameter of Diode Electrical Specifications

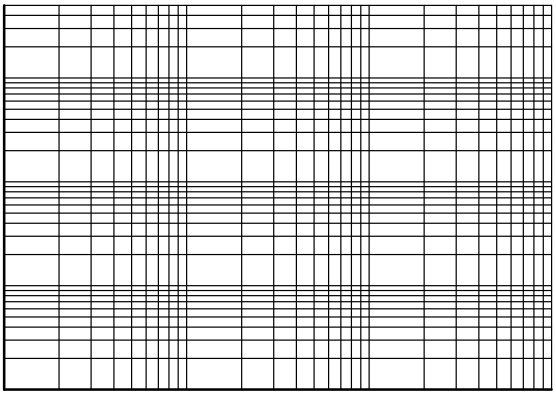
Instantaneous Reverse Current (I_R)	Current flowing in reverse after the reverse recovery time t_{rr}.. I_R is shown in Figure 4 above The behaviour over voltage can be seen in Figure 23.
Instantaneous Forward Voltage V_{FM}	Voltage drop over the diode in a dynamic condition given in Note 5. The voltage is measured after the given test pulse width. To avoid self heating effects a small duty cycle is used The behaviour over voltage can be seen in Figure 22.

TYPICAL CHARACTERISTICS MOSFETs

TYPICAL CHARACTERISTICS MOSFETs

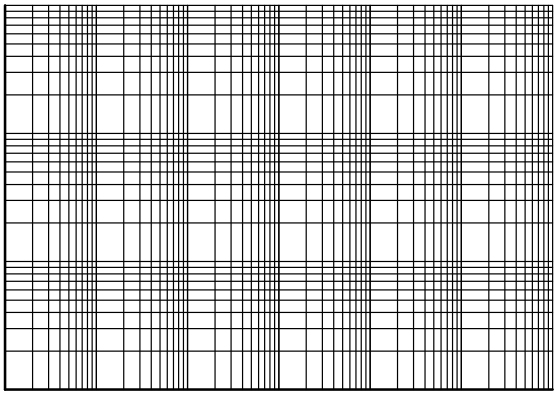
Q_G, GATE CHARGE (nC)

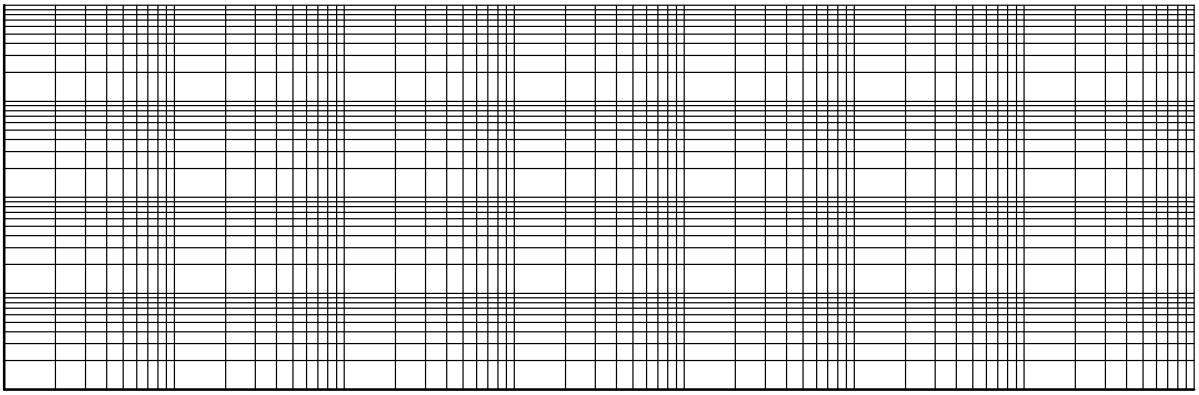
Figure 17. Gate Charge Characteristics



I_D

Figure 18. ON Resistance Variation with Drain Current and Gage Voltage



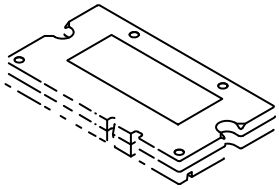


APMCD−A16 / 12LD, AUTOMOTIVE MODULE

1. DIMENSIONING

SION: MILLIMETERS

GENERIC
MARKING DIAGRAM*



APMCD−B16 / 12LD, AUTOMOTIVE MODULE
CASE MODGK
ISSUE D

DATE 04 NOV 2021

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.