

nse



**FAM65CR51DZ1, FAM65CR51DZ2**

# FAM65CR51DZ1, FAM65CR51DZ2

## INTERNAL EQUIVALENT CIRCUIT

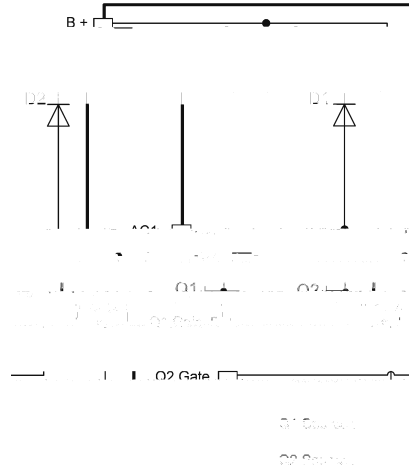


Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS OF MOSFET ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

| Symbol           | Parameter  | Max         | Unit             |
|------------------|--|-------------|------------------|
| $V_{DS}$ (Q1~Q2) | Drain-to-Source Voltage  | 650         | V                |
| $V_{GS}$ (Q1~Q2) | Gate-to-Source Voltage   | $\pm 20$    | V                |
| $I_D$ (Q1~Q2)    | Drain Current Continuous ( $T_C = 25^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ ) (Note 1)  | 33          | A                |
|                  | Drain Current Continuous ( $T_C = 100^\circ\text{C}$ , $V_{GS} = 10\text{ V}$ ) (Note 1) | 23          | A                |
| $E_{AS}$ (Q1~Q2) | Single Pulse Avalanche Energy (Note 2)   | 623         | mJ               |
| $P_D$            | Power Dissipation (Note 1)   | 160         | W                |
| $T_J$            | Maximum Junction Temperature   | -55 to +150 | $^\circ\text{C}$ |
| $T_C$            | Maximum Case Temperature   | -40 to +125 | $^\circ\text{C}$ |

## FAM65CR51DZ1, FAM65CR51DZ2

**Table 3. ELECTRICAL SPECIFICATIONS OF MOSFET** ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)

| Symbol          | Parameter                         | Conditions  | Min  | Typ | Max  | Unit             |
|-----------------|-----------------------------------|---|------|-----|------|------------------|
| $BV_{DSS}$      | Drain-to-Source Breakdown Voltage | $I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$                                    | 650  | –   | –    | V                |
| $V_{GS(th)}$    | Gate-to-Source Threshold Voltage  | $V_{GS} = V_{DS}, I_D = 3.3\text{ mA}$                                      | 3.0  | –   | 5.0  | V                |
| $R_{DS(ON)} Q1$ | Q1 Low Side MOSFET                | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}$                                   | –    | 44  | 51   | $\text{m}\Omega$ |
| $R_{DS(ON)} Q2$ | Q2 Low Side MOSFET                |   | –    | 44  | 51   | $\text{m}\Omega$ |
| $R_{DS(ON)} Q1$ | Q1 Low Side MOSFET                | $V_{GS} = 10\text{ V}, I_D = 20\text{ A}, T_J = 125^\circ\text{C}$ (Note 3) | –    | 79  | –    | $\text{m}\Omega$ |
| $R_{DS(ON)} Q2$ | Q2 Low Side MOSFET                |   | –    | 79  | –    | $\text{m}\Omega$ |
| $g_{FS}$        | Forward Transconductance          | $V_{DS} = 20\text{ V}, I_D = 20\text{ A}$ (Note 3)                          | –    | 30  | –    | S                |
| $I_{GSS}$       | Gate-to-Source Leakage Current    | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$                             | –100 | –   | +100 | nA               |
| $I_{DSS}$       | Drain-to-Source Leakage Current   | $V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$                                | –    | –   | 10   | $\mu\text{A}$    |

### DYNAMIC CHARACTERISTICS (Note 3)

|                |                               |  |   |      |   |          |
|----------------|-------------------------------|--|---|------|---|----------|
| $C_{iss}$      | Input Capacitance             | $V_{DS} = 400\text{ V}$<br>$V_{GS} = 0\text{ V}$<br>$f = 1\text{ MHz}$               | – | 4864 | – | pF       |
| $C_{oss}$      | Output Capacitance            |  | – | 109  | – | pF       |
| $C_{rss}$      | Reverse Transfer Capacitance  |  | – | 16   | – | pF       |
| $C_{oss(eff)}$ | Effective Output Capacitance  | $V_{DS} = 0\text{ to }520\text{ V}$<br>$V_{GS} = 0\text{ V}$                         | – | 652  | – | pF       |
| $R_g$          | Gate Resistance               | $f = 1\text{ MHz}$   | – | 2    | – | $\Omega$ |
| $Q_{g(tot)}$   | Total Gate Charge             | $V_{DS} = 380\text{ V}$<br>$I_D = 20\text{ A}$<br>$V_{GS} = 0\text{ to }10\text{ V}$ | – | 123  | – | nC       |
| $Q_{gs}$       | Gate-to-Source Gate Charge    |  | – | 37.5 | – | nC       |
| $Q_{gd}$       | Gate-to-Drain "Miller" Charge |  | – | 49   | – | nC       |

### SWITCHING CHARACTERISTICS (Note 3)

|          |              |  |
|----------|--------------|--|
| $t_{on}$ | Turn-on Time | $V_{DS} = 400\text{ V}$<br>$I_D = 20\text{ A}$<br>$V_{GS}$ |
|----------|--------------|--|



# FAM65CR51DZ1, FAM65CR51DZ2

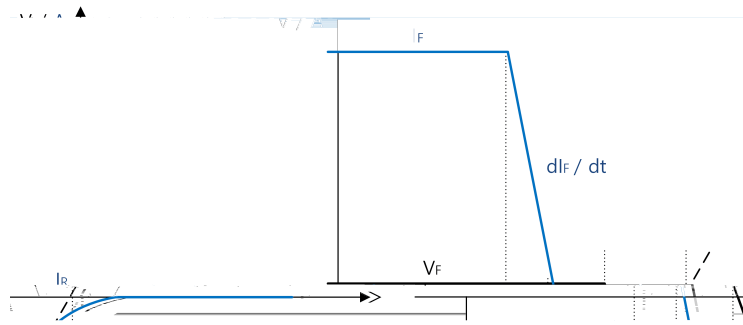
## PARAMETER DEFINITIONS

Reference to Table 3: Parameter of MOSFET Electrical Specifications

|              |   |
|--------------|---|
| $BV_{DSS}$   | <p>Q1, Q2 MOSFET Drain-to-Source Breakdown Voltage</p> <p>The maximum drain-to-source voltage the MOSFET can endure without the avalanche breakdown of the body-drain P-N junction in off state.</p> <p>The measurement conditions are to be found in Table 3.</p> <p>The typ. Temperature behavior is described in Figure 14</p> |
| $V_{GS(th)}$ | <p>Q1, Q2 MOSFET Gate to Source Threshold Voltage</p> <p>The gate-to-source voltage measurement is triggered by a threshold ID current given in conditions at Table 4.</p> <p>The typ. Temperature behavior can be found in Figure 11</p>   |
| $R_{DS(on)}$ | <p>Q1, Q2 MOSFET On Resistance</p> <p><math>R_{DS(on)}</math> is the total resistance between the source and the drain during the on state.</p> <p>The measurement conditions are to be found in Table 3.</p> <p>The typ behavior can be found in Figure 12 and Figure 13 as well as Figure 18</p>                                |
| $g_{fs}$     | <p>Q1, Q2 MOSFET Forward Transconductance</p> <p>Transconductance is the gain in the MOSFET, expressed in the Equation below.</p> <p>It describes the change in drain current by the change in the gate-source bias voltage: <math>g_{fs} = [\Delta I_{DS} / \Delta V_{GS}]_{V_{DS}}</math></p>                                   |
| $I_{GSS}$    | <p>Q1, Q2 MOSFET Gate-to-Source Leakage Current</p> <p>The current flowing from Gate to Source at the maximum allowed VGS</p> <p>The measurement conditions are described in the Table 3.</p>   |
| $I_{DSS}$    | <p>Q1, Q2 MOSFET Drain-to-Source Leakage Current</p> <p>Drain - Source current is measured in off state while providing the maximum allowed drain-to-source voltage and the gate is shorted to the source.</p> <p><math>I_{DSS}</math> has a positive temperature coefficient.</p>  |

**FAM65CR51DZ1, FAM65CR51DZ2**

## FAM65CR51DZ1, FAM65CR51DZ2



**Figure 4. Dynamic Parameters of Silicon Diode (not in scale)**

Reference to Table 5: Parameter of Diode Electrical Specifications

|  |  |
|--|--|
| Instantaneous Reverse Current<br>( $I_R$ ) | Current flowing in reverse after the reverse recovery time $t_{rr}$ .<br>$I_R$ is shown in Figure 4 above<br>The behaviour over voltage can be seen in Figure 23.  |
| Instantaneous Forward Voltage<br>$V_{FM}$  | Voltage drop over the diode in a dynamic condition given in Note 5.<br>The voltage is measured after the given test pulse width.<br>To avoid self heating effects a small duty cycle is used<br>The behaviour over voltage can be seen in Figure 22. |



**FAM65CR51DZ1, FAM65CR51DZ2**

**FAM65CR51DZ1, FAM65CR51DZ2**

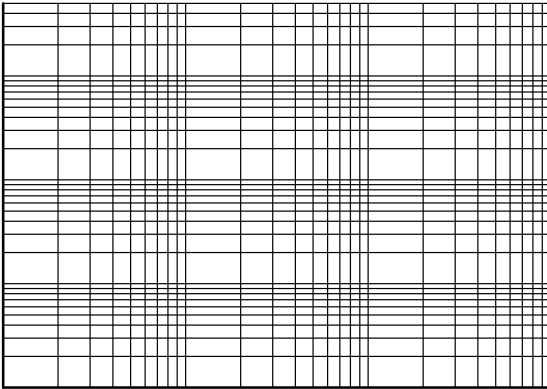
**TYPICAL CHARACTERISTICS MOSFETs**

# FAM65CR51DZ1, FAM65CR51DZ2

## TYPICAL CHARACTERISTICS MOSFETs

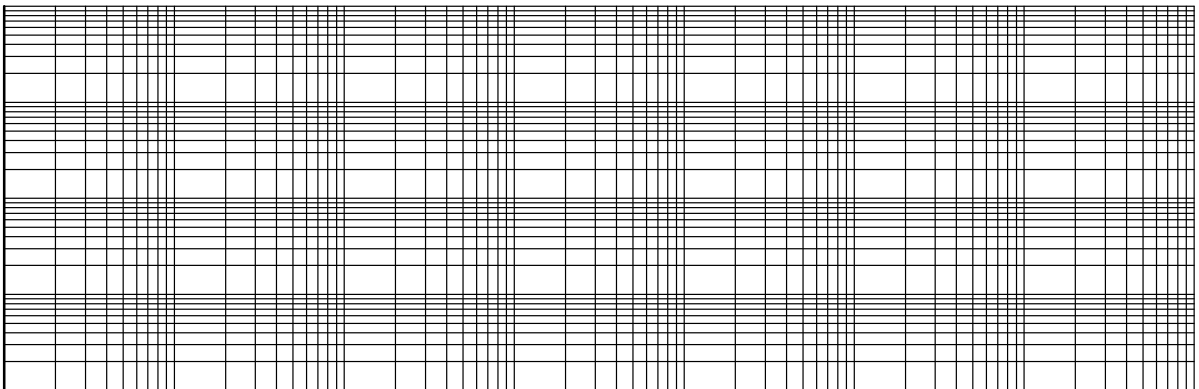
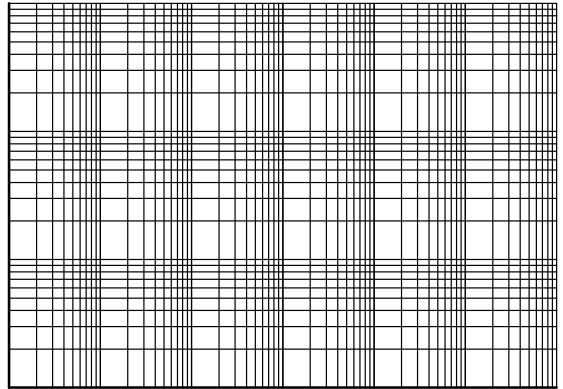
$Q_G$ , GATE CHARGE (nC)

**Figure 17. Gate Charge Characteristics**



$I_D$

**Figure 18. ON Resistance Variation with Drain Current and Gate Voltage**





**FAM65CR51DZ1, FAM65CR51DZ2**

**APMCD-A16 / 12LD, AUTOMOTIVE MODULE**



|

**1. DIMENSIONS**

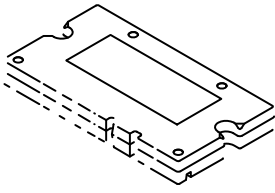
UNITS: MILLIMETERS

**GENERIC  
MARKING DIAGRAM\***



-

■



**APMCD-B16 / 12LD, AUTOMOTIVE MODULE**  
CASE MODGK  
ISSUE D

DATE 04 NOV 2021

**GENERIC  
MARKING DIAGRAM\***

XXXX = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly & Test Location  
Y = Year  
W = Work Week  
NNN = Serial Number

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

**onsemi**, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**

---

---