Boost Converter Stage in APM16 Series for Multiphase and Semi-Bridgeless PFC

FAM65CR51XZ1, FAM65CR51XZ2

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Features

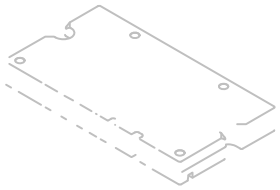
- Integrated SIP or DIP Boost Converter Stage Power Module for On−board Charger (OBC) in EV or PHEV
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Creepage and Clearance per IEC60664−1, IEC 60950−1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Low Thermal Resistance Due to the Used ALN Substrate
- AEC−Q101 & AQG324 Qualified and PPAP Capable
- UL94V−0 Compliant
- These Devices are Pb−Free and are RoHS Compliant

Applications

- PFC Stage of an On−board Charger in PHEV or EV

Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO_2 Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



XXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
WW = Work Week
NNN = Serial Number

ORDERING INFORMATION

Part Number	Package	Lead Forming	DBC Material	Pb−Free and RoHS Compliant	Operating Temperature (Ta)	Shipping
FAM65CR51XZ1	APMCD−A16	Y−Shape	AlN	Yes	−40°C~125°C	72 Units / Tube
FAM65CR51XZ2	APMCD−B16	L−Shape	AlN	Yes	−40°C~125°C	72 Units / Tube

Pin Configuration and Block Description

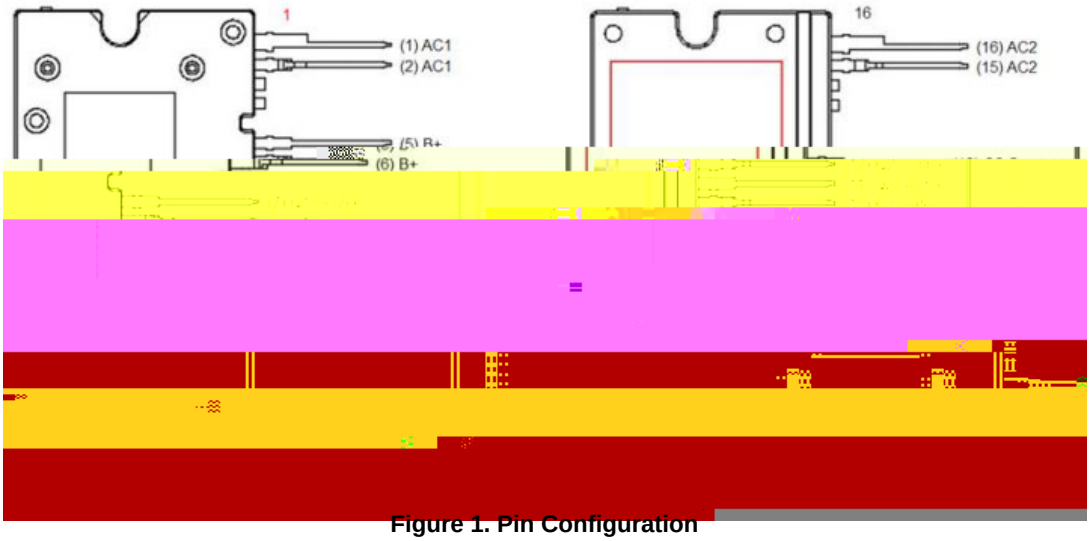


Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

Pin No.	Name	Description
1, 2	AC1	Phase 1 Leg of the PFC Bridge
3	NC	Not Connected
4	NC	Not Connected
5, 6	B+	Positive Battery Terminal
7, 8	Q1 Source	Source Terminal of Q1
9	Q1 Gate	Gate Terminal of Q1
10	Q2 Gate	Gate Terminal of Q2
11, 12	Q2 Source	Source Terminal of Q2
13	NC	Not Connected
14	NC	Not Connected
15, 16	AC2	Phase 2 Leg of the PFC Bridge

INTERNAL EQUIVALENT CIRCUIT

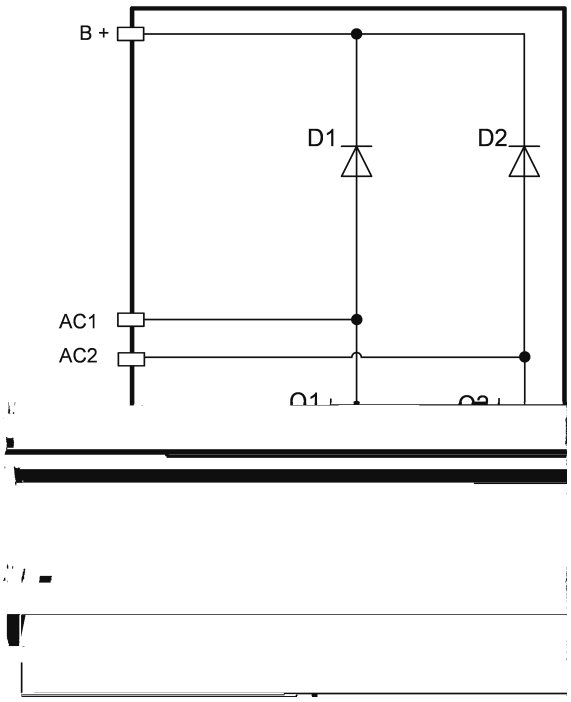


Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS OF MOSFET (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Max	Unit
V_{DS} (Q1~Q2)	Drain−to−Source Voltage	650	V
V_{GS} (Q1~Q2)	Gate−to−Source Voltage	±20	V
I_D (Q1~Q2)	Drain Current Continuous (T_C = 25°C, V_{GS} = 10 V) (Note 1)	64	A
	Drain Current Continuous (T_C = 100°C, V_{GS} = 10 V) (Note 1)	40	A
E_{AS} (Q1~Q2)	Single Pulse Avalanche Energy (Note 2)	623	mJ
P_D	Power Dissipation (T_C = 25°C, V_{GS} = 10 V) (Note 1)	463	W
T_J	Maximum Junction Temperature	−55 to +150	°C
T_C	Maximum Case Temperature	−40 to +125	°C
T_{STG}	Storage Temperature	−40 to +125	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum continuous current and power, without switching losses, to reach T_J = 150°C respectively at T_C = 25°C and T_C = 100°C; defined by design based on MOSFET $R_{DS(ON)}$ and max. $R_{\theta JC}$ and not subject to production test
2. Starting T_J = 25°C, I_{AS} = 6.5 A, R_G = 25 Ω

DBC Substrate

0.63 mm AlN

Table 4. ABSOLUTE MAXIMUM RATINGS OF THE BOOST DIODE (T_J = 25°C unless otherwise noted) (Note 4)

Symbol	Parameter	Max	Unit
V_{RRM}	Peak Repetitive Reverse Voltage (Note 5)	600	V
V_{RWM}	Working Peak Reverse Voltage (Note 5)	600	V
V_R	DC Blocking Voltage	600	V
$I_{F(AV)}$	Average Rectified Forward Current T_C = 25°C	15	A
I_{FSM}	Non−Repetitive Peak Surge Current (Half Wave 1 Phase 60 Hz)	45	A
T_J	Maximum Junction Temperature	−55 to +175	°C
T_C	Maximum Case Temperature	−40 to +125	°C
T_{STG}	Storage Temperature	−40 to +125	°C
E_{AVL}	Avalanche Energy (2.85 A, 1 mH)	4	mJ

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Defined by design, not subject to production test
5. V_{RRM} and $I_{F(AV)}$ value referenced to TO220−2L Auto Qualified Package Device ISL9R1560P_F085

Table 5. ELECTRICAL SPECIFICATIONS OF THE BOOST DIODE (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
I_R	Instantaneous Reverse Current	V_R = 600 V	T_C = 25°C	−	−	100	μA
			T_C = 125°C	−	−	1	mA
V_{FM}	Instantaneous Forward Voltage (Note 7)	I_F = 15 A	T_C = 25°C	−	1.65	2.2	V
			T_C = 125°C	−	1.24	1.7	V
t_{rr}	Reverse Recovery Time	I_F = 15 A d_{IF}/dt = 200 A/μs V_R = 390 V (Note 6)	T_C = 25°C	−	29	−	ns
t_a	Time to reach peak reverse current		T_C = 25°C	−	16	−	ns
t_b	Time from peak I_{RRM} to projected zero crossing of I_{RRM} based on a straight line from peak I_{RRM} through 25% of I_{RRM}		T_C = 25°C	−	13	−	ns
Q_{rr}	Reverse Recovered Charge		T_C = 25°C	−	43	−	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Defined by design, not subject to production test
7. Test pulse width = 300 μs, Duty Cycle = 2%

Table 6. THERMAL RESISTANCE

Parameters		Min	Typ	Max	Unit
$R_{\theta JC}$ (per MOSFET chip)	Q1, Q2 Thermal Resistance Junction−to−Case (Note 8)	−	0.19	0.27	°C/W
$R_{\theta JS}$ (per MOSFET chip)	Q1, Q2 Thermal Resistance Junction−to−Sink (Note 9)	−	0.62	−	°C/W
$R_{\theta JC}$ (per DIODE chip)	D1, D2 Thermal Resistance Junction−to−Case (Note 8)	−	0.74	1.1	°C/W
$R_{\theta JS}$ (per DIODE chip)	D1, D2 Thermal Resistance Junction−to−Sink (Note 9)	−	1.65	−	°C/W

8. $R_{\theta JC\ (junction\ to\ case)}$Test method compliant with MIL STD 883−1012.1, from case temperature under the chip to case temperature measured below the package at the chip center, Cosmetic oxidation and

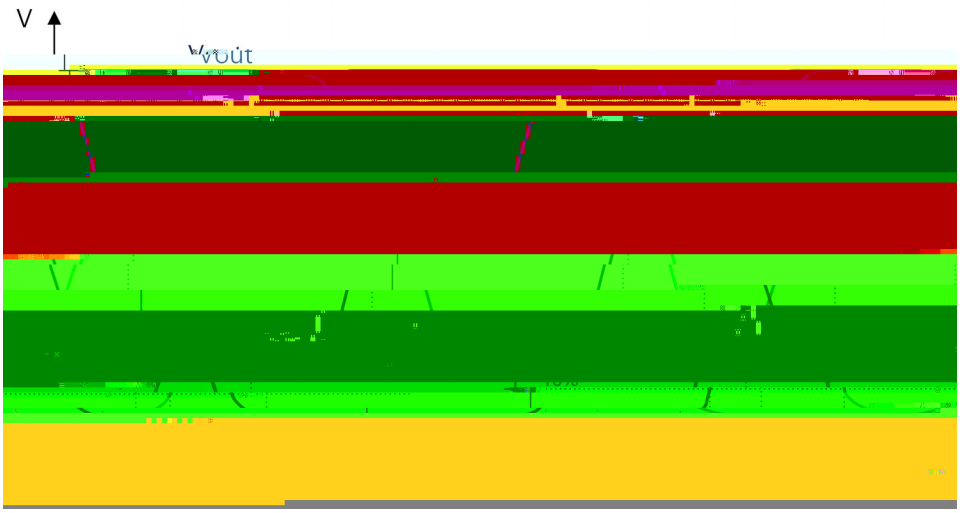
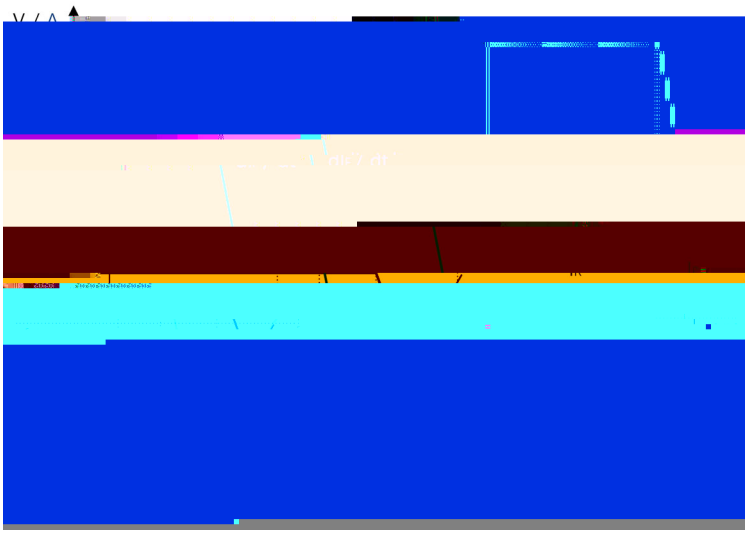


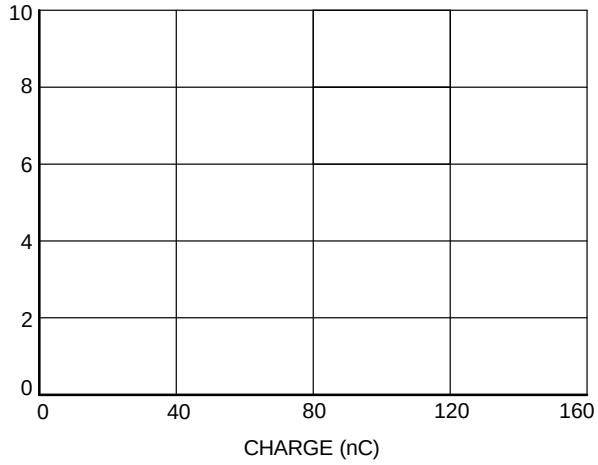
Figure 3. Timing Measurement Variable Definition

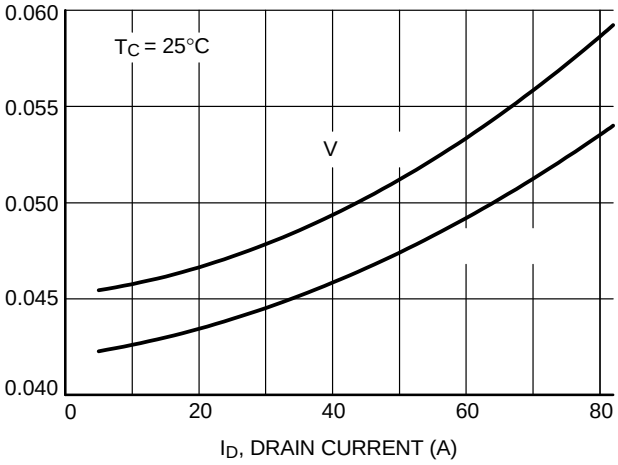
Table 9. PARAMETER OF SWITCHING CHARACTERISTICS

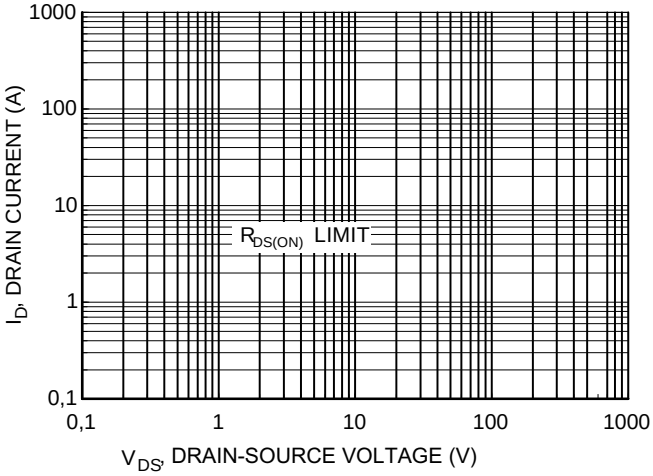
Turn−On Delay (t

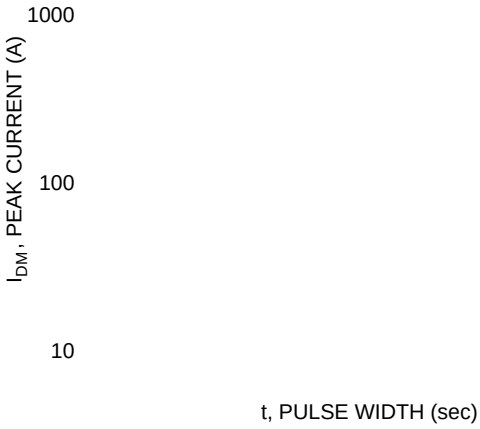


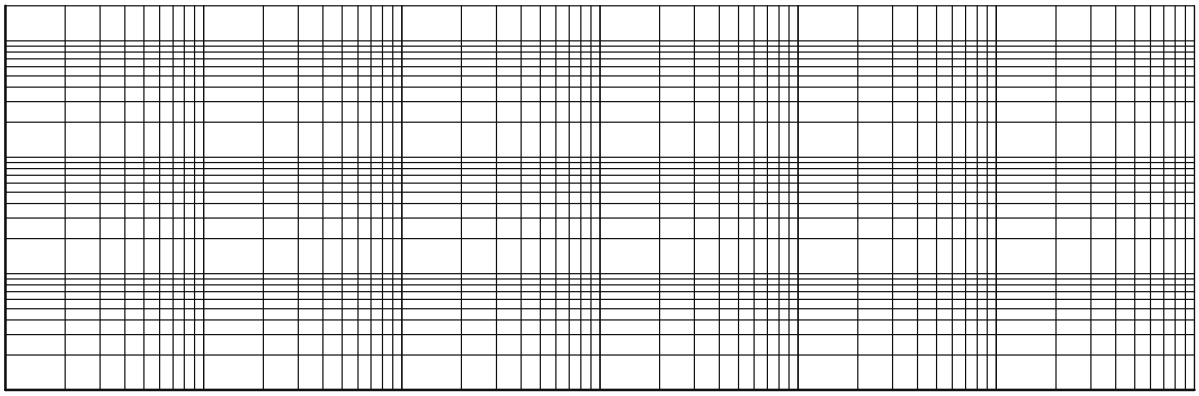
TYPICAL CHARACTERISTICS – MOSFETS (continued)











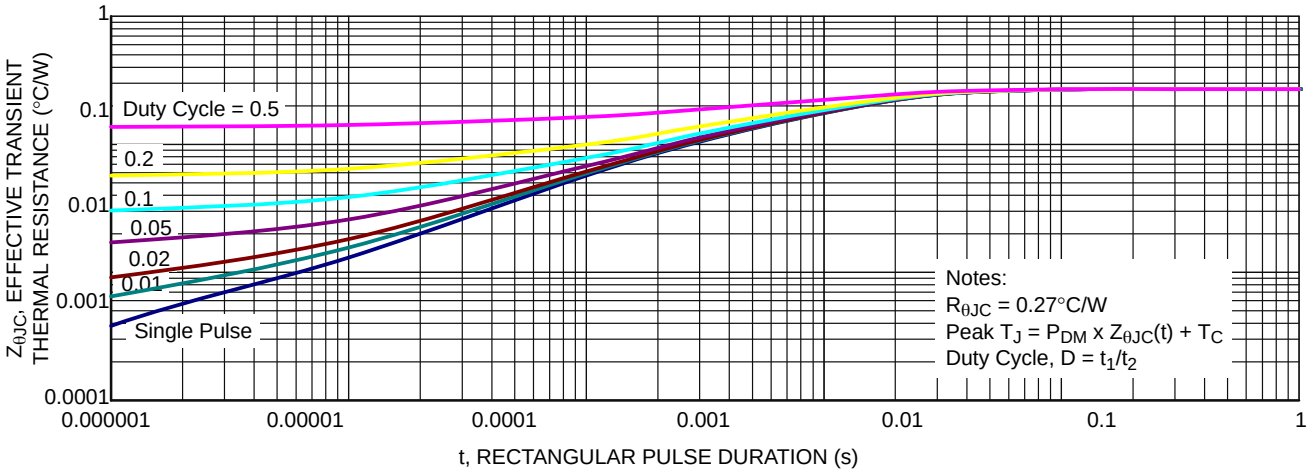


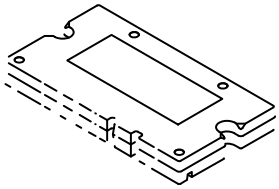
Figure 28. Transient Thermal Impedance

APMCD−A16 / 12LD, AUTOMOTIVE MODULE

1. DIMENSIONING

SION: MILLIMETERS

GENERIC
MARKING DIAGRAM*



APMCD−B16 / 12LD, AUTOMOTIVE MODULE
CASE MODGK
ISSUE D

DATE 04 NOV 2021

GENERIC
MARKING DIAGRAM*

XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.