

H-Bridge in APM16 Series for LLC and Phase-shifted DC-DC Converter

FAM65HR51DS2

Features

- SIP or DIP H-Bridge Power Module for On-board Charger (OBC) in EV or PHEV
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Creepage and Clearance per IEC60664-1, IEC 60950-1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, RoHS and UL94V-0 Compliant
- Automotive Qualified per AEC Q101 and AQG324 Guidelines

Applications

- DC-DC Converter for On-board Charger in EV or PHEV

Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and CO₂ Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance



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APMCA-B16
16 LEAD
CASE MODGJ



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

FAM65HR51DS2

ORDERING INFORMATION

Part Number	Package	Lead Forming	Snubber Capacitor Inside	DBC Material	Pb-Free and RoHS Compliant	Operating Temperature (T _A)	Packing Method
FAM65HR51DS2	APM16-CAB	L-Shape	Yes	Al ₂ O ₃	Yes		

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Table 4. ELECTRICAL SPECIFICATIONS ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-to-Source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0 \text{ V}$	650	–	–	V
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 3.3 \text{ mA}$	3.0	–	5.0	V
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	–	44	51	$\text{m}\Omega$
$R_{DS(ON)}$	Q1 – Q4 MOSFET On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$, $T_J = 125^\circ\text{C}$ (Note 4)	–	79	–	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}$, $I_D = 20 \text{ A}$ (Note 4)	–	30	–	S
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$	–100	–	+100	nA
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 650 \text{ V}$, $V_{GS} = 0 \text{ V}$	–	–	10	μA

DYNAMIC CHARACTERISTICS (Note 4)

C_{iss}	Input Capacitance	$V_{DS} = 400 \text{ V}$ $V_{GS} = 0 \text{ V}$ $f = 1 \text{ MHz}$	–	4864	–	pF
C_{oss}	Output Capacitance		–	109	–	pF
C_{rss}	Reverse Transfer Capacitance		–	16	–	pF
$C_{oss(eff)}$	Effective Output Capacitance	$V_{DS} = 0 \text{ to } 520 \text{ V}$ $V_{GS} = 0 \text{ V}$	–	652	–	pF
R_g	Gate Resistance	$f = 1 \text{ MHz}$	–	2	–	Ω
$Q_{g(tot)}$ Q	Total Gate Charge	$V_{DS} = 380 \text{ V}$ $I_D = 20 \text{ A}$ $V_{GS} = 0 \text{ to } 10 \text{ V}$	–	123	–	nC

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PARAMETER DEFINITIONS

Reference to Table 4: Parameter of Electrical Specifications

BV_{DSS}	Q1 – Q4 MOSFET Drain-to-
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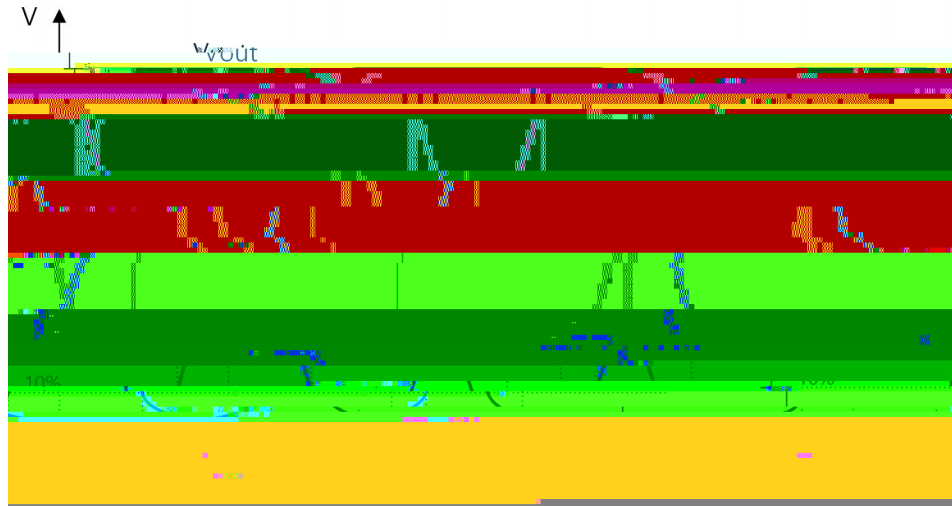


Figure 3. Timing Measurement Variable Definition

Table 7. PARAMETER OF SWITCHING CHARACTERISTICS

Turn-On Delay ($t_{d(on)}$)	This is the time needed to charge the input capacitance, C_{iss} , before the load current I_D starts flowing. The measurement conditions are described in the Table 4. For signal definition please check Figure 3 above.
Rise Time (t_r)	The rise time is the time to discharge output capacitance, C_{oss} . After that time the MOSFET conducts the given load current I_D . The measurement conditions are described in the Table 4. For signal definition please check Figure 3 above.
Turn-On Time (t_{on})	Is the sum of turn-on-delay and rise time
Turn-Off Delay ($t_{d(off)}$)	$t_{d(off)}$ is the time to discharge C_{iss} after the MOSFET is turned off. During this time the load current I_D is still flowing. The measurement conditions are described in the Table 4. For signal definition please check Figure 3 above.
Fall Time (t_f)	The fall time, t_f , is the time to charge the output capacitance, C_{oss} . During this time the load current drops down and the voltage V_{DS}

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TYPICAL CHARACTERISTICS

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TYPICAL CHARACTERISTICS

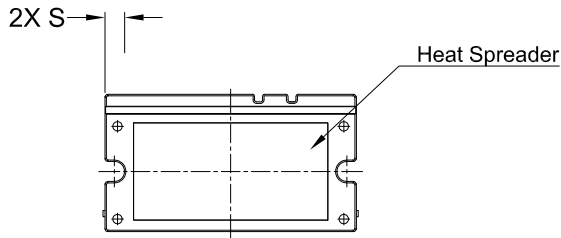
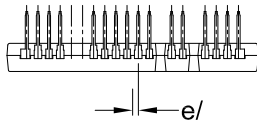
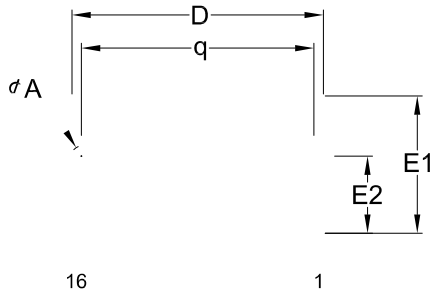
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Figure 10. On-Resistance vs. Gate-to-Source Voltage

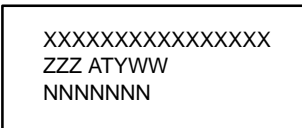
Figure 11. $R_{DS(norm)}$ vs. Junction Temperature

PIM16 40.10x21.90x4.50
CASE MODGJ
ISSUE D

DATE 17 JAN 2024



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- ZZZ = Lot ID
- AT = Assembly & Test Location
- Y = Year
- W = Work Week
- NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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