onsemi

DATA SHEET
www.onsemi.com

Features

- SIP or DIP H−Bridge Power Module for On−board Charger (OBC) in EV or PHEV
- 5 kV/1 sec Electrically Isolated Substrate for Easy Assembly
- Creepage and Clearance per IEC60664−1, IEC 60950−1
- Compact Design for Low Total Module Resistance
- Module Serialization for Full Traceability
- Lead Free, RoHS and UL94V−0 Compliant
- Automotive Qualified per AEC Q101 and AQG324 Guidelines

Applications

- DC−DC Converter for On−board Charger in EV or PHEV

Benefits

- Enable Design of Small, Efficient and Reliable System for Reduced Vehicle Fuel Consumption and $CO_2$ Emission
- Simplified Assembly, Optimized Layout, High Level of Integration, and Improved Thermal Performance

APMCA−B16
16 LEAD
CASE MODGJ

MARKING DIAGRAM

XXXXXXXXXXX
ZZZ ATYWW
NNNNNNN

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 2 of this data sheet.

© Semiconductor Components Industries, LLC, 2020

## ORDERING INFORMATION

| Part Number | Package | Lead Forming | Snubber Capacitor Inside | DBC Material | Pb−Free and RoHS Compliant | Operating Temperature ($T_A$) | Packing Method |
|---|---|---|---|---|---|---|---|
| FAM65HR51XS1 | APM16−CAA | Y−Shape | Yes | ALN | Yes | −40°C ~ 125°C | Tube |
| FAM65HR51XS2 | APM16−CAB | L−Shape | Yes | ALN | Yes | −40°C ~ 125°C | Tube |

## Pin Configuration and Description

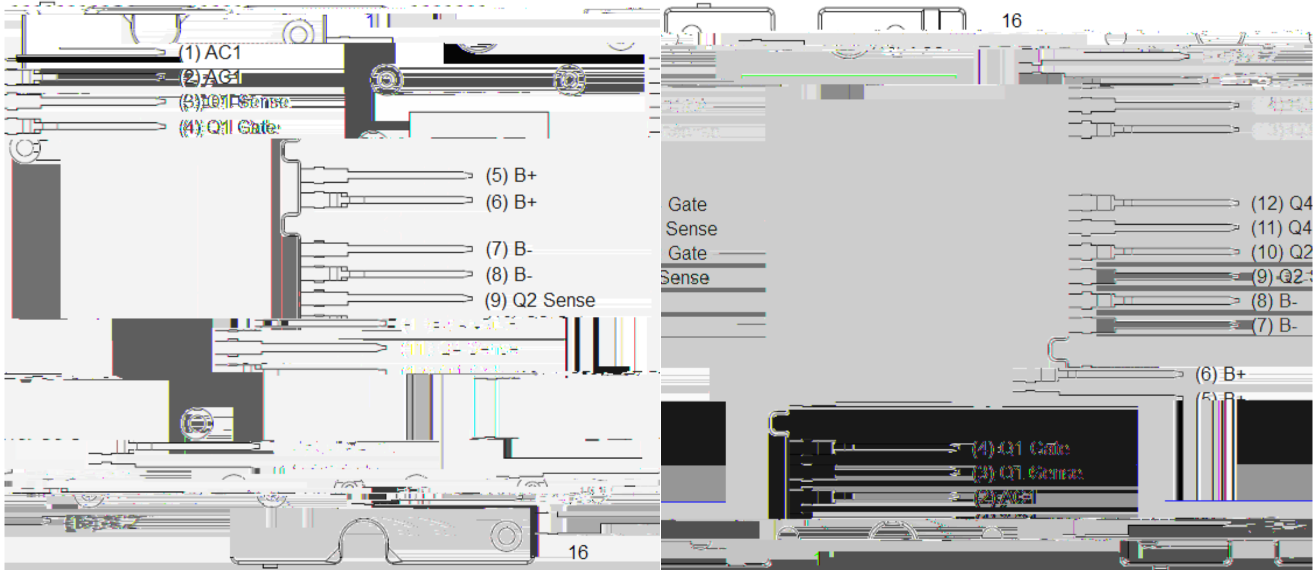



Figure 1. Pin Configuration

Table 1. PIN DESCRIPTION

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1, 2 | AC1 | Phase 1 Leg of the H−Bridge |
| 3 | Q1 Sense | Source Sense of Q1 |
| 4 | Q1 Gate | Gate Terminal of Q1 |
| 5, 6 | B+ | Positive Battery Terminal |
| 7, 8 | B− | Negative Battery Terminal |
| 9 | Q2 Sense | Source Sense of Q2 |
| 10 | Q2 Gate | Gate Terminal of Q2 |
| 11 | Q4 Sense | Source Sense of Q4 |
| 12 | Q4 Gate | Gate Terminal of Q4 |
| 13 | Q3 Sense | Source Sense of Q3 |
| 14 | Q3 Gate | Gate Terminal of Q3 |
| 15, 16 | AC2 | Phase 2 Leg of the H−Bridge |



Share Feedback
Your Opinion Matters

## INTERNAL EQUIVALENT CIRCUIT

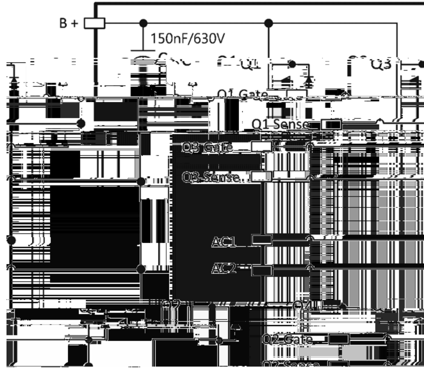



Figure 2. Internal Block Diagram

Table 2. ABSOLUTE MAXIMUM RATINGS ($T_J$ = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $V_{DS}$ (Q1~Q4) | Drain−to−Source Voltage | 650 | V |
| $V_{GS}$ (Q1~Q4) | Gate−to−Source Voltage | | |



Share Feedback
Your Opinion Matters

Solder presents high risk to melt at temperature beyond 210°C. Base of the leads, at the interface with the package body, should not be exposed to more than 200°C during mounting on the PCB or during welding to prevent the re–melting of the solder joints.

Table 4. ELECTRICAL SPECIFICATIONS ($T_J$ = 25°C, Unless Otherwise Specified)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain–to–Source Breakdown Voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 V | 650 | – | – | V |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 3.3 mA | 3.0 | – | 5.0 | V |
| $R_{DS(ON)}$ | Q1 – Q4 MOSFET On Resistance | $V_{GS}$ = 10 V, $I_D$ = 20 A | – | 44 | 51 | mΩ |
| $R_{DS(ON)}$ | Q1 – Q4 MOSFET On Resistance | $V_{GS}$ = 10 V, $I_D$ = 20 A, $T_J$ = 125°C (Note 4) | – | 79 | – | mΩ |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 20 V, $I_D$ = 20 A (Note 4) | – | 30 | – | S |
| $I_{GSS}$ | Gate–to–Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | –100 | – | +100 | nA |
| $I_{DSS}$ | Drain–to–Source Leakage Current | $V_{DS}$ = 650 V, $V_{GS}$ = 0 V | – | – | 10 | μA |
| **DYNAMIC CHARACTERISTICS (Note 4)** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 400 V<br>$V_{GS}$ = 0 V<br>f = 1 MHz | – | 4864 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 109 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 16 | – | pF |
| $C_{oss(eff)}$ | Effective Output Capacitance | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 V | – | 652 | – | pF |
| $R_g$ | Gate Resistance | f = 1 MHz | – | 2 | – | Ω |
| $Q_{g(tot)}$ | Total Gate Charge | $V_{DS}$ = 380 V<br>$I_D$ = 20 A<br>$V_{GS}$ = 0 to 10 V | – | 123 | – | nC |
| $Q_{gs}$ | Gate–to–Source Gate Charge | | – | 37.5 | – | nC |
| $Q_{gd}$ | Gate–to–Drain "Miller" Charge | | – | 49 | – | nC |
| **SWITCHING CHARACTERISTICS (Note 4)** | | | | | | |
| $t_{on}$ | Turn–on Time | $V_{DS}$ = 400 V<br>$I_D$ = 20 A<br>$V_{GS}$ = 10 V<br>$R_G$ = 4.7 Ω | – | 87 | – | ns |
| $t_{d(on)}$ | Turn–on Delay Time | | – | 47 | – | ns |
| $t_r$ | Turn–on Rise Time | | – | 43 | – | ns |
| $t_{off}$ | Turn–off Time | | – | 148 | – | ns |
| $t_{d(off)}$ | Turn–off Delay Time | | – | 118 | – | ns |
| $t_f$ | Turn–off Fall Time | | – | 29 | – | ns |
| **BODY DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source–to–Drain Diode Voltage | $I_{SD}$ = 20 A, $V_{GS}$ = 0 V | – | 0.95 | – | V |
| $T_{rr}$ | Reverse Recovery Time | $V_{DS}$ = 520 V, $I_D$ = 20 A,<br>$d_I/d_t$ = 100 A/μs (Note 4) | – | 133 | – | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 669 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Defined by design, not subject to production test

Table 5. THERMAL RESISTANCE

| Parameters | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $R_{\theta JC}$ (per chip) | Q1~Q4 Thermal Resistance Junction–to–Case (Note 5) | – | 0.19 | 0.27 | °C/W |
| $R_{\theta JS}$ (per chip) | Q1~Q4 Thermal Resistance Junction–to–Sink (Note 6) | – | 0.75 | – | °C/W |

54hw2r the listed5.teTest 4Tety331.,3287l39M3049.46399.0935e.9eft00wtfBMT34TcOre7420e207.949ucti Tcm0 M34Tc0re7l20e2meas20e0 0elow9uctipacka251.499979839

## PARAMETER DEFINITIONS

### Reference to Table 4: Parameter of Electrical Specifications

| | |
|---|---|
| $BV_{DSS}$ | Q1 – Q4 MOSFET Drain−to−Source Breakdown Voltage<br>The maximum drain−to−source voltage the MOSFET can endure without the avalanche breakdown of the body− drain P−N junction in off state.<br>The measurement conditions are to be found in Table 4.<br>The typ. Temperature behavior is described in Figure 13 |
| $V_{GS(th)}$ | Q1 – Q4 MOSFET Gate to Source Threshold Voltage<br>The gate−to−source voltage measurement is triggered by a threshold ID current given in conditions at Table 3.<br>The typ. Temperature behavior can be found in Figure 12 |

Share Feedback
Your Opinion Matters

## TYPICAL CHARACTERISTICS

| | | | | |
|---|---|---|---|---|
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |
| | | | | |

## TYPICAL CHARACTERISTICS

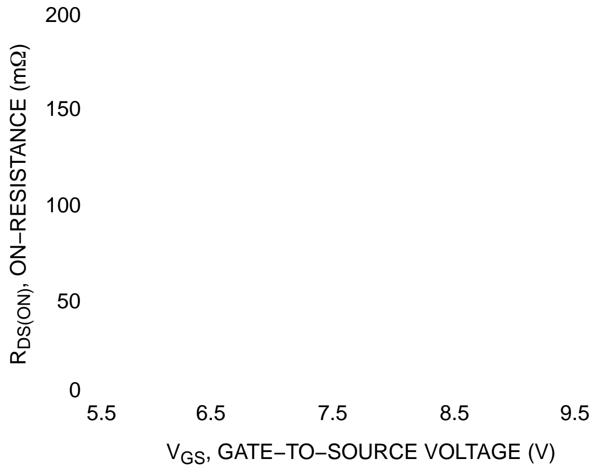



Figure 10. On−Resistance vs. Gate−to−Source Voltage

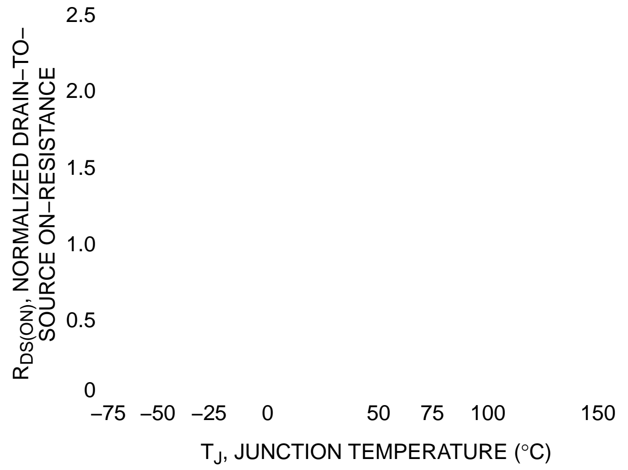



Figure 11. $R_{DS(norm)}$ vs. Junction Temperature

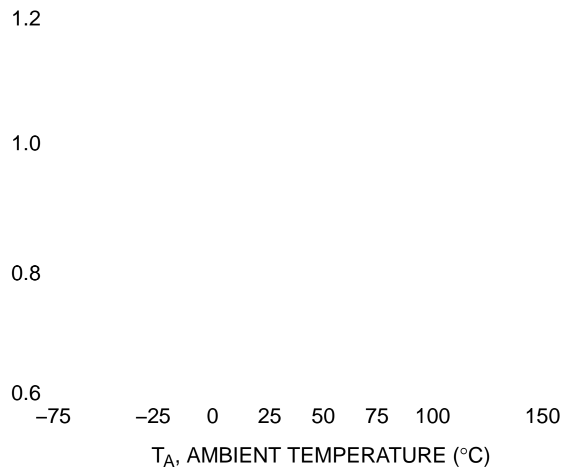



Figure 12. Normalized Gate Threshold Voltage vs. Temperature

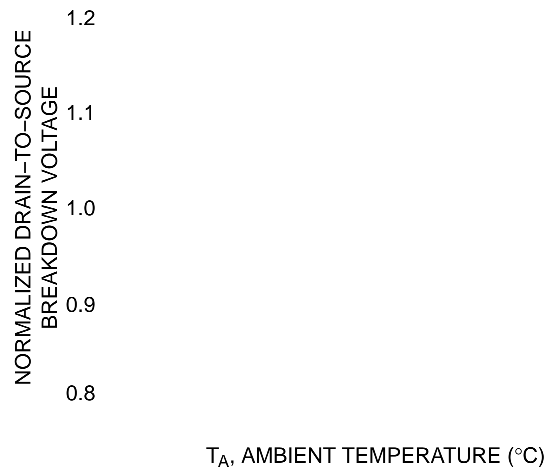



Figure 13. Normalized Breakdown Voltage vs. Temperature

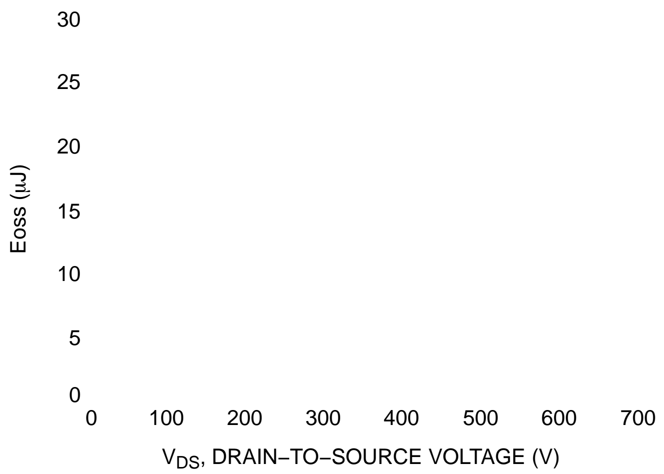



Figure 14. Eoss vs. Drain−to−Source Voltage

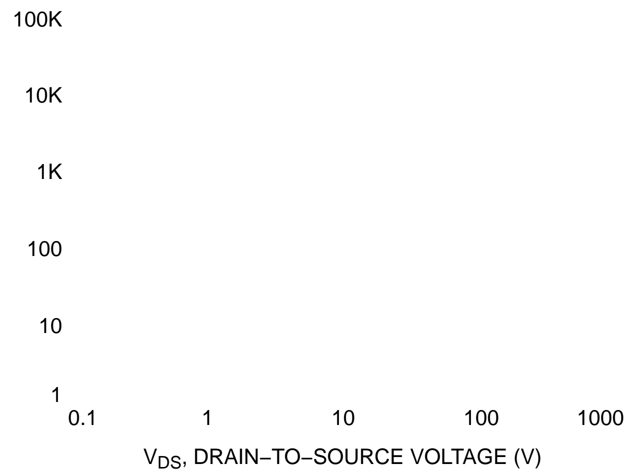
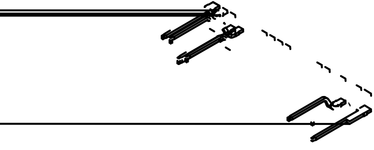


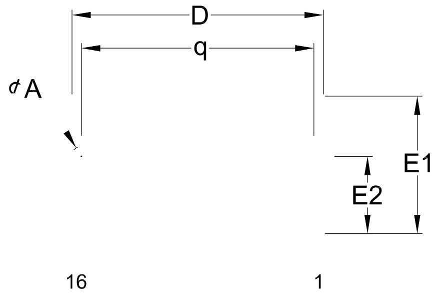

Figure 15. Capacitance Variation

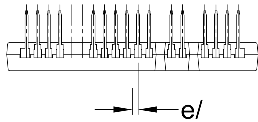
Share Feedback
Your Opinion Matters

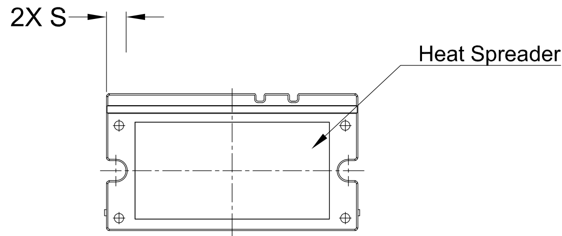


**PIM16 40.10x21.90x4.50**
CASE MODGJ
ISSUE D

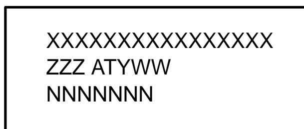
DATE 17 JAN 2024




**GENERIC MARKING DIAGRAM***




XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

*This information is generic. Please refer to device data sheet for actual part marking. Pb Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**onsemi**, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**