

# High-Efficiency Step-Down DC-DC Converter

# 1 A

# FAN2001/FAN2002

# Description

Designed for use in battery–powered applications, the FAN2001/ FAN2002 is a high–efficiency, low–noise synchronous PWM current mode and Pulse Skip (Power Save) mode dc–dc converter. It can provide up to 1 A of output current over a wide input range from 2.5 V to 5.5 V. The output voltage can be externally adjusted over a wide range of 0.8 V to 5.5 V by means of an external voltage divider.

At moderate and light loads, pulse skipping modulation is used. Dynamic voltage positioning is applied, and the output voltage is shifted 0.8% above nominal value for increased headroom during load transients. At higher loads the system automatically switches over to current mode PWM control, operating at 1.3 MHz. A current mode control loop with fast transient response ensures excellent line and load regulation. To achieve high efficiency and ensure long battery life, the quiescent current is reduced to 25  $\mu$ A in Power Save mode, and the supply current drops below 1  $\mu$ A in shut–down mode. The FAN2001/FAN2002 is available in a 3x3 mm 6–lead MLP package.

#### Features

- 96% Efficiency, Synchronous Operation
- Adjustable Output Voltage Options from 0.8 V to  $V_{IN}$
- 2.5 V to 5.5 V Input Voltage Range
- Up to 1 A Output Current
- Fixed Frequency 1.3 MHz PWM Operation
- High Efficiency Power Save Mode
- 100% Duty Cycle Low Dropout Operation
- Soft Start
- Output Over–Voltage Protection
- Dynamic Output Voltage Positioning
- 25 µA Quiescent Current
- Thermal Shutdown and Short Circuit Protection
- Pb–Free and Halide Free

# Applications

- Pocket PCs, PDAs
- Cell Phones
- Battery–Powered Portable Devices
- Digital Cameras
- Hard Disk Drives
- Set-Top-Boxes
- Point-of-Load Power
- Notebook Computers
- Communications Equipment



WDFN6 CASE 511CP

# MARKING DIAGRAM

\$Y	= <b>onsemi</b> Logo	
&Z	= Assembly Plant Code	

- &2 = 2–Digit Data Code
- &K = Lot Run Traceability Code
- 200xC = Specific Device Code
  - x = 1 or 2

# **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
FAN2001MPX	WDFN6 (Pb–Free,	3000 / Tape & Reel
FAN2002MPX	Halide Free)	

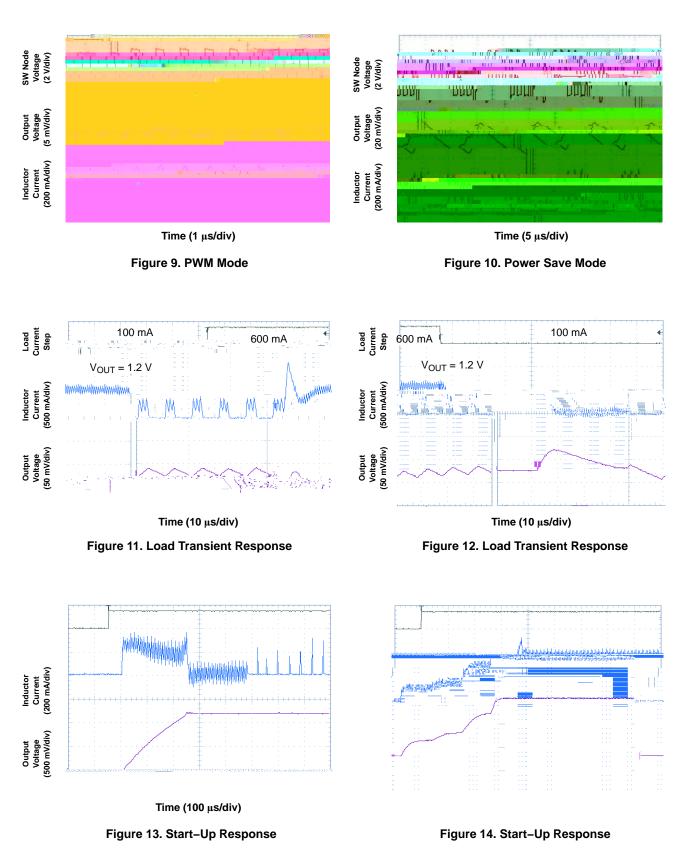
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, <u>BRD8011/D</u>.

# ELECTRICAL CHARACTERISTICS

(V\_{IN} = V\_{OUT} + 0.6 V (min. 2.5 V) to 5.5 V,  $I_{OUT}$ 

# TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

(T<sub>A</sub> = 25°C, C<sub>IN</sub> = 10  $\mu$ F, C<sub>OUT</sub> = 20  $\mu$ F, L = 3.3  $\mu$ H, R2 = 10 k $\Omega$ , unless otherwise noted.)



## **BLOCK DIAGRAM**

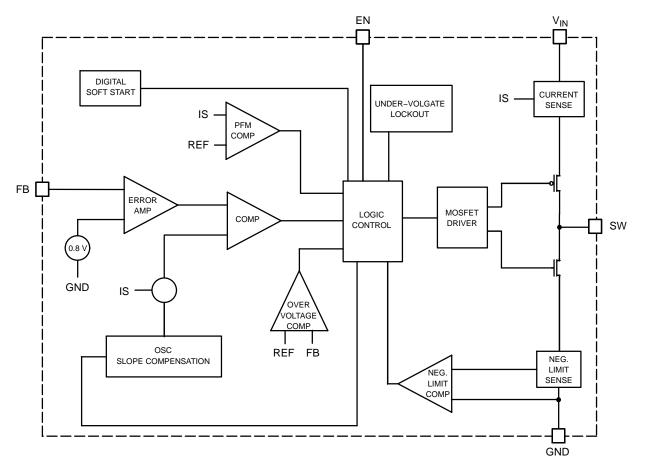


Figure 15. Block Diagram

# DETAILED OPERATION DESCRIPTION

The FAN2001/FAN2002 is a step-down converter operating in a current-mode PFM/PWM architecture with a typical switching frequency of 1.3 MHz. At moderate to heavy loads, the converter operates in pulse-width-modulation (PWM) mode. At light loads the converter enters a power-save mode (PFM pulse skipping) to keep the efficiency high.

# **PWM Mode**

In PWM mode, the device operates at a fixed frequency of 1.3 MHz. At the beginning of each clock cycle, the P–channel transistor is turned on. The inductor current ramps up and is monitored via an internal circuit. The P–channel switch is turned off when the sensed current causes the PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set internally to typically 1500 mA). After a minimum dead time the N–channel transistor is turned on and the inductor current ramps down. As the clock cycle is completed, the N–channel switch is turned off and the next clock cycle starts.

#### PFM (Power Save) Mode

As the load current decreases and the inductor current reaches negative value, the converter enters pulse–frequency–modulation (PFM) mode. The transition point for the PFM mode is given by the equation:

$$I_{OUT} = V_{OUT} \times \frac{1 - \left(\frac{V_{OUT}}{V_{IN}}\right)}{2 \times L \times f}$$
 (eq. 1)

The typical output current when the device enters PFM mode is 150 mA for input voltage of 3.6 V and output voltage of 1.2 V. In minimum. Consequently, the high efficiency is maintained at light loads. As soon as the output voltage falls below a threshold, set at 0.8% above the nominal value, the P–channel transistor is turned on and the inductor current ramps up. The P–channel switch turns off and the N–channel turns on as the peak inductor current is reached (typical 450 mA).

The N-channel transistor is turned off before the inductor current becomes negative. At this time the P-channel is switched on again starting the next pulse. The converter

continues these pulses until the high threshold (typical 1.6% above nominal value) is reached. A higher output voltage in PFM mode gives additional headroom for the voltage drop during a load transient from light to full load. The voltage overshoot during this load transient is also minimized due to active regulation during turn on of the N–channel rectifier switch. The device stays in sleep mode until the output voltage falls below the low threshold. The FAN2001/FAN2002 enters the PWM mode as soon as the output voltage can no longer be regulated in PFM with constant peak current.

#### 100% Duty Cycle Operation

As the input voltage approaches the output voltage and the duty cycle exceeds the typical 95%, the converter turns the P-channel transistor continuously on. In this mode the output voltage is equal to the input voltage minus the voltage drop across the P-channel transistor:

$$V_{OUT} = V_{IN} - I_{LOAD} \times (R_{DS(on)} + R_L)$$
 (eq. 2)

where:

 $\begin{array}{ll} R_{DS(on)} &= P-channel \ Switch \ ON \ Resistance \\ I_{LOAD} &= Output \ Current \\ R_L &= Inductor \ DC \ Resistance \end{array}$ 

#### **UVLO and Soft Start**

The reference and the circuit remain reset until the  $V_{IN}\xspace$  crosses its UVLO threshold.

The FAN2001/FAN2002 has an internal soft–start circuit that limits the in–rush current during start–up. This prevents possible voltage drops of the input voltage and eliminates the output voltage overshoot. The soft–start is implemented as a digital circuit increasing the switch current in four steps to the P–channel current limit (1500 mA). Typical start–up time for a 20  $\mu$ F output capacitor and a load current of 1000 mA is 800  $\mu$ s.

## **Short Circuit Protection**

The switch peak current is limited cycle–by–cycle to a typical value of 1500 mA. In the event of an output voltage short circuit, the device operates with a frequency of 400 kHz and minimum duty cycle, therefore the average input current is typically 200 mA.

## **Thermal Shutdown**

When the die temperature exceeds 150°C, a reset occurs and will remain in effect until the die cools to 130°C, at that time the circuit will be allowed to restart.

# APPLICATIONS INFORMATION

#### Setting the Output Voltage

The internal reference is 0.8 V (Typical). The output voltage is divided by a resistor divider, R1 and R2 to the FB pin. The output voltage is given by:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$
 (eq. 3)

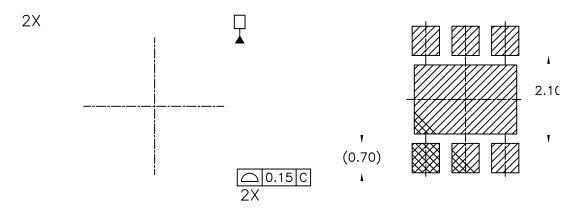
where:

 $R_1+R_2<800\;k\Omega$ 

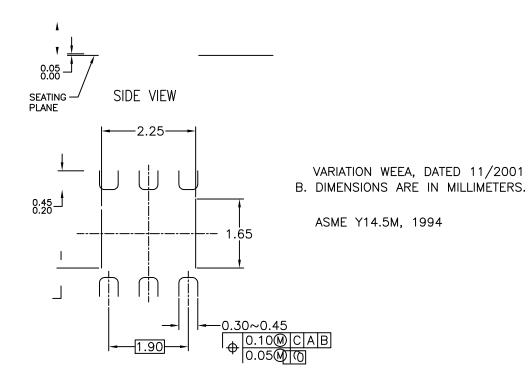
According to this equation, and assuming desired output voltage of 1.5096 V, and given  $R2 = 10 \text{ k}\Omega$ , the calculated value of R1 is 8.87 k $\Omega$ . If quiescent current is a key design parameter a higher value feedback resistor can be used (e.g.  $R2 = 100 \text{ k}\Omega$ ) and a small bypass capacitor of 10 pF is

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