To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

September 2015

FAN2106 ð 3-24 V Input, 6 A, High-Efficiency, Integrated Synchronous Buck Regulator

Features

- 6 A Output Current
- Wide Input Range: 3 V - 24 V
- Output Voltage Range: 0.8 V to 80% V_{IN}
- Over 95% Peak Efficiency
- 1% Reference Accuracy Over Temperature
- Programmable Frequency Operation: 200 KHz to 600 KHz
- Fully Synchronous Operation with Integrated Schottky Diode on Low-Side MOSFET Boosts Efficiency
- Internal Bootstrap Diode
- Internal Soft-Start
- Power-Good Signal
- Starts on Pre-Biased Outputs
- Accepts Ceramic Capacitors on Output
- External Compensation for Flexible Design
- Programmable Current Limit
- Under-Voltage, Over-Voltage, and Thermal Protections
- 5x6 mm, 25-Pin, 3-Pad MLP Package

Applications

- Servers & Telecom
- Graphics Cards & Displays
- Computing Systems
- Point-of-Load Regulation
- Set-Top Boxes & Game Consoles

Description

The FAN2106 is a highly efficient, small-footprint, constant-frequency, 6 A, integrated synchronous buck regulator.

The FAN2106 contains both synchronous MOSFETs and a controller/driver with optimized interconnects in one package, which enables designers to solve high-current requirements in a small area with minimal external components. Integration helps to minimize critical inductances, making component layout simpler and more efficient compared to discrete solutions.

The FAN2106 provides for external loop compensation, programmable switching frequency, and current limit. These features allow design flexibility and optimization. High-frequency operation allows for all-ceramic solutions.

The summing current-mode modulator uses lossless current sensing for current feedback and over-current protection. Voltage feedforward helps operation over a wide input voltage range.

, combined with low-$R_{DS(ON)}$ internal MOSFETs and a thermally efficient MLP package, provide the ability to dissipate high power in a small package.

Output over-voltage, under-voltage, over-current, and thermal shutdown protections help protect the device from damage during fault conditions. FAN2106 prevents pre-biased output discharge during startup in point-of-load applications.

Typical Application Diagram

Figure 1. Typical Application

Block Diagram

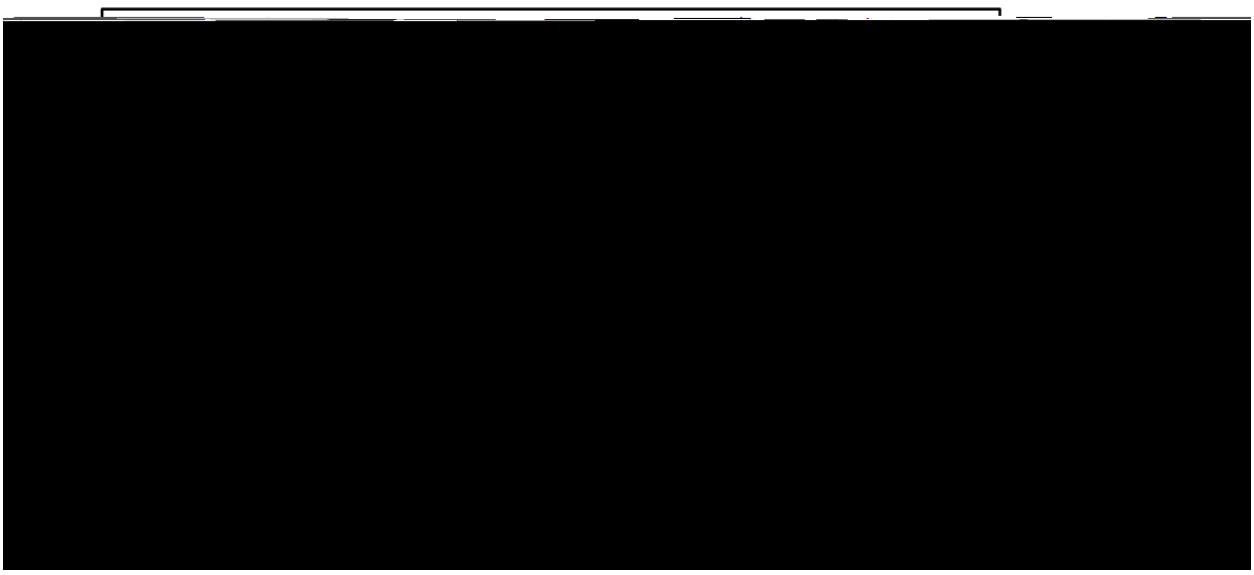

Figure 2. Block Diagram

Pin Configuration

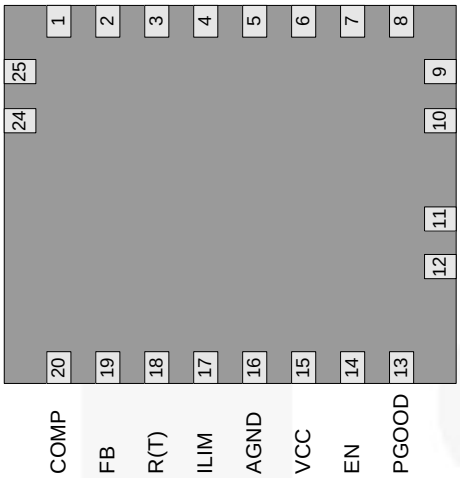

Figure 3. MLP 5 x 6 mm Pin Configuration (Bottom View)

Pin Definitions

Pin #	Name	Description
P1, 6-12	SW	**Switching Node**. Junction of high-side and low-side MOSFETs.
P2, 2-5	VIN	

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended.

Electrical Specifications

Electrical specifications are the result of using the circuit shown in Figure 1 with V_{IN} = 12 V, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Supplies					
V_{CC} Current	SW = Open, FB = 0.7 V, V_{CC} = 5 V, f_{SW} = 600 KHz		8	12	mA
	Shutdown: EN = 0, V_{CC} = 5 V		7	10	µA
V_{CC} UVLO Threshold	Rising V_{CC}	4.1	4.3	4.5	V
	Hysteresis		300		mV

Electrical Specifications (Continued)

Electrical specifications are the result of using the circuit shown in Figure 1 with V_{IN}= 12 V, unless otherwise noted.

Typical Characteristics

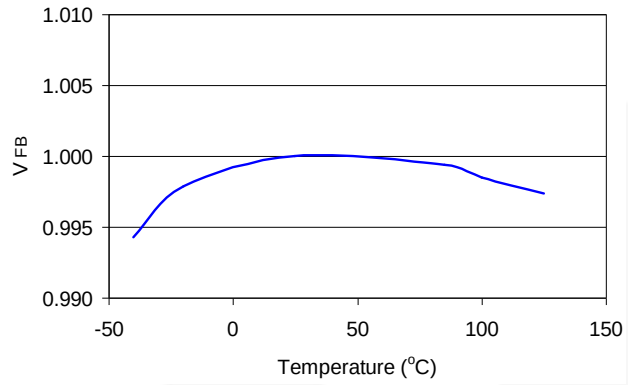

Figure 4. Reference Voltage (V_{FB}) vs. Temperature, Normalized

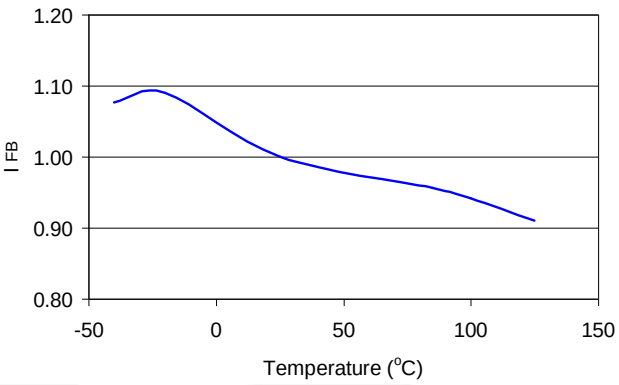

Figure 5. Reference Bias Current (I_{FB}) vs. Temperature, Normalized

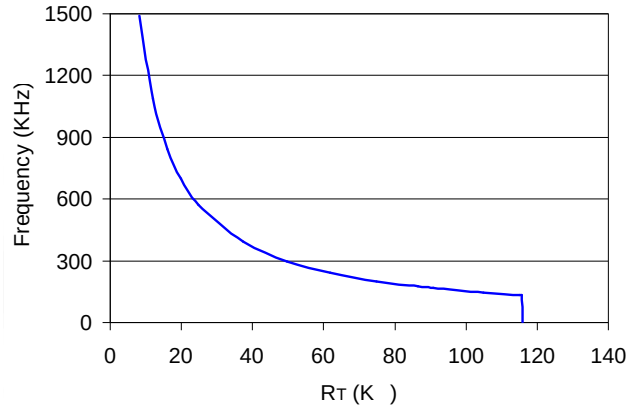

Figure 6. Frequency vs. R_T

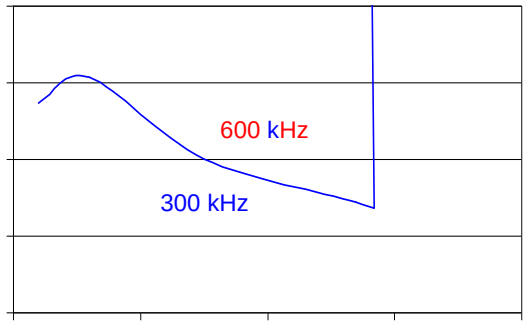

Figure 7. Frequency vs. Temperature, Normalized

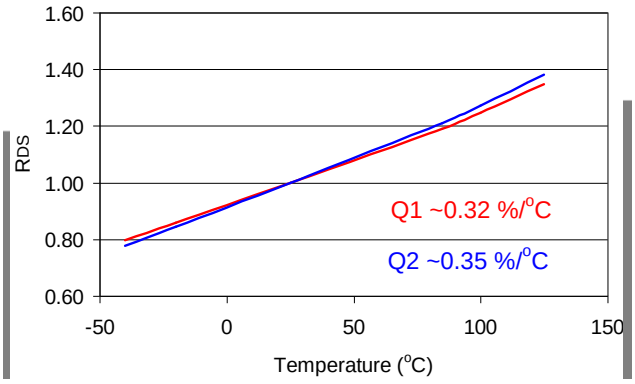

Figure 8. R_{DS} vs. Temperature, Normalized (V_{CC} = V_{GS} = 5 V)

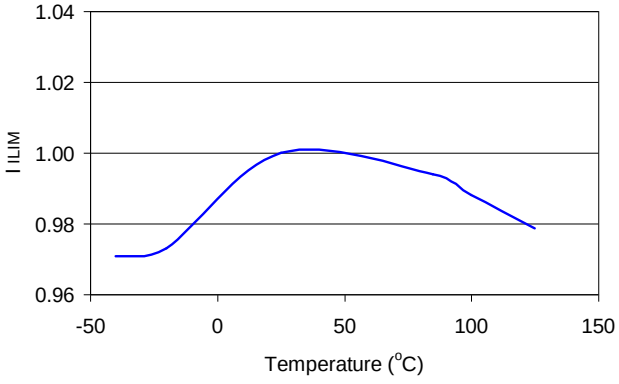

Figure 9. I_{LIM} Current (I_{ILIM}) vs. Temperature, Normalized

Application Circuit

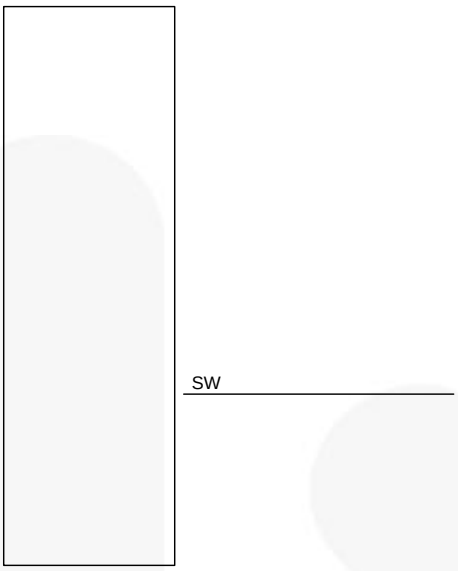

Figure 10. Application Circuit: 1.8 V

Circuit Description

PWM Generation

Refer to Figure 2 for the PWM control mechanism. FAN2106 uses the summing-mode method of control to generate the PWM pulses. An amplified current-sense signal is summed with an internally generated ramp and the combined signal is compared with the output of the error amplifier to generate the pulsewidth to drive the high-side MOSFET. Sensed current from the previous cycle is used to modulate the output of the summing block. The output of the summing block is also compared against a voltage threshold set by the R_{LIM} resistor to limit the inductor current on a cycle-by-cycle basis. The R_{RAMP} resistor helps set the charging current for the internal ramp and provides input voltage feed-forward function. The controller facilitates external compensation for enhanced flexibility.

Initialization

Once V_{CC} exceeds the UVLO threshold and EN is HIGH, the IC checks for a shorted FB pin before releasing the internal soft-start ramp (SS).

If the parallel combination of R1 and R_{BIAS} is 1 K , the internal SS ramp is not released and the regulator does not start.

Enable

FAN2106 has an internal pull-up to the ENABLE (EN) pin so that the IC is enabled once V_{CC} exceeds the UVLO threshold. Connecting a small capacitor across EN and AGND delays the rate of voltage rise on the EN pin. The EN pin also serves for the restart whenever a fault occurs *(refer to the Auto-Restart section)*. If the regulator is enabled externally, the external EN signal should go HIGH only after V_{CC} is established. For applications where such sequencing is required, FAN2106 can be enabled (after the V_{CC} comes up) with external control, as shown in Figure 21.

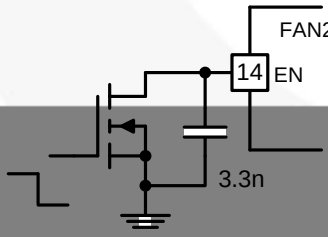

Figure 21. Enabling with External Control

Soft-Start

Once internal SS ramp has charged to 0.8 V (T0.8), the output voltage is in regulation. Until SS ramp reaches 1.0 V (T1.0), the fault latch is inhibited.

To avoid skipping the soft-start cycle, it is necessary to apply V_{IN} before V_{CC} reaches its UVLO threshold. Normal sequence for powering up would be VIN VCC EN.

Soft-start time is a function of switching frequency.

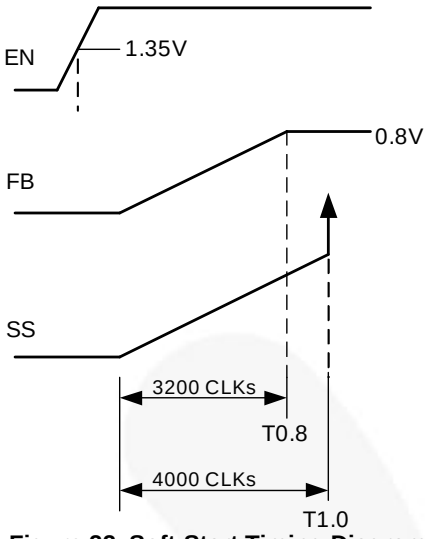

Figure 22. Soft-Start Timing Diagram

Cycling V_{CC} or the EN pin discharges the internal SS and resets the IC. In applications where external EN signal is used, V_{IN} and V_{CC} should be established before the EN signal comes up to prevent skipping the soft-start function.

Startup on Pre-Bias

BT/F3 11T1 Tf1 0 0 1 1 0CIm[(o)-3(n)-3(4a)-3(c

The regulator does not allow the low-side MOSFET to operate in full synchronous rectification mode until internal signal CC

MOSFET is fully enhanced. The fault latch is set immediately upon detection.

The OV and high-side short fault protections are active all the time, including during soft-start.

Over-Temperature Protection (OTP)

The chip incorporates an over-temperature protection circuit that sets the fault latch when a die temperature of about 150°C is reached. The IC restarts when the die temperature falls below 125°C.

Auto-Restart

After a fault, EN pin is discharged by a 1 µA current sink to a 1.1 V threshold before the internal 800 K pull-up is restored. A new soft-start cycle begins when EN charges above 1.35 V.

Depending on the external circuit, the FAN2106 can be configured to remain latched-off or to automatically restart after a fault.

Table 1. Fault / Restart Configurations

EN Pin	Controller / Restart State
Pull to GND	OFF (Disabled)
Pull-up to V_{CC} with 100 K	No Restart Latched OFF (After V_{CC} Comes Up)
Open	Immediate Restart After Fault
Cap. to GND	New Soft-Start Cycle After: t_{DELAY} (ms)=3.9 C(nf)

When EN is left open, restart is immediate.

If auto-restart is not desired, tie the EN pin to the VCC pin or pull it HIGH after V_{CC} comes up with a logic gate to keep the 1 µA cu3(tu)-5(re)-3( )3 1

Loop Compensation

The loop is compensated using a feedback network around the error amplifier. Figure 25 shows a complete Type-3 compensation network. For Type-2 compensation, eliminate R3 and C3.

Figure 25. Compensation Network

Since the FAN2106 employs a summing current-mode architecture, Type-2 compensation can be used for many applications. For applications that require wide loop bandwidth and/or use very low-ESR output capacitors, Type-3 compensation may be required.

R_{RAMP} also provides feedforward compensation for changes in V_{IN}. With a fixed R_{RAMP} value, the modulator gain increases as V_{IN} is reduced; this could make it difficult to compensate the loop. For low-input-voltage-range designs (3 V to 8 V), R_{RAMP} and the compensation component values are different compared to designs with V_{IN} between 8 V and 24 V.

Application note AN-8022 (TinyCalc) can be used to calculate the compensation components.

Recommended PCB Layout

Good PCB layout and careful attention to temperature rise is essential for reliable operation of the regulator. Four-layer PCB with two-ounce copper on the top and bottom sides and thermal vias connecting the layers are recommended. Keep power traces wide and short to minimize losses and ringing. Do not connect AGND to PGND below the IC. Connect the AGND pin to PGND at the output OR to the PGND plane.

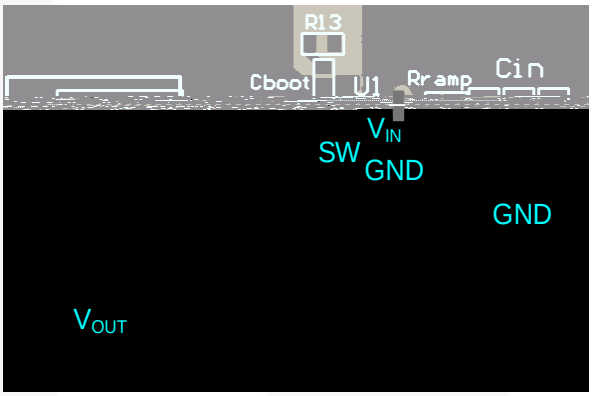

Figure 26. Recommended PCB Layout


25
21