



PFC/PWM Controller Combinational

FAN4800AS/CS/01S/2S

Description

The highly integrated FAN4800AS/CS/01S/02S parts are specially designed for power supplies that consist of boost PFC and PWM. They require very few external components to achieve versatile

operation at Light Load

- $f_{RTCT} = 4 \cdot f_{PFC} = 4 \cdot f_{PWM}$
for FAN4800AS/01S
- $f_{RTCT} = 4 \cdot f_{PFC} = 2 \cdot f_{PWM}$
for FAN4800CS/02S
- These are Pb-Free Devices

- Internet Server Power Supply
- LCD TV, Monitor Power Supply
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FAN4800AS/CS/01S/2S

Application Diagram

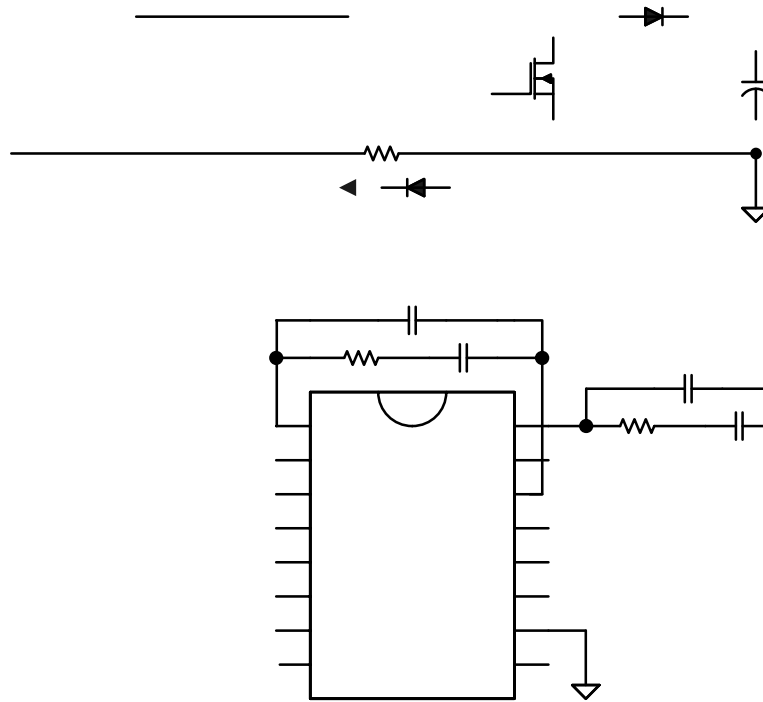


Figure 1. Typical Application, Current Mode

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Application Diagram

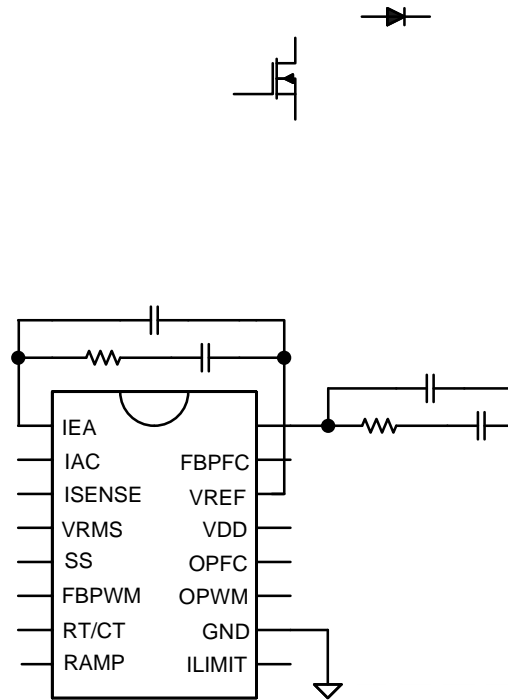


Figure 2. Typical Application, Voltage Mode

Pin Configuration

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Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V _{DD}	DC Supply Voltage	–	30	V
V _H	SS, FBPWM, RAMP, OPWM, OPFC, VREF	–0.3	30.0	V
V _L	IAC, VRMS, RT/CT, ILIMIT, FBPFC, VEA	–0.3	7.0	V
V _{IEA}	IEA	0	VREF +0.3	V
V _N	ISENSE	–5.0	0.7	V
I _{AC}	Input AC Current	–	1	mA
I _{REF}	V _{REF} Output Current	–	5	mA
I _{PFC-OUT}	Peak PFC OUT Current, Source or Sink	–	0.5	A
I _{PWM-OUT}	Peak PWM OUT Current, Source or Sink	–	0.5	A
P _D	Power Dissipation T _A < 50°C	–	800	mW
θ _{JA}	Thermal Resistance (Junction-to-Air)	DIP	80.80	°C/W
		SOP	104.10	
θ _{JC}	Thermal Resistance (Junction-to-Case)	DIP	35.38	°C/W
		SOP		

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Table 4. ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, $V_{DD} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, $T_A = T_J$, $R_T = 6.8\text{ k}\Omega$, and $C_T = 1000\text{ pF}$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD} SECTION						
V_{DD-OP}	Continuously Operating Voltage		–	–	26	V
I_{DD-ST}	Startup Current	$V_{DD} = V_{TH-ON} - 0.1\text{ V}$, OPFC OPWM Open	–	30	80	μA
I_{DD-OP}	Operating Current	$V_{DD} = 13\text{ V}$, OPFC OPWM Open	2.0	2.6	5.0	mA
V_{TH-ON}	Turn-On Threshold Voltage		10	11	12	V
ΔV_{TH}	Hysteresis		1.3	–	1.9	V
V_{DD-OVP}	V_{DD} OVP		27			

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Table 4. ELECTRICAL CHARACTERISTICS (continued)

(Unless otherwise noted, $V_{DD} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, $T_A = T_J$, $R_T = 6.8\text{ k}\Omega$, and $C_T = 1000\text{ pF}$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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VOLTAGE ERROR AMPLIFIER

V_{REF}	Reference Voltage		2.45	2.50	2.55	V
A_V	Open-Loop Gain (Note 3)		35	42	–	dB
G_{m_V}	Transconductance	$V_{NONINV} = V_{INV}$, $V_{VEA} = 3.75\text{ V}$	50	70	90	umho
$I_{FBPFC-L}$	Maximum Source Current	$V_{FBPFC} = 2\text{ V}$, $V_{VEA} = 1.5\text{ V}$	40	50	–	μA
$I_{FBPFC-H}$	Maximum Sink Current	$V_{FBPFC} = 3\text{ V}$, $V_{VEA} = 6\text{ V}$	–	–50	–40	μA
I_{BS}	Input Bias Current		–1	–	1	μA
V_{VEA-H}	Output High Voltage on V_{VEA}		5.8	6.0	–	V
V_{VEA-L}	Output Low Voltage on V_{VEA}		–	0.1	0.4	V

CURRENT ERROR AMPLIFIER

G_{m_I}	Transconductance	$V_{NONINV} = V_{INV}$, $V_{IEA} = 3.75\text{ V}$	78	88	100	umho
V_{OFFSET}	Input Offset Voltage	$V_{VEA} = 0\text{ V}$, IAC Open	–10	–	10	mV
V_{IEA-H}	Output High Voltage		6.8	7.4	8.0	V
V_{IEA-L}	Output Low Voltage		–	0.1	0.4	V
I_L	Source Current	$V_{ISENSE} = -0.6\text{ V}$, $V_{IEA} = 1.5\text{ V}$	35	50	–	μA
I_H	Sink Current	$V_{ISENSE} = +0.6\text{ V}$, $V_{IEA} = 4.0\text{ V}$	–	–50	–35	μA
A_I (Note 3)	Open-Loop Gain		40	50	–	dB

TriFault Detect™

t_{FBPFC_OPEN}	Time to FBPFC Open	$V_{FBPFC} = V_{PFC-UVLP}$ to FBPFC OPEN, 470 pF from FBPFC to GND	–	2	4	ms
$V_{PFC-UVLP}$	PFC Feedback Under-Voltage Protection		0.4	0.5	0.6	V

GAIN MODULATOR

I_{AC}	Input for AC Current (Note 3)	Multiplier Linear Range	0	–	100	μA
GAIN	GAIN Modulator (Note 4)	$I_{AC} = 17.67\text{ }\mu\text{A}$, $V_{RMS} = 1.080\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	7.500	9.000	10.500	
		$I_{AC} = 20.00\text{ }\mu\text{A}$, $V_{RMS} = 1.224\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	6.367	7.004	7.704	
		$I_{AC} = 25.69\text{ }\mu\text{A}$, $V_{RMS} = 1.585\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	3.801	4.182	4.600	
		$I_{AC} = 51.62\text{ }\mu\text{A}$, $V_{RMS} = 3.169\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	0.950	1.045	1.149	
		$I_{AC} = 62.23\text{ }\mu\text{A}$, $V_{RMS} = 3.803\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	0.660	0.726	0.798	
BW	Bandwidth (Note 3)	$I_{AC} = 40\text{ }\mu\text{A}$	–	2	–	kHz
$V_o(gm)$	Output Voltage = $5.7\text{ k}\Omega \times (I_{SENSE} - I_{OFFSET})$	$I_{AC} = 20\text{ }\mu\text{A}$, $V_{RMS} = 1.224\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	0.710	0.798	0.885	V

PFC I_{LIMIT} COMPARATOR

$V_{PFC-ILIMIT}$	Peak Current Limit Threshold Voltage, Cycle-by-Cycle Limit		–1.35	–1.20	–1.05	V
ΔV_{PK}	PFC I_{LIMIT} –Gain Modulator Output	$I_{AC} = 17.67\text{ }\mu\text{A}$, $V_{RMS} = 1.08\text{ V}$ $V_{FBPFC} = 2.25\text{ V}$	200	–	–	mV

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Table 4. ELECTRICAL CHARACTERISTICS (continued)

(Unless otherwise noted, $V_{DD} = 15\text{ V}$, $T_A = 25^\circ\text{C}$, $T_A = T_J$, $R_T = 6.8\text{ k}\Omega$, and $C_T = 1000\text{ pF}$)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
PFC OUTPUT DRIVER						
$V_{\text{GATE-CLAMP}}$	Gate Output Clamping Voltage	$V_{DD} = 22\text{ V}$	13	15	17	V
$V_{\text{GATE-L}}$	Gate Low Voltage	$V_{DD} = 15\text{ V}$, $I_O = 100\text{ mA}$	–	–	1.5	V
$V_{\text{GATE-H}}$	Gate High Voltage	$V_{DD} = 13\text{ V}$, $I_O = 100\text{ mA}$	8	–	–	V
t_R	Gate Rising Time	$V_{DD} = 15\text{ V}$, $C_L = 4.7\text{ nF}$,				

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TYPICAL CHARACTERISTICS

I_{DD-ST} (μA)

Temperature ($^{\circ}C$)

Figure 6. I_{DD-ST} vs. Temperature

V_{DD-OVP} (V)

Temperature ($^{\circ}C$)

Figure 7. V_{DD-OVP} vs. Temperature

f_{osc} (kHz)

Figure 8. f_{osc} vs. Temperature

V_{DD-OVP} (V)

Temperature ($^{\circ}C$)

Figure 9. V_{VREF} vs. Temperature

$V_{PFC-OVP}$ (V)

Temperature ($^{\circ}C$)

Figure 10. $V_{PFC-OVP}$ vs. Temperature

Figure 11. V_{REF} vs. Temperature

Figure 12. G_{mV} vs. Temperature

Temperature ($^{\circ}C$)

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TYPICAL CHARACTERISTICS (continued)

V_{SS} (μA)

-40 -25 -

Temperature ($^{\circ}C$)

Figure 22. I_{SS} vs. Temperature

I_{TC} (μA)

Temperature ($^{\circ}C$)

Figure 23. I_{TC} vs. Temperature

Functional Description

The FAN4800AS/CS/01S/02S consist of an average current controlled, continuous boost, Power Factor Correction (PFC) front end and a synchronized Pulse Width Modulator (PWM) back end. The PWM can be used in current or voltage mode. In voltage mode, feedforward from the PFC output bus can help improve the line regulation of PWM. In either mode, the PWM stage uses conventional trailing edge, duty cycle modulation. This proprietary leading / trailing edge modulation results in a higher usable PFC error amplifier bandwidth and can significantly reduce the size of the PFC DC bus capacitor.

The synchronization of the PWM with the PFC simplifies the PWM compensation due to the controlled ripple on the PFC output capacitor (the PWM input capacitor).

In addition to power factor correction, a number of protection features are built into this series. They include soft

low, too high, or open; TriFault Detect senses the error and terminates the PFC output drive.

TriFault Detect is an entirely internal circuit. It requires no external components to serve its protective function.

PFC Over-Voltage Protection

In the FAN4800AS/CS/01S/02S, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high voltage DC output of the PFC is fed to FBPF. When the voltage on FBPF exceeds 2.75 V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 250 mV of hysteresis and the PFC does not restart until the voltage at FBPF drops below 2.5 V. V_{DD} OVP can also serve as a redundant PFC OVP protection. V_{DD} OVP threshold is 28 V with 1 V hysteresis.

Selecting PFC R_{sense}

R_{sense} is the sensing resistor of the PFC boost converter. During the steady state, line input current $\times R_{sense}$ equals $I_{GAINMOD} \times 5.7 \text{ k}\Omega$.

At full load, the average V_{VEA} needs to around 4.5 V and ripple on the VEA pin needs to be less than 400 mV. Choose the resistance of the sensing resistor:

$$R_{SENSE} = \frac{(4.5 - 0.7) \times 5.7 \text{ k}\Omega \times IAC \times Gain \times V_{IN} \times \sqrt{2}}{2 \times (5.6 - 0.7) \times \text{Line_Input_Power}} \quad (\text{eq. 2})$$

where 5.6 is V

The programmable range of second level PFC output voltage is 340 V ~ 300 V.

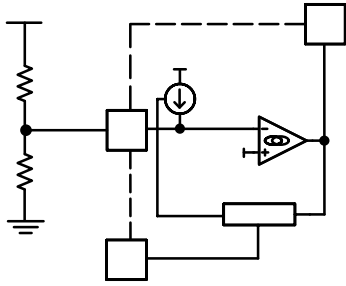


Figure 25. Two-Level PFC Scheme

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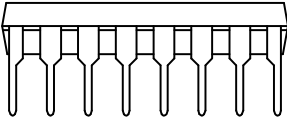
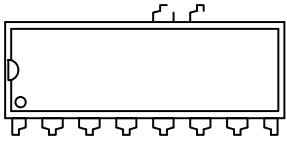
is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on time of the switch.

In the case of leading edge modulation, the switch is turned off exactly at the leading edge of the system clock.

When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty cycle of the leading edge modulation is determined during off time of the switch.

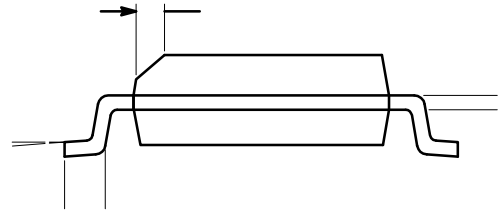
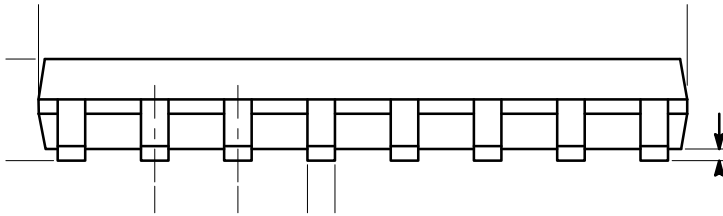
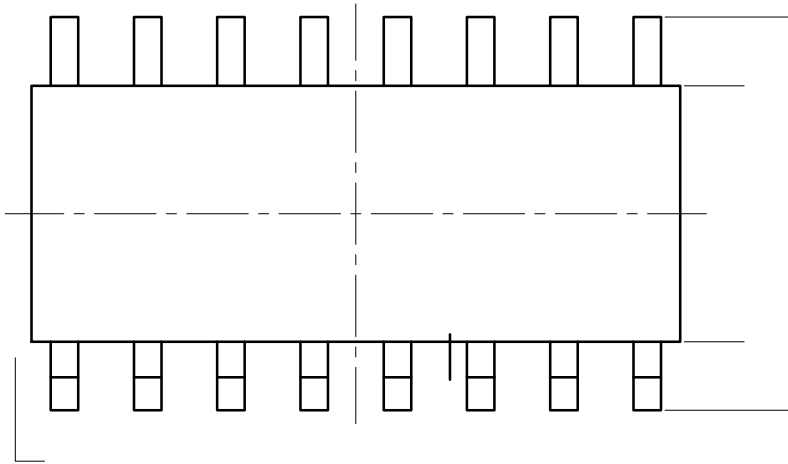
Table 5. ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Packing Method
FAN4800ASNY	-40°C to 105°C	16-Pin Dual Inline Package (DIP)	Tube
FAN4800CSNY	-40°C to 105°C	16-Pin Dual Inline Package (DIP)	Tube
FAN4800CSMY	-40°C to 105°C	16-Pin Small Outline Package (SOP)	Tape & Reel
FAN4801SNY	-40°C to 105°C	16-Pin Dual Inline Package (DIP)	Tube
FAN4801SMY	-40°C to 105°C	16-Pin Small Outline Package (SOP)	Tape & Reel
FAN4802SNY	-40°C to 105°C	16-Pin Dual Inline Package (DIP)	Tube
FAN4802SMY	-40°C to 105°C	16-Pin Small Outline Package (SOP)	Tape & Reel



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