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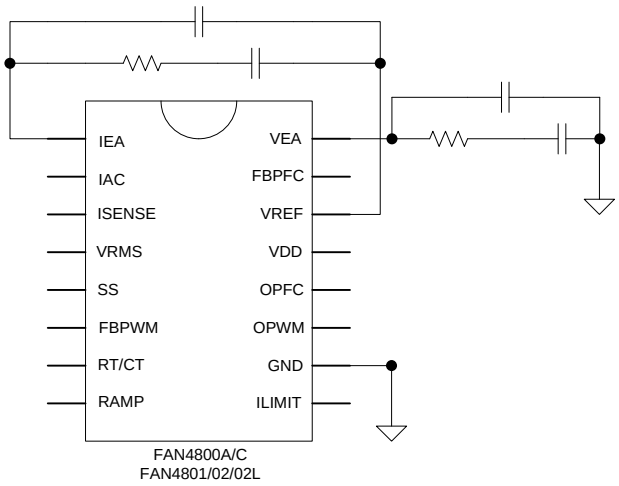
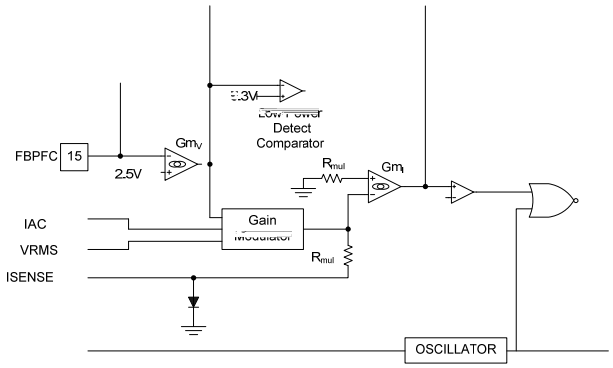
January 2011

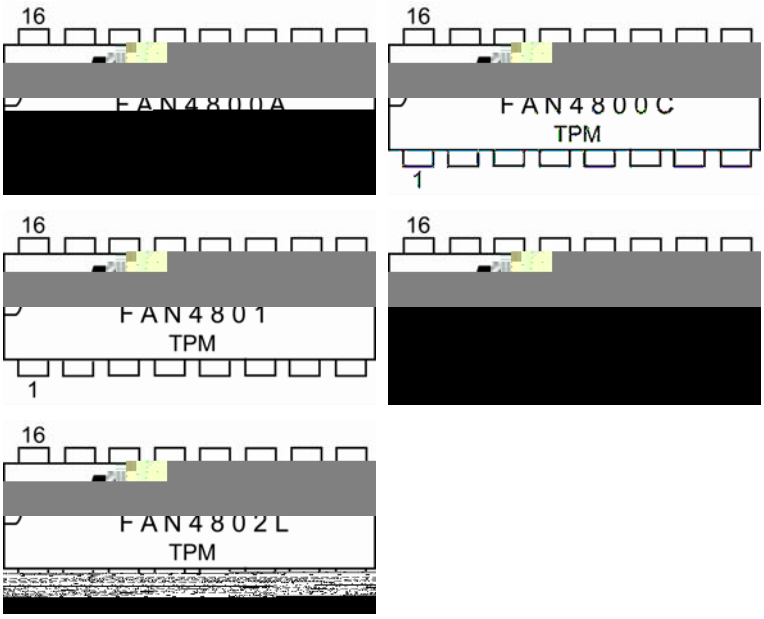
## Application Diagram



## Block Diagram

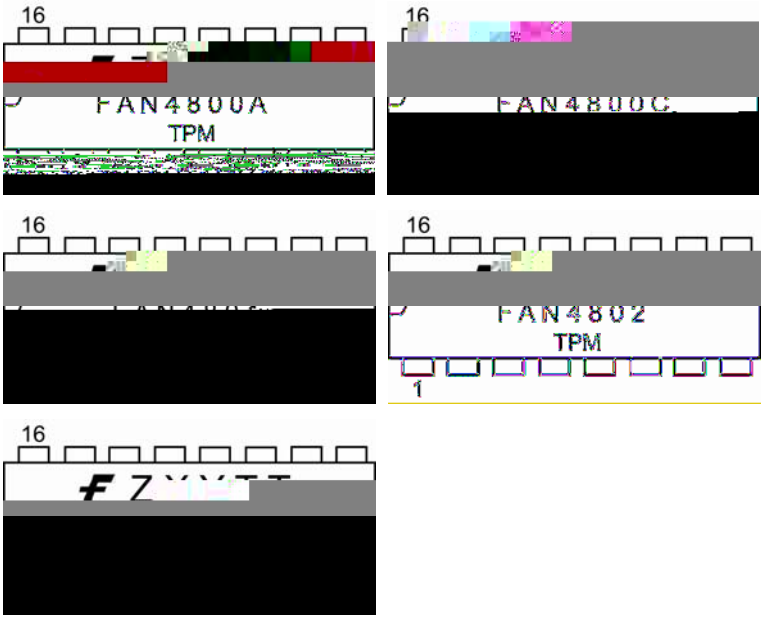


## Marking Information




*F* – Fairchild Logo
Z – Plant Code
X – 1-Digit Year Code
Y – 2-Digit Week Code
TT – 2-Digit Die-Run Code
T – Package Type (M:SOP)
P – Y: Green Package
M – Manufacture Flow Code

**Figure 5. DIP Top Mark**

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T – Package Type (M:SOP)
P – Y: Green Package
M – Manufacture Flow Code

**Figure 6. SOP Top Mark**

## Pin Configuration

**Figure 7. Pin Configuration (Top View)**

## Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1 | IEA | **Output of PFC Current Amplifier**. The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive. |
| 2 | IAC | **Input AC Current**. For normal operation, this input provides current reference for the multiplier. The suggested maximum IAC is 100µA. |
| 3 | ISENSE | **PFC Current Sense**. The non-inverting input of the PFC current amplifier and the output of multiplier and PFC ILIMIT comparator. |
| 4 | VRMS | **Line-Voltage Detection**. Line voltage detection. The pin is used for PFC multiplier. |
| 5 | SS | **PWM Soft-Start**. During startup, the SS pin charges an external capacitor with a 10µA constant current source. The voltage on FBPWM is clamped |

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | DC Supply Voltage | | 30 | V |
| $V_H$ | SS, FBPWM, RAMP, OPWM, OPFC | -0.3 | 30.0 | V |
| $V_L$ | IAC, VRMS, RT/CT, ILIMIT, FBPFC, VEA | -0.3 | 7.0 | V |
| $V_{VREF}$ | VREF | | 7.5 | V |
| $V_{IEA}$ | IEA | 0 | $V_{VREF}$+0.3 | V |
| $V_N$ | ISENSE | -5.0 | 0.7 | V |
| $I_{AC}$ | | | | |

## Electrical Characteristics

$V_{DD}$=15V, $T_A$=25°C, $R_T$=6.8kΩ, $C_T$=1000pF unless noted operating specifications.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **$V_{DD}$ Section** | | | | | | |
| $I_{DD\ ST}$ | Startup Current | $V_{DD}$=$V_{TH-ON}$-0.1V; OPFC OPWM Open | | 30 | 80 | µA |

## Electrical Characteristics (Continued)

$V_{DD}$=15V, $T_A$=25°C, $R_T$=6.8kΩ, $C_T$=1000pF unless noted operating specifications.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **Voltage Error Amplifier** | | | | | | |
| FBPFC | Input Voltage Range(3) | | 0 | | 6 | V |
| $V_{ref}$ | Reference Voltage | at T=25°C | 2.45 | 2.50 | 2.55 | V |
| $A_V$ | Open-Loop Gain(3) | | 35 | 42 | | dB |
| $Gm_v$ | Transconductance | $V_{NONINV}$=$V_{INV}$, $V_{VEA}$=3.75V at T=25°C | 50 | 70 | 90 | µmho |
| $I_{FBPFC-L}$ | Maximum Source Current | $V_{FBPFC}$=2V, $V_{VEA}$=1.5V | 40 | 50 | | µA |
| $I_{FBPFC-H}$ | Maximum Sink Current | $V_{FBPFC}$=3V, $V_{VEA}$=6V | | -50 | -40 | µA |
| $I_{BS}$ | Input Bias Current | | -1 | | 1 | µA |
| $V_{VEA-H}$ | Output High Voltage on $V_{VEA}$ | | 5.8 | 6 | | V |
| $V_{VEA-L}$ | Output Low Voltage on $V_{VEA}$ | | | 0.1 | 0.4 | V |
| **Current Error Amplifier** | | | | | | |
| $V_{ISENSE}$ | Input Voltage Range (ISENSE Pin)(3) | | -1.5 | | 0.7 | V |
| $Gm_I$ | Transconductance | $V_{NONINV}$=$V_{INV}$, $V_{IEA}$=3.75V | 78 | 88 | 100 | µmho |
| $V_{OFFSET}$ | Input Offset Voltage | $V_{VEA}$=0V, IAC Open | -10 | | 10 | mV |
| $V_{IEA-H}$ | Output High Voltage | | 6.8 | 7.4 | 8.0 | V |
| $V_{IEA-L}$ | Output Low Voltage | | | 0.1 | 0.4 | V |
| $I_L$ | Source Current | $V_{ISENSE}$=-0.6V, $V_{IEA}$=1.5V | 35 | 50 | | µA |
| $I_H$ | Sink Current | $V_{ISENSE}$=+0.6V, $V_{IEA}$=4.0V | | -50 | -35 | µA |
| $A_I$ | Open-Loop Gain(3) | | 40 | 50 | | dB |
| **Tri-Fault Detect** | | | | | | |
| $t_{FBPFC\_OPEN}$ | Time to FBPFC Open(3) | $V_{FBPFC}$=$V_{PFC-UVP}$ to FBPFC OPEN, 470pF from FBPFC to GND | | 2 | 4 | ms |
| $V_{PFC-UVP}$ | PFC Feedback Under-Voltage Protection | | 0.4 | 0.5 | 0.6 | V |
| **Gain Modulator** | | | | | | |
| $I_{AC}$ | Input for AC Current(3) | Multiplier Linear Range | 0 | | 100 | µA |
| GAIN | GAIN Modulator(4) | $I_{AC}$=17.67µA, $V_{RMS}$=1.080V $V_{FBPFC}$=2.25V, at T=25°C | 7.50 | 9.00 | 10.50 | |
| | | $I_{AC}$=20µA, $V_{RMS}$=1.224V $V_{FBPFC}$=2.25V, at T=25°C | 6.30 | 7.00 | 7.70 | |
| | | $I_{AC}$=25.69µA, $V_{RMS}$=1.585V $V_{FBPFC}$=2.25V, at T=25°C | 3.80 | 4.20 | 4.60 | |
| | | $I_{AC}$=51.62µA, $V_{RMS}$=3.169V $V_{FBPFC}$=2.25V, at T=25°C | 0.95 | 1.05 | 1.16 | |
| | | $I_{AC}$=62.23µA, $V_{RMS}$=3.803V $V_{FBPFC}$=2.25V, at T=25°C | 0.66 | 0.73 | 0.80 | |
| BW | Bandwidth(3) | $I_{AC}$=40µA | | 2 | | kHz |
| $V_{o(gm)}$ | Output Voltage=5.7kΩ × ($I_{SENSE}$-$I_{OFFSET}$)(3) | $I_{AC}$=20µA, $V_{RMS}$=1.224V $V_{FBPFC}$=2.25V, at T=25°C | 0.74 | 0.82 | 0.90 | V |

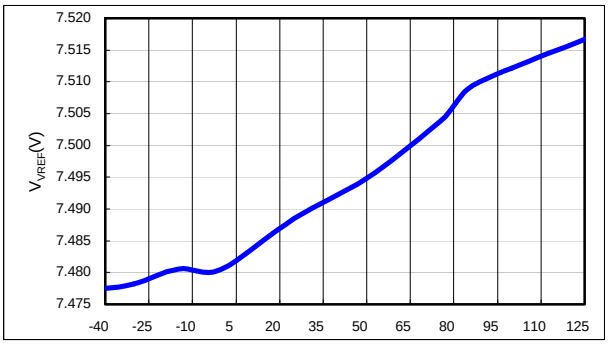
## Electrical Characteristics (Continued)

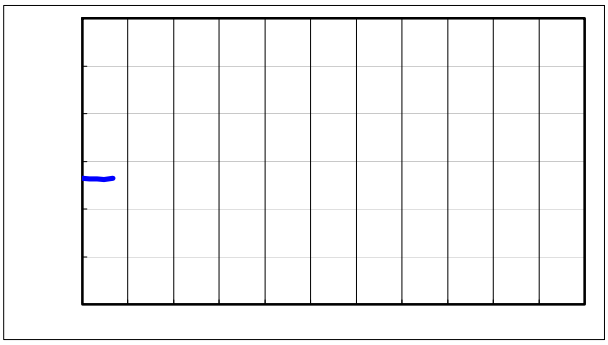
$V_{DD}$=15V, $T_A$=25°C, $R_T$=6.8kΩ, $C_T$=1000pF unless noted operating specifications.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **PWM Output Driver** | | | | | | |
| $V_{GATE-CLAMP}$ | Gate Output Clamping Voltage | $V_{DD}$=22V | 13 | 15 | 17 | V |
| $V_{GATE-L}$ | Gate Low Voltage | $V_{DD}$=15V; $I_O$=100mA | | | 1.5 | V |
| $V_{GATE-H}$ | Gate High Voltage | $V_{DD}$=13V; $I_O$=100mA | 8 | | | V |
| $t_r$ | Gate Rising Time | $V_{DD}$=15V; $C_L$=4.7nF | 30 | 60 | 120 | ns |
| $t_f$ | Gate Falling Time | $V_{DD}$=15V; $C_L$=4.7nF | 30 | 50 | 110 | ns |
| $D_{PWM-MAX}$ | Maximum Duty Cycle | | 49.0 | 49.5 | 50.0 | % |
| $V_{PWM-LS}$ | PWM Comparator Level Shift | | 1.3 | 1.5 | 1.8 | V |

## Typical Characteristics

## Typical Characteristics



## Typical Characteristics

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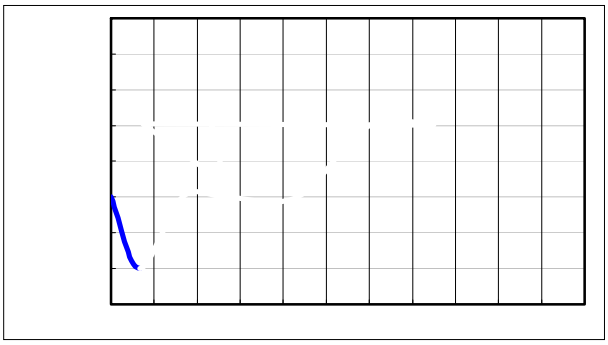
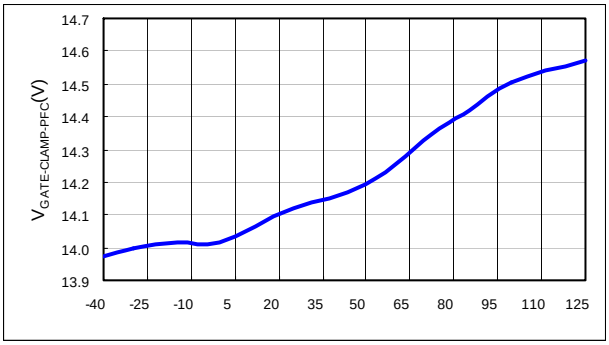
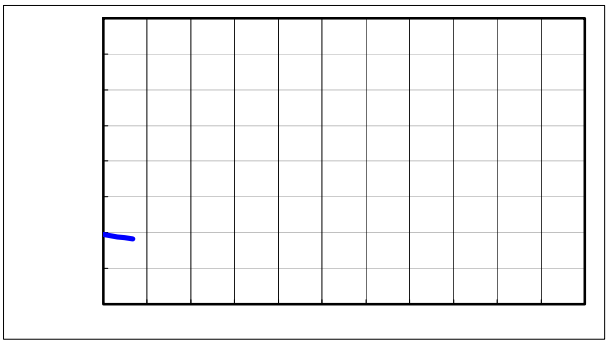


## Typical Characteristics



## Functional Description

The FAN4800A/C and FAN4801/02/02L consist of an average current controlled, continuous boost Power Factor Correction (PFC) front-end and a synchronized Pulse Width Modulator (PWM) back-end. The PWM can be used in current or voltage mode. In voltage mode, feed forward from the PFC output bus can be used to improve the line regulation of PWM. In either mode, the PWM stage uses conventional trailing-edge, duty-cycle modulation. This propriety leading/trailing edge modulation results in a higher usable PFC error

## TriFault Detect™

To improve power supply reliability, reduce system component count, and simplify compliance to UL 1950 safety standards, the FAN4800A/C, FAN4801/02/02L includes TriFault Detect. This feature monitors FBPFC for certain PFC fault conditions.

In a feedback path failure, the output of the PFC could exceed safe operating limits. With such a failure, FBPFC exceeds its normal operating area. Should FBPFC go too LOW, too HIGH, or OPEN, TriFault Detect senses the error and terminates the PFC output drive.

TriFault detect is an entirely internal circuit. It requires no external components to serve its protective function.

## PFC Over-Voltage Protection

In the FAN4800A/C, FAN4801/02/02L, the PFC OVP comparator serves to protect the power circuit from being subjected to excessive voltages if the load changes suddenly. A resistor divider from the high-voltage DC output of the PFC is fed to FBPFC. When the voltage on FBPFC exceeds 2.75V, the PFC output driver is shut down. The PWM section continues to operate. The OVP comparator has 250mV of hysteresis and the PFC does not restart until the voltage at FBPFC drops below 2.50V. $V_{DD}$ OVP can also serve as a redundant PFC OVP protection. $V_{DD}$ OVP threshold is 28V with 1V hysteresis.

## Selecting PFC $R_{SENSE}$

$R_{SENSE}$ is the sensing resistor of the PFC boost converter. During the steady state, line input current x $R_{SENSE}$ equals $I_{GAINMOD}$ x 5.7KΩ.

At full load, the average $V_{EA}$ needs to around 4.5V and ripple on the VEA needs to be less than 400mV. Choose the resistance of the sensing resistor:

$$R_{sense} \quad \frac{4.5 \quad 0.7 \quad 5.7K \quad IAC \quad Gain \quad V_{IN} \quad \sqrt{2}}{2 \quad 5.6 \quad 0.7 \quad Line\ input\ Power} \qquad (2)$$

where 5.6 is $V_{EA}$ maximum output.

## PFC Soft-Start

PFC startup is controlled by $V_{EA}$ level. Before FBPFC voltage reaches 2.4V, the $V_{EA}$ level is around 2.8V. At $90V_{AC}$, the PFC soft-start time is 90ms.

## PFC Brownout

The AC UVP comparator monitors the AC input voltage. The FAN4800A/C, FAN4801/02 disables PFC as lower AC input such that the VRMS is less than 1.05V. The brownout voltage of FAN4802L is lower than FAN4801/1S/2, such that the VRMS is less than 0.9V.

## Error Amplifier Compensation

The PWM loading of the PFC can be modeled as a negative resistor because an increase in the input voltage to the PWM causes a decrease in the input current. This response dictates the proper compensation of the two transconductance error amplifiers. Figure 46 shows the types of compensation networks most commonly used for the voltage and current error amplifiers, along with10.98 0 01.1(r t)-4.1nu 0 .2n.0

## Two-Level PFC Function

To improve the efficiency, the system can reduce PFC switching loss at low line and light load by reducing the PFC output voltage. The two-level PFC output of FAN4801/02/02L can be programmable.

As Figure 47 shows, FAN4801/02/02L detect VEA pin and VRMS pin to determine the system operates low line and light load or not. At the second-level PFC, there is a current of 20μA through $R_{F2}$ from FBPFC pin. So the second-level PFC output voltage can be calculated as.

1 2

## PWM Control (RAMP)

When the PWM section is used in current mode, RAMP is generally used as the sampling point for a voltage, representing the current in the primary of the PWM's output transformer. The voltage is derived either from a current sensing resistor or a current transformer. In voltage mode, RAMP is the input for a ramp voltage generated by a second set of timing components ($R_{RAMP}$, $C_{RAMP}$) that have a minimum value of 0V and a peak value of approximately 6V. In voltage mode, feed forward from the PFC output bus is an excellent way to derive the timing ramp for the PWM stage.

## Generating $V_{DD}$

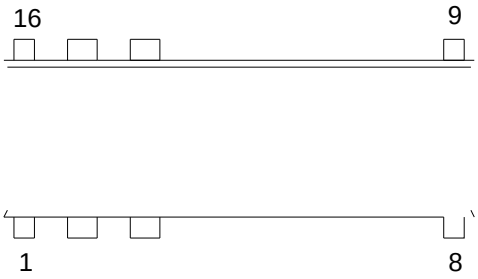
After turning on the FAN4800A/C, FAN4801/02/02L at 11V, the operating voltage can vary from 9.3V to 28V. The threshold voltage of the $V_{DD}$ OVP comparator is 28V and its hysteresis is 1V. When $V_{DD}$ reaches 28V, OPFC is LOW, and the PWM section is not disturbed. There are two ways to generate $V_{DD}$: use auxiliary power supply around 15V or use bootstrap winding to self-bias the FAN4800A/C, FAN4801/02/02L system. The bootstrap winding can be taped from the PFC boost choke or the transformer of the DC-to-DC stage.

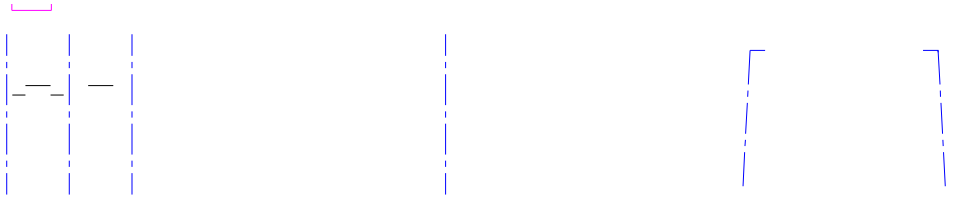
## Leading/Trailing Modulation

Conventional PWM techniques employ trailing-edge modulation, in which the switch turns on right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp up. The effective duty cycle of the trailing edge modulation is determined during the on-time of the switch.

In the case of leading-edge modulation, the switch is turned off exactly at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch is turned on. The effective duty-cycle of the leading-edge modulation is determined during off-time of the switch.

## Physical Dimensions



## Physical Dimensions (Continued)

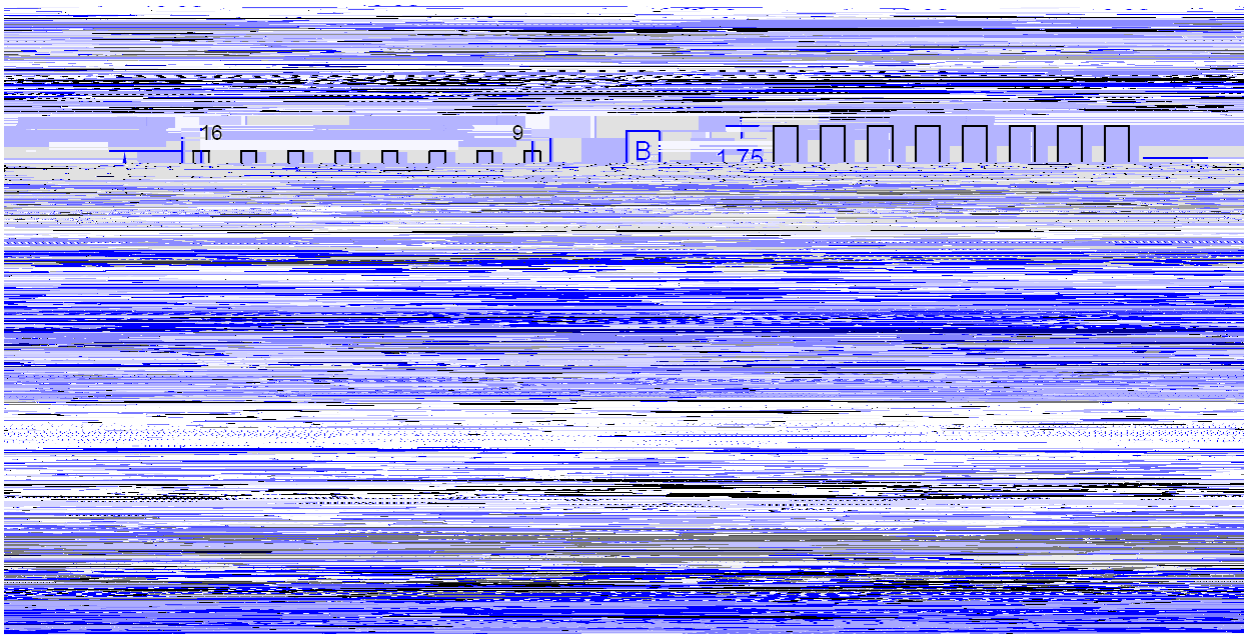



**Figure 49. 16-Pin Small Outline Package (SOIC)**

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