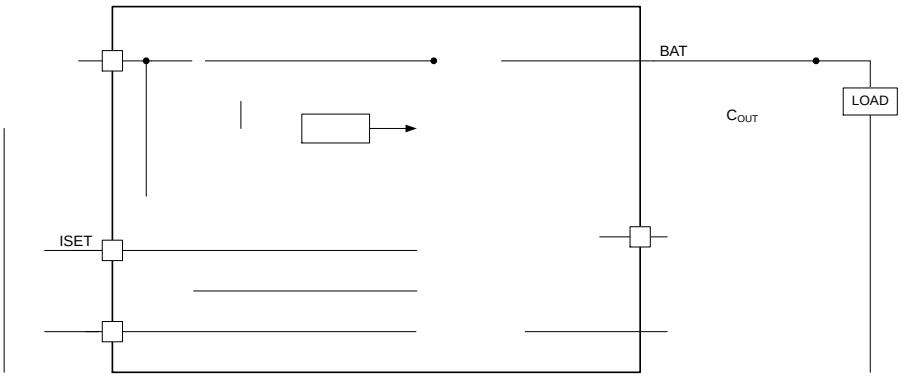
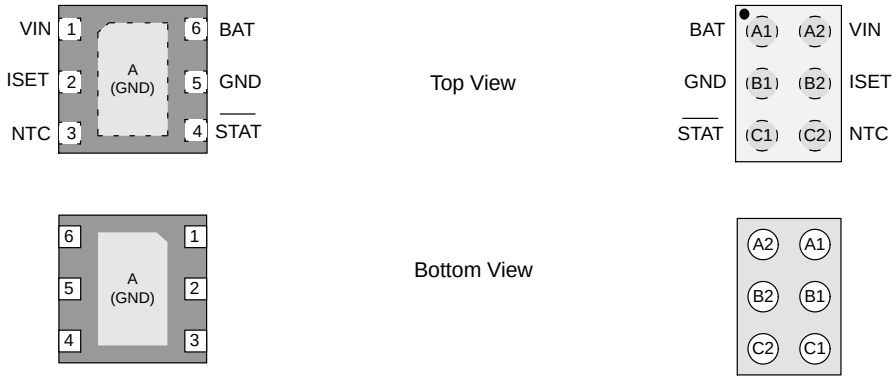
se

				†
FAN54120MP420X	4.20	20	DFN6, 2x2 mm (Pb Free)	3000 / Tape & Reel
FAN54120MP425X	4.25	25		
FAN54120MP435X	4.35	35		
FAN54120UC420X	4.20	V4	WLCSP−6, 1.36x0.76 mm (Pb Free)	3000 / Tape & Reel
FAN54120UC425X	4.25	V5		
FAN54120UC435X	4.35	V6		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





1	A2	VIN	Input Voltage. Connect C_{IN} bypass directly to VIN and GND pins on top layer.
2	B2	ISET	Set Charge Current. Connect R_{SET} directly to GND to set the maximum input/charging current (I_{FAST}).
3	C2	NTC	NTC input. Connect to battery pack NTC to provide JEITA “safe−charging” functionality. See “NTC Pin” applications section for additional usage information.
4	C1	$\overline{\text{STAT}}$	Status. Open−drain output used to indicate charge and/or fault status. Internally, there is a weak pull−up ($R_{\overline{STAT}}$) to BAT. This pin is also used to enable Power Back operation.
5, A	B1	GND	Ground. Connect to system GND plane. C_{IN} and C_{OUT} also connect directly to this pin on top layer.
6	A1	BAT	Output. Connect to system load and positive terminal of battery. Bypass with C_{OUT}, connected directly to BAT and GND pins on top layer.

V_{IN}	Voltage on VIN Pin	−1.2	28.0	V
V_{IN_SLEW}	VIN Rise Time, V_{IN} > 6 V		10	V/μsec
V_{BAT}	Voltage on BAT Pin	−0.3	6.3	V
V_X	Voltage on All Other Pins	−0.3	(Note 3)	V
ESD	Electrostatic Discharge Protection Level, HBM per JESD22−A114		1500	V
	Electrostatic Discharge Protection Level, CDM per JESD22−C101		2000	V
LU	Latch Up per JESD78, Class I, 25 C		100	mA
T_J	Junction Temperature	−40	+150	C
T_{STG}	Storage Temperature	−65	+150	C
T_{LS}	Lead Soldering Temperature, 10 Seconds		+260	C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these

V_{IN}	Voltage on VIN Pin	4	6	V
V_{BAT}	Battery Voltage	2.5	4.5	V
T_A	Ambient Temperature	−30	+85	C
T_J	Junction Temperature	−30	+120	C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

NOTE: The Recommended Operating Conditions table defines the conditions for actual device operation using the circuit of Figure 1, with the Recommended External Components shown in Table 2. Recommended operating conditions are specified to ensure

(Unless otherwise specified, circuit of Figure 1 with V_{IN} = 5.0 V, V_{FLOAT} = 4.2 V, V_{BAT} = 3.9 V, R_{SET} = 1.0 kΩ, over recommended T_A operating temperature range. Typical values are at 25 C.) (continued)

V_{BATMIN}	Pre−to−Fast Charge Threshold	Rising V_{BAT}	2.9	3.1	3.3	V
V_{RCH}	Battery Recharge Indicator Threshold	V_{BAT} Falling Below V_{FLOAT}				

(Unless otherwise specified, circuit of Figure 1 with V_{IN} = 5.0 V, V_{FLOAT} = 4.2 V, V_{BAT} = 3.9 V, R_{SET} = 1.0 kΩ, over recommended T_A operating temperature range. Typical values are at 25 C.) (continued)

I_{TREG}	Adaptive Thermal Regulation Foldback (Note 7)		40		80	% I_{FAST}
T_{SDOWN}	Thermal Shutdown Threshold (Note 7) (Note 8)	T_J Rising	130	145	160	C
	Hysteresis(Note 7)	T_J Falling		T_{REG}		C
t_{TSD_QUAL}	Thermal Shutdown Qualification Time (Note 7)	T_J Rising		1		msec
t_{DIE_T}	Die Temperature Sampling Rate (Note 7)			32		msec

t_{PRE_SC}	Pre−Charge Fault Timer (Note 7)			32		msec
t_{OSC}	Internal Oscillator Accuracy	Applies to All Timers/Counters	−15		+15	%
t_{IN_REVAL}	Input Re−Validation Attempt Period (Note					

Unless otherwise specified, circuit of Figure 1 with V_{IN} = 5.0 V, V_{FLOAT} = 4.2 V, V_{BAT} = 3.8 V, R_{SET} = 1.0 kΩ, T_A = 25 C.

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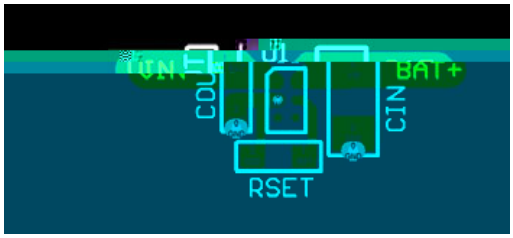
R_{SET}, connected to the ISET pin, is used to establish the maximum charging current (I_{FAST}

During the pre‐conditioning stage (Pre‐Charge), a constant current I_{PRE} (I_{FAST}

Place C_{IN} and C_{OUT} as close possible to the IC. Connect the capacitors directly to the appropriate IC pins on the top layer. Reference the circuit to the system GND plane, typically on an inner layer, using a via in the IC DAP and/or at the GND side of C_{OUT}.

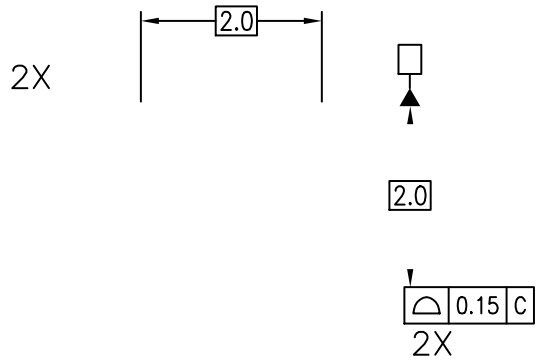
The GND side of R_{SET} should be routed with a trace directly to IC GND, rather than using a via to the GND plane. This prevents transient currents in GND plane from influencing the IC's current regulation.

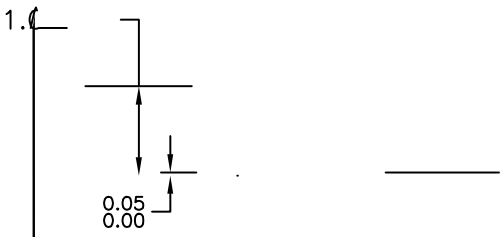
The same practices should be applied to the WLCSP version. Due to the lack of a DAP on the CSP, the GND side of C_{IN} should be connected by via to the system GND plane.



DFN6 2x2, 0.65P
CASE 506DQ
ISSUE O

DATE 31 AUG 2016





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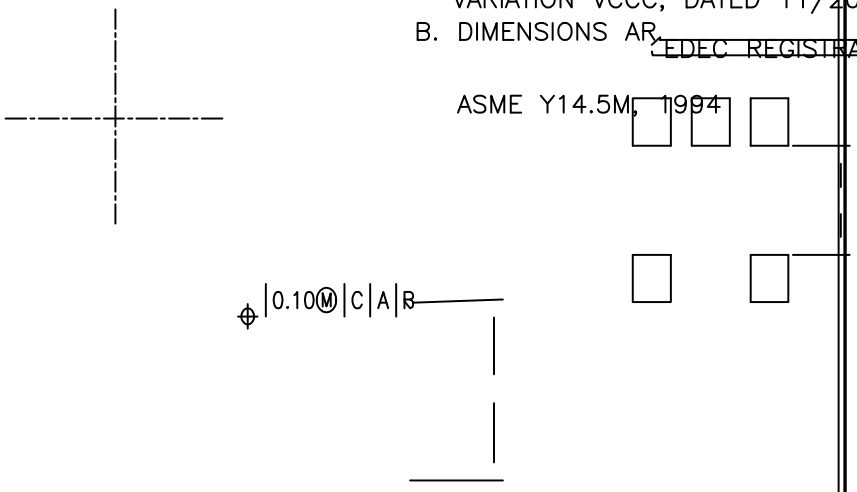
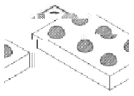


0.10 C



WLCSP6 1.36x0.76x0.581
CASE 567XQ
ISSUE O

DATE 03 APR 2019

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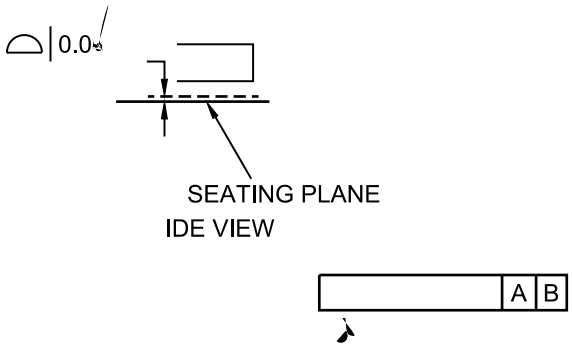

IDE VIEW

RECOMMENDED MOUNTING FOOTPRINT*
(NSMD PAD TYPE

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