Is Now Part of

To learn more about ON Semiconductor, please visit our website at www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

July 2016

Application Diagram

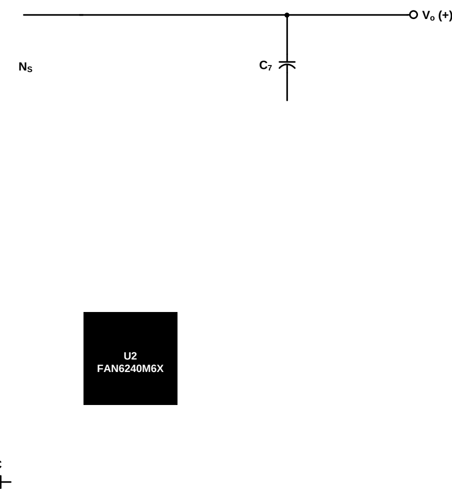

Figure 1. Typical Application

Internal Block Diagram

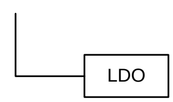

Figure 2. Function Block Diagram

Marking Information

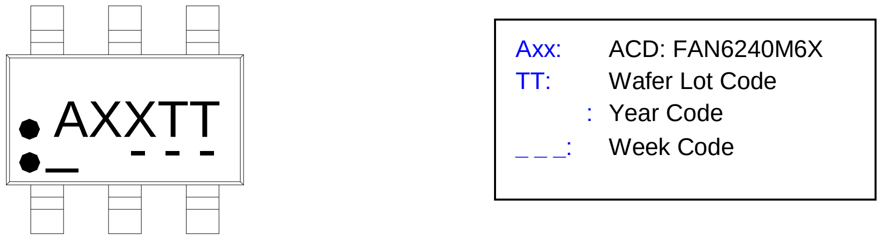

Figure 3. Top Mark

Pin Configuration

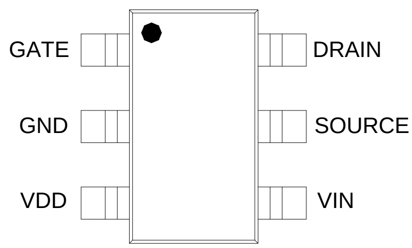

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	GATE	Gate drive output
2	GND	Ground
3	VDD	Internal regulator 5 V output and gate drive power supply rail. Bypass with 1uF capacitor to GND.
4	VIN	LDO input, supports up to 30 V operation. An integrated 5 V LDO generates the internal VDD power supply rail for the low-voltage control circuitry.
5	SOURCE	Synchronous rectifier source sense input.
6	DRAIN	Synchronous rectifier drain sense input.

Absolute Maximum Ratings

Electrical Characteristics

V_{IN} = 12 V and T_J = -40°C to 125°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage						
V_{IN_ON}	Turn-On Threshold	V_{IN} Rising	3.1	3.4	3.7	V
V_{IN_OFF}	Turn-Off Threshold	V_{IN} Falling	2.8	2.9	3.0	V
I_{IN_OP}	Operating Current	f_{SW} = 100 kHz, C_{GATE} = 3.3 nF, V_{IN} = 5 V		2	3.5	mA

Power Supply Section

Functional Description

Theory of SR Control Operation

For an ideal circuit operation, the SR control algorithm of FAN6240 is very straightforward. FAN6240 controls the SR MOSFET based on the instantaneous drain-to-source voltage as illustrated in Figure 5. When the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold (V_{TH_ON}

SR Turn-Off Algorithm

As diagram shown in Figure 7, the turn-off of SR GATE is triggered by the two input signals of AND gate. The first input signal is turn off signal, which is enabled when $V_{DS.SR}>V_{TH\_OFF}$. The second input is TURN_OFF_ALLOW signal given from the adaptive turn-off blanking. The blanking time is adaptively determined as half of SR conduction time (SR_COND) of the previous switching cycle for better noise immunity.

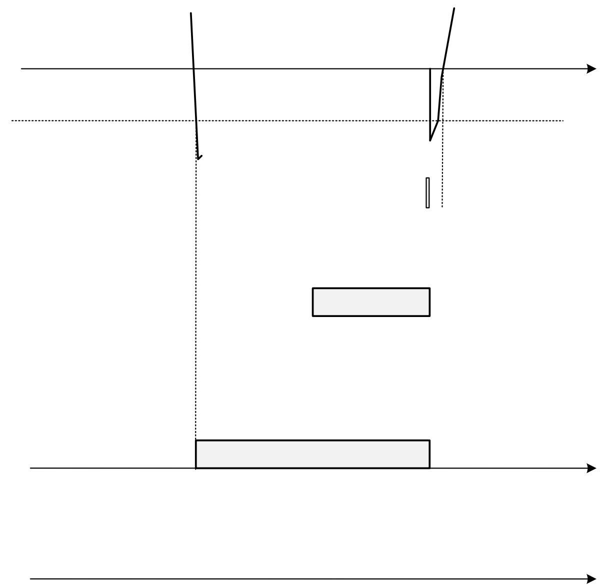

Figure 7. SR Turn-Off Algorithm

SR Skipping Mode Algorithm

As diagram shown in Figure 8, FAN6240 disables SR gate signal (SR skipping) at next cycle when previous cycle SR conduction time $V_{GS.SR}$ signal is smaller than the minimum ON time $t_{ON\_MIN.LL}$ in order reduce power consumption. This operation occurs only when the burst mode entry level of the primary side PWM controller is extremely low.

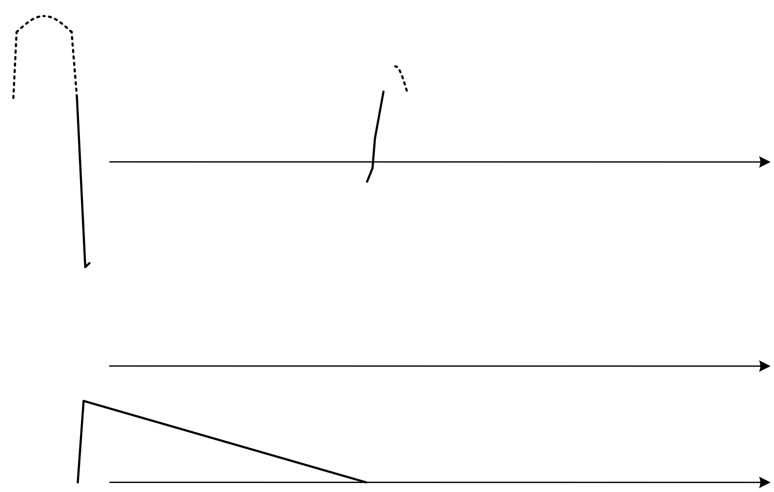

Figure 8. SR Skipping Diagram

PUBLICATION ORDERING INFORMATION

N. American Technical Support: 800−282−9855 Toll Free
USA/Canada