

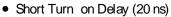
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SOT 23, 6 Lead CASE 527AJ

Features

- Support Discontinuous Conduction Modes (DCM) and Boundary Conduction Mode (BCM)
- Adaptive Turn off Dead Time Tuning for General SR MOSFET Application
- 120 V of Voltage Rating on the Drain Pin
- Charge Pump (CP) Function which Enhance SR MOSFET Voltage Driving Level through Connected a Ceramic Capacitor between Gate and CP Pin

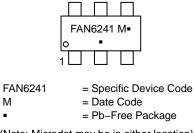


- Supporting PD General Output Voltage (VIN) Range: 3.25 V~25 V with LDO Input
- Fewest External Component Allowed
- At Green mode SR Driving Signal is Still Working under Extremely Low Power Consumption
- Small Footprint: SOT 236 pin
- These Device is Pb Free and is RoHS Compliant

Typical Applications

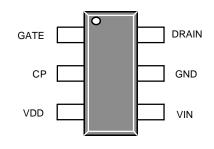
- Travel Adapter for Smart Phones, Feature Phones, and Tablet PCs
- AC DC Adapters for Portable Devices that Require CV/CC Control
- IoT Power Applications5tt

MARKING DIAGRAM



(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Operating Temperature	Package	Packing Method
FAN6241M6X	–40°C ~125°C	6-Lead, SOT23 (Pb-Free)	3000 / Tap & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

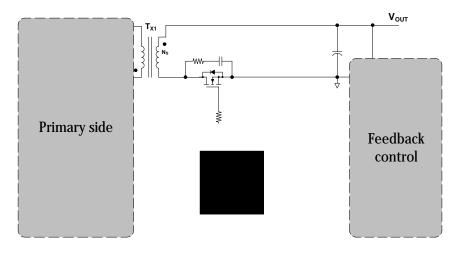


Figure 1. FAN6241M6X Typical Application Schematic

PIN FUNCTION DESCRIPTION

Pin #	Name	Description
1	GATE	Gate drive output pin
2	СР	SR gate charge pump. connect one 3.3 nF capacitor to GATE pin
3	VDD	Internal regulator 5 V output and gate drive power supply rail. Bypass with 1 μF capacitor to GND
4	VIN	LDO input, supports up to 26 V operation. An integrated 5 V LDO generates the internal VDD power supply rail for the low–voltage control circuitry
5	GND	Ground pin
6	DRAIN	Synchronous rectifier drain sense input

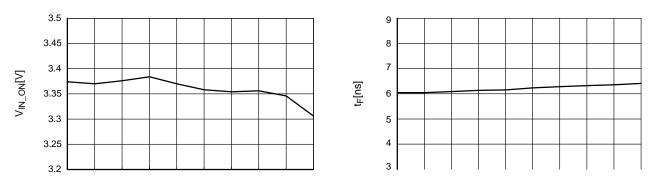
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Parameter	Symbol	Min.	Max.	Unit
V _{IN}	Power Supply Input Pin Voltage	-0.3	26	V
V _{DD}	Internal Regulator Output Pin Voltage	-0.3	6.5 V	V
V _{DRAIN}	Drain Sense Input Pin Voltage	-1	120	V
V _{GATE}	Gate Drive Output Pin Voltage	-0.3	6.5 V	V
СР	Charge pump Pin Voltage			-

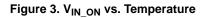
RECOMMENDED OPERATING RANGES (Note 5)

Parameter	Symbol	Min.	Max.	

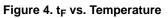
TYPICAL PERFORMANCE CHARACTERISTICS

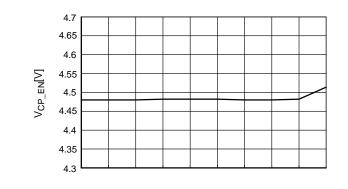


Temperature (°C)









Temperature (°C)

Figure 6. V_{CP_EN} vs. Temperature

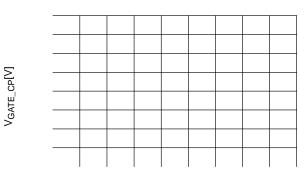
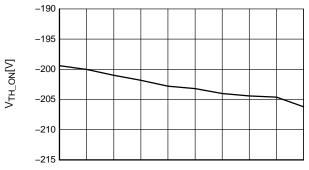


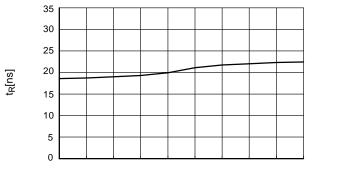


Figure 8. V_{GATE_CP} vs. Temperature

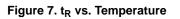


Temperature (°C)





Temperature (°C)



FUNCTIONAL DESCRIPTION

Theory of SR Control Operation

For an ideal circuit operation, the SR control algorithm of FAN6241M6X is very straightforward. FAN6241M6X controls the SR MOSFET based on the instantaneous Drain to Source voltage as illustrated in Figure 9. When the body diode starts conducting, the drain to source voltage drops below the turn on threshold ($V_{TH ON}$) which triggers the turn on of the gate. Then the product of R_{DSON}

and instantaneous SR current determines the Drain to Source voltage. When the drain to source voltage reaches the turn off threshold ($V_{TH \ OFF}$) as SR MOSFET current decreases to near zero, FAN6241M6X turns off the gate. If the turn off threshold ($V_{TH \ OFF}$) is 0 V and no stray inductance from MOSFET package and PCB layout, there is no dead time which is an ideal case.

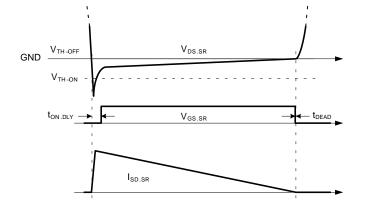


Figure 9. SR MOSFET Operation Waveforms (Ideal Case)

SR Turn On Algorithm

As the diagram shown in Figure 10, the turn on of SR GATE is triggered by the three input signals of AND gate. The first input signal is TURN_ON_ALLOW signal, which is given after $t_{OFF\ MIN}$ from the falling edge of $V_{GS.SR}$ signal. The second input is the TURN_ON_TRG signal,

which is enable after DRAIN pin voltage drops below $V_{TH \ ON}$. The third signal is t_{ARM} which allows turn on trigger only when SR drain voltage drops fast with a large slope, preventing SR from triggering by the drain resonance voltage in DCM operation.

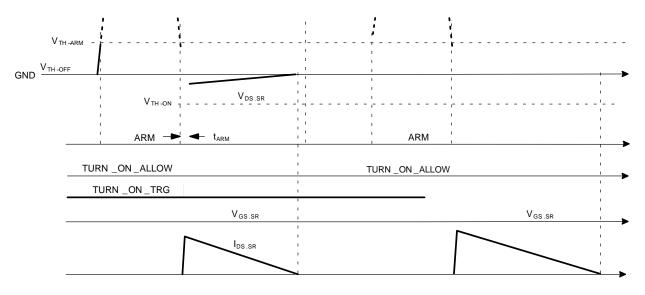


Figure 10. Turn On Algorithm

SR Turn Off Algorithm

PCB LAYOUT GUIDANCE

Printed Circuit Board (PCB) Layout

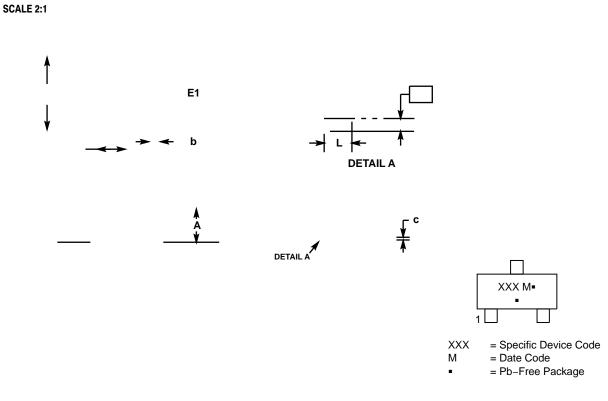
• Better PCB layout improves and minimizes excessive EMI and prevents power supply from being disrupted during ESD/Surge test. Figure 17 shows the layout guidance for low side system

IC Side:

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*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "

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