

The FAN6248 is an advanced synchronous rectifier (SR) controller

- Separate 100 V Rated Sense Inputs for Sensing the Drain and Source Voltage of each SR MOSFET
- Adaptive Parasitic Inductance Compensation to Minimize the Body Diode Conduction
- SR Current Inversion Detection under Light Load Condition
- Light Load Detection to Increase Dead Time Target
- Adaptive Minimum on Time for Noise Immunity
- Operating Voltage Range up to 30 V
- Low Start-up and Stand-by Current Consumption
- Operating Frequency Range from 25 kHz up to 700 kHz
- SOIC-8 Package
- High Driver Output Voltage of 10.5 V to Drive All MOSFET Brands to the Lowest R_{DS_ON}
- Low Operating Current in Green Mode (typ. 350 μ A)
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

Applications

- High Power Density Laptop Adapter
- High Power Density Adapter
- Large Screen LCD-TV, PDP-TV, RP-TV Power
- High-efficiency Desktop and Serv81nRP

FAN6248HC/HD/LC/LD

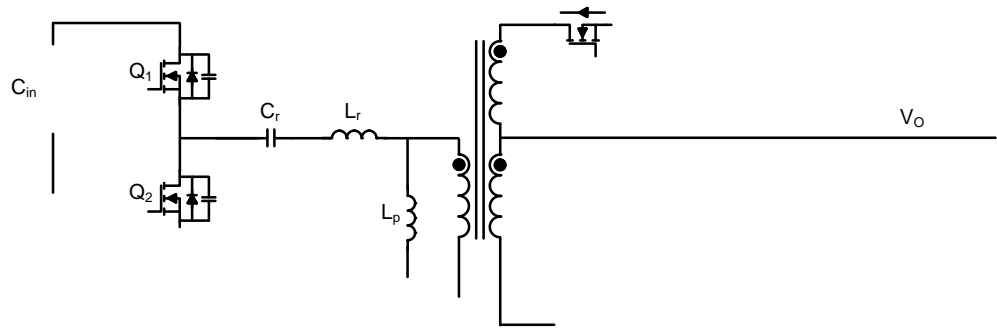


Figure 1. Typical Application Schematic of FAN6248

FAN6248HC/HD/LC/LD

PIN DESCRIPTION

Pin Number	Pin Name	Description
1	GATE1	Gate drive output for SR1
2	GND	Ground
3	VD1	Synchronous rectifier drain sense input. A $I_{OFFSET1}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET1}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
4	VS1	Synchronous rectifier source sense input for SR1
5	VS2	Synchronous rectifier source sense input for SR2
6	VD2	Synchronous rectifier drain sense input. A $I_{OFFSET2}$ current source flows out of the DRAIN pin such that an external series resistor can be used to adjust the synchronous rectifier turn-off threshold. The $I_{OFFSET2}$ current source is turned off when V_{DD} is under-voltage or when switching is disabled in green mode
7	VDD	Supply Voltage
8	GATE2	Gate drive output for SR2

ORDERING AND SHIPPING INFORMATION

Ordering Code	Device Marking	$V_{TH_OFF1} / V_{TH_OFF2}$	Package	Shipping [†]
FAN6248HCMX				

FAN6248HC/HD/LC/LD

MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Power Supply Input Pin Voltage	-0.3	30	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage	-1	100	V
V_{GATE1}, V_{GATE2}	Gate Drive Output Pin Voltage	-0.3	30	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage	-0.4	0.4	V
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)		0.625	W
J_A	Thermal Resistance (Junction-to-Ambient Thermal)		165	$^\circ\text{C}/\text{W}$
T_J	Operating Junction Temperature	-40	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-60	150	$^\circ\text{C}$
T_L	Lead Temperature (Soldering) 10 Seconds		260	$^\circ\text{C}$
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012	4	kV
		Charged Device Model, JESD22-C101	1.75	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values are with respect to the GND pin.

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
R_{JT}	Thermal Characteristics	22	$^\circ\text{C}/\text{W}$
R_{JA}	Thermal Characteristics	165	$^\circ\text{C}/\text{W}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD Pin Supply Voltage to GND (Note 2)	0	27	V
V_{D1}, V_{D2}	Drain Sense Input Pin Voltage	-0.7	100	V
V_{S1}, V_{S2}	Source Sense Input Pin Voltage	-0.4	0.4	V
T_A	Operating Ambient Temperature (Note 3)	-40	+125	$^\circ\text{C}$

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

2. Allowable operating supply voltage V_{DD} can be limited by the power dissipation of FAN6248 related to switching frequency, load capacitance and ambient temperature.
3. Allowable operating ambient temperature can be limited by the power dissipation of FAN6248 related to switching frequency, load capacitance on GATE pin and V_{DD} .

FAN6248HC/HD/LC/LD

ELECTRICAL CHARACTERISTICS ($V_{DD} = 12\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE						
V_{DD_ON}	Turn-On Threshold	V_{DD} rising	4.2	4.5	4.7	V
V_{DD_OFF}	Turn-Off Threshold	V_{DD} falling	4.0	4.2	4.4	
$V_{DD_GATE_ON}^*$	SR Gate Enable Threshold Voltage	V_{DD} rising		7.2		V

FAN6248HC/HD/LC/LD

ELECTRICAL CHARACTERISTICS ($V_{DD} = 12\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ unless otherwise specified) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
--------	-----------	------------	-----	-----	-----	------

GREEN MODE CONTROL

$t_{S_NORMAL_H}$	Switching period to be recognized as normal switching for HC and HD version		13	20	27	s
$t_{S_NORMAL_L}$	Switching period to be recognized as normal switching for LC and LD version		27	40	53	s

OUTPUT DRIVER SECTION

V_{GATE_MAX}	Gate Clamping Voltage	$12\text{ V} < V_{DD} < 25\text{ V}$	9	10.5	12	V
V_{OL}	Output Voltage Low	$V_{DD} = 12\text{ V}$, $V_{D1} = V_{D2} = 2\text{ V}$, $I_{GATE} = 50\text{ mA}$			1.5	V
V_{OH}	Output Voltage High	$V_{DD} = 12\text{ V}$, $I_{GATE} = -50\text{ mA}$	7			V
I_{SOURCE}^*	Peak Source Current for Turning On	$V_{DD} = 12\text{ V}$, $V_{GATE} = 2\text{ V}$		0.7		A
I_{SINK}^*	Peak Sink Current for Turning Off	$V_{DD} = 12\text{ V}$, $V_{GATE} = 7\text{ V}$		1.4		A
t_R^*	Rise Time	$V_{DD} = 12\text{ V}$, $C_L = 3.3\text{ nF}$, $V_{GATE} = 2\text{ V} \rightarrow 7\text{ V}$		50		ns
t_F^*	Fall Time	$V_{DD} = 12\text{ V}$, $C_L = 3.3\text{ nF}$, $V_{GATE} = 7\text{ V} \rightarrow 2\text{ V}$		30GATE		

FAN6248HC/HD/LC/LD

TYPICAL CHARACTERISTICS

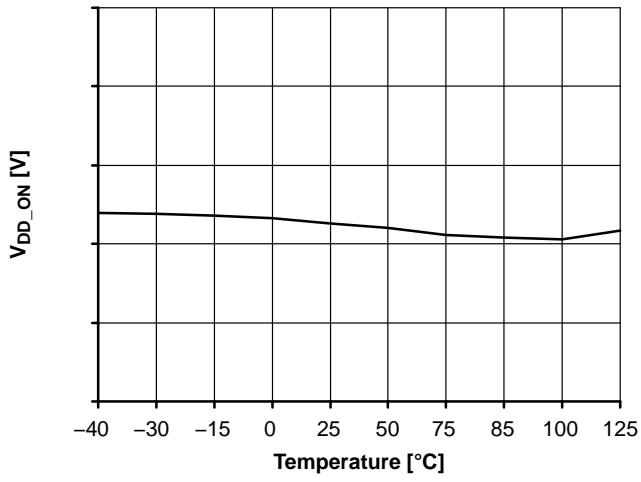


Figure 3. V_{DD_ON}

Figure 4. V_{DD_OFF}

Figure 5. I_{DD_OP}

Figure 6. I_{DD_GREEN}

Figure 7. V_{TH_HIGH}

Figure 8. V_{TH_ON}

FAN6248HC/HD/LC/LD

TYPICAL CHARACTERISTICS

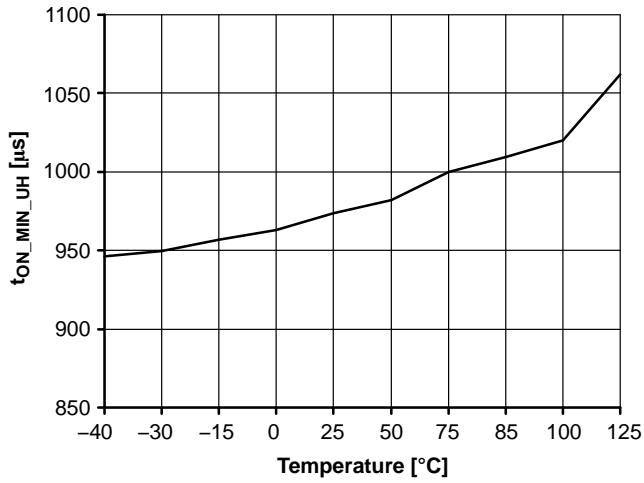


Figure 9. $t_{ON_DLY2_H}$

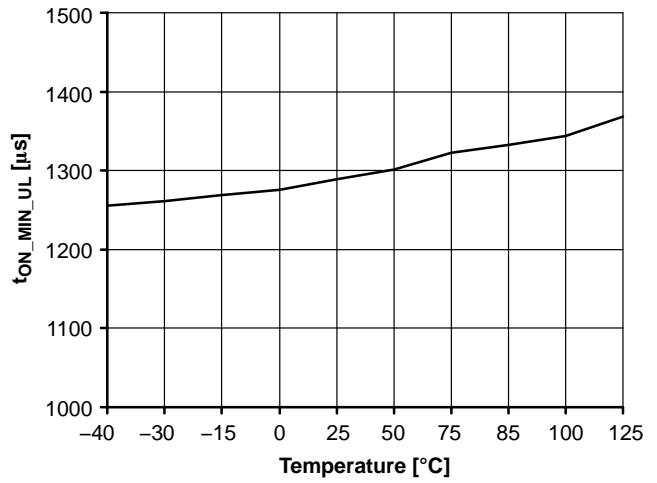


Figure 10. $t_{ON_DLY2_L}$

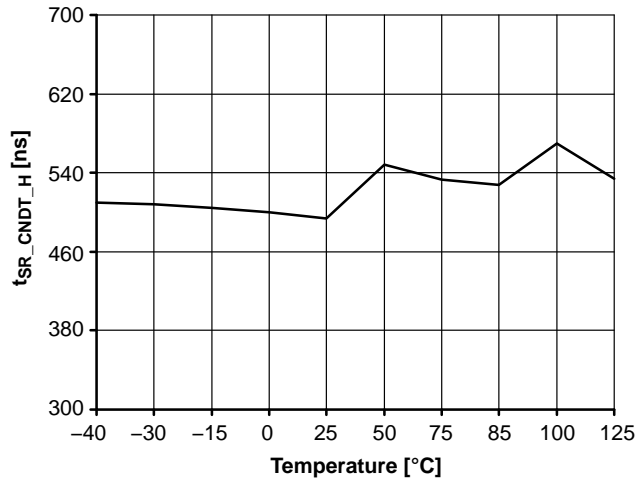


Figure 11. $t_{SR_CNDT_H}$

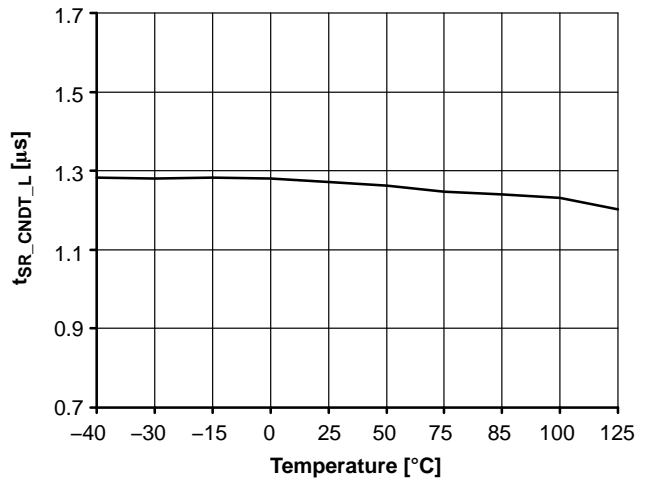


Figure 12. $t_{SR_CNDT_L}$

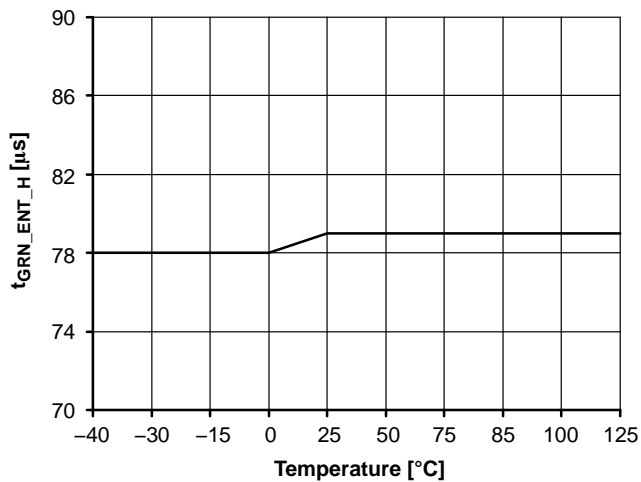


Figure 13. $t_{GRN_ENT_H}$

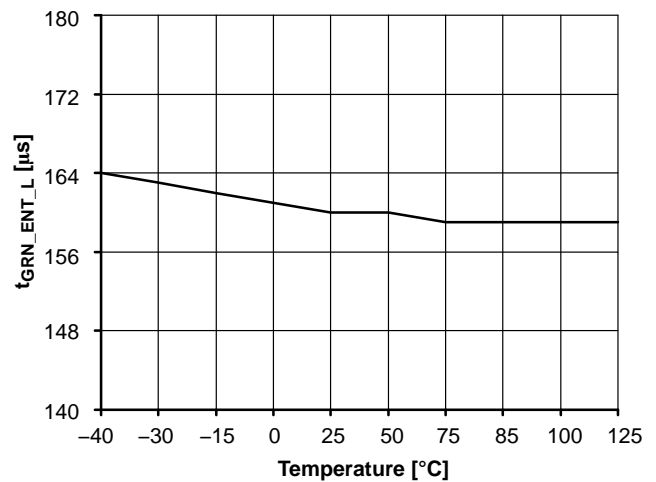


Figure 14. $t_{GRN_ENT_L}$

FAN6248HC/HD/LC/LD

TYPICAL CHARACTERISTICS

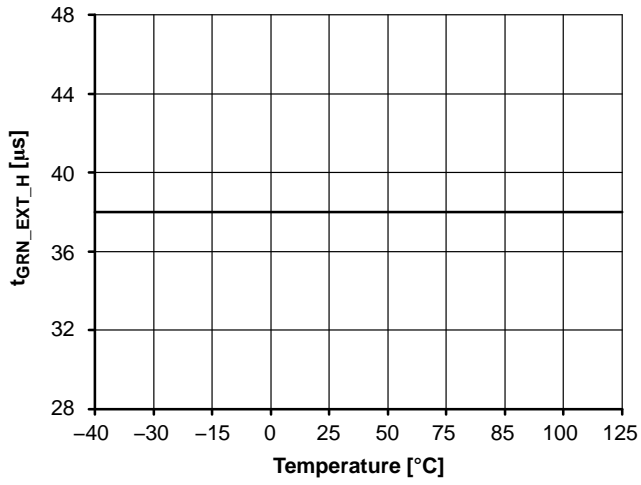


Figure 15. $t_{GRN_EXT_H}$

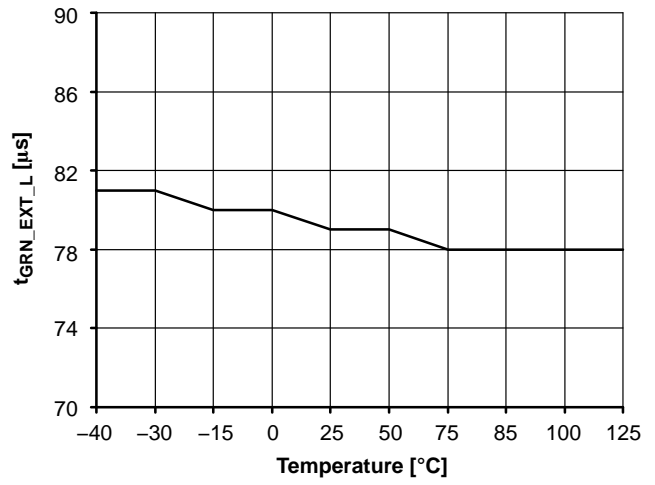


Figure 16. $t_{GRN_EXT_L}$

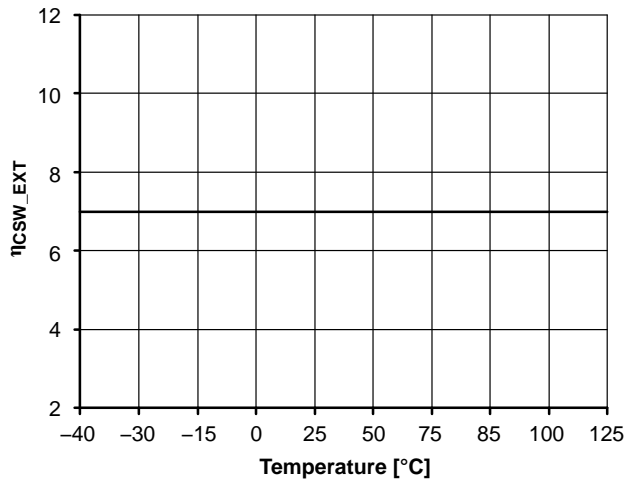


Figure 17. η_{CSW_EXT}

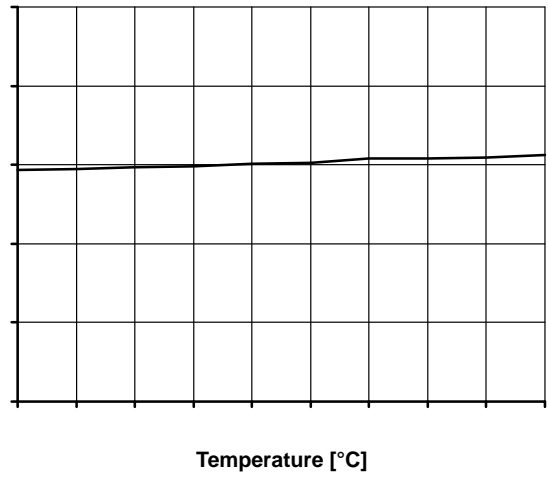


Figure 18. V_{GATE_MAX}

Figure 19. V_{OH}

Figure 20. V_{OL}

Basic Operation Principle

FAN6248 controls the SR MOSFET based on the instantaneous drain-to-source voltage sensed across *DRAIN* and *SOURCE* pins. Before SR gate is turned on, SR body diode operates as the conventional diode rectifier. Once the body diode starts conducting, the drain-to-source voltage drops below the turn-on threshold voltage V_{TH_ON} which triggers the turn-on of the SR gate. Then the drain-to-source voltage is determined by the product of turn-on resistance R_{ds_on} of SR MOSFET and instantaneous SR current. When the drain-to-source voltage reaches the turn-off threshold voltage V_{TH_OFF} as SR MOSFET current decreases to near zero, FAN6248 turns off the gate. If a SR dead time is larger or smaller than the dead time regulation target t_{DEAD} , FAN6248 adaptively changes internal offset voltage to compensate the dead time. In addition, to prevent cross conduction SR operation, FAN6248 has 200 ns of turn-on blocking time just after alternating SR gate is turned off.

SR Turn-off Algorithm

Since a SR turn-off method determines SR conduction time and stable SR operation, the SR turn-off method is one of important feature of SR controllers. The SR turn-off method can be

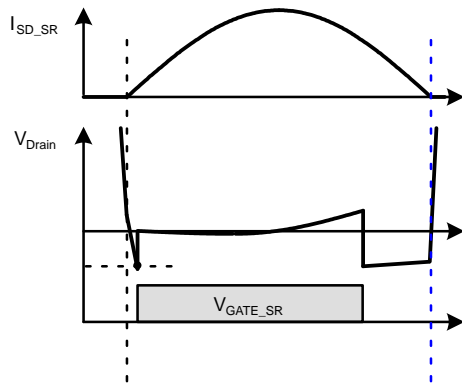


Figure 23. Premature SR Gate Turn-off
($T_{DEAD} > t_{DEAD_H}$)

Light Load Detection (LLD)

To guarantee stable operation under light load condition, FAN6248 adopts a light load detection function. The modulation current I_{OFFSET} is mainly used for the adaptive dead time control. When the output load is heavy, I_{OFFSET_STEP} declines due to large di/dt in the secondary side current to maintain 280 ns of t_{DEAD} in FAN6248HC(D). On the contrary, I_{OFFSET_STEP} increases at light load condition by small di/dt of SR current. FAN6248 can detect light load condition by using this I_{OFFSET_STEP} as shown in Figure 27. When SR turn-off threshold voltage is V_{TH_OFF1} and the modulation current is higher than I_{OFFEST_STEP8} , the light load detection is triggered. In this mode, dead time target becomes to 320 ns of t_{DEAD_LIGHT} in FAN6248HC(D) and 360 ns in FAN6248LC(D) version.

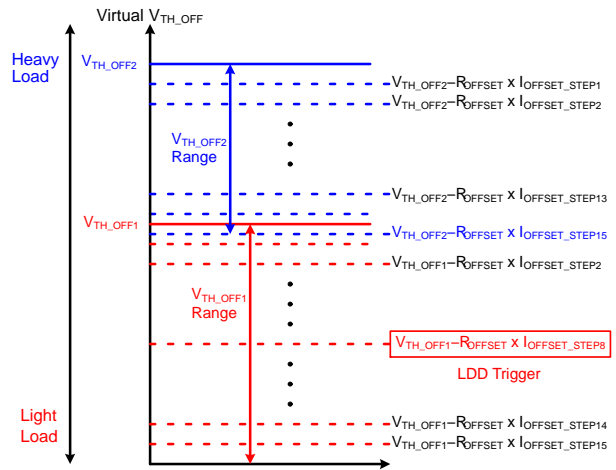


Figure 27. Light Load Detection

Green Mode

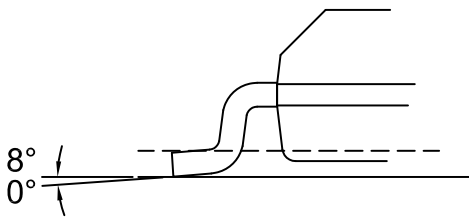
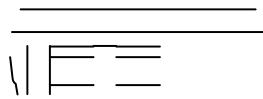
When the power supply system operates at very light load condition, FAN6248 disables SR operation and enters into green mode operation. Once FAN6248 is in the green mode, all the major blocks are disabled to minimize the operating current. When V_{DS_SR} has no switching operation longer than t_{GRN_ENT} during the burst mode of the primary side LLC controller, the green mode is enabled after $t_{GRN_ENT_DBNC}$ of debounce time. After then, FAN6248 exits the green mode when the non-switching time in the burst mode is less than $t_{GRN_EXT_H}$ or 7 consecutive switching cycles are detected as shown in Figure 28.



Figure 28. Green Mode Exit

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



onsemi, **onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi**
