# Highly Integrated Secondary-Side Adaptive USB Type-C Charging Controller with USB-PD with SR Embedded

# FAN6390MPX

The FAN6390MPX is a highly integrated, secondary−side power adaptor controller supporting USB Type−C and USB Power Delivery 2.0/3.0. It includes a fully autonomous USB PD state machine which is fully compliant with the latest USB PD 3.0 specification, minimizing design time and cost. Support for the latest Programmable Power Supply (PPS) rules allows for control of voltages from 3.3 V to 21 V and current limits from 1 A to 3 A to meet a wide range of applications and power levels.

To minimize BOM count, the FAN6390MPX includes internal synchronous rectifier control, an NMOS gate driver for VBUS load switch control, as well as Constant Voltage (CV) and Constant Current (CC) control blocks with adjustable internal references. To ensure proper operation of the adaptor, various protections are integrated into the controller including output over−voltage protection, under−voltage protection, external over−temperature protection via NTC, internal over−temperature protection, CC over voltage protection and Cable Fault Protection.

**Features**

- USB Type−C Rev 1.3 Compatible
- Support 60 W Output Profile
- (PDO: 5 V, 9 V, 15 V, 20 V. APDO: 9 V, 15 V, 20 V)
- 

**Figure 1. Application Schematic**

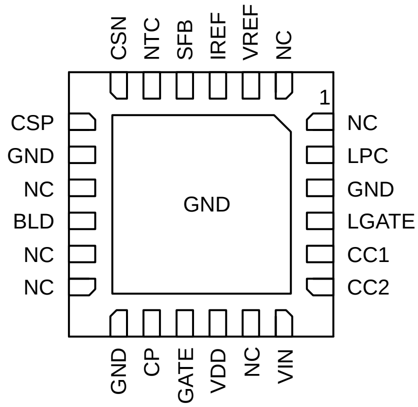



**Figure 3. Pin Connections (Bottom View)**

**Table 1. PIN FUNCTION DESCRIPTION(MLP44)**

| Pin # | Pin Name | Description |
|---|---|---|
| 1 | NC | No connection |
| 2 | LPC | SR control input signal. This pin is used to detect the voltage on the secondary winding during the on time period of the primary MOSFET |
| 3 | GND | Ground |
| 4 | LGATE | Load switch gate drive signal. This pin is tied to the gate of the load switch |
| 5 | CC1 | Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable. |
| 6 | CC2 | Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD when applicable. |
| 7 | VIN | Output voltage (Input voltage to the FAN6390MPX). This pin is tied to the output of the adapter to monitor its output voltage and supply internal bias. |
| 8 | NC | No connection |
| 9 | VDD | Internal supply voltage. This pin is connected to an external capacitor. |
| 10 | GATE | Gate drive output. Totem−pole output to drive the external SR MOSFET. |
| 11 | CP | SR gate charge pump |
| 12 | GND | Ground |
| 13 | NC | No connection |
| 14 | NC | No connection |
| 15 | BLD | Bleeder pin. This pin is tied to VBUS after the load switch to discharge VBUS. |
| 16 | NC | No connection |
| 17 | GND | Ground |
| 18 | CSP | Current sensing amplifier positive terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace. |
| 19 | CSN | Current sensing amplifier negative terminal. Connect this pin directly to the negative end of the current sense resistor with a short PCB trace. |
| 20 | NTC | This pin is used for external temperature detection and protection |
| 21 | SFB | Secondary Feedback. Common output of the dual OTA open drain operation amplifiers. Typically an opto−coupler is connected to this pin to provide feedback signal to the primary side PWM controller |
| 22 | IREF | Constant Current Amplifying Signal. The voltage level on this point is the amplified current sense signal. This pin is tied to the internal CC loop amplifier’s non−inverting input terminal |
| 23 | VREF | Output Voltage Sensing Voltage. This pin is used for CV regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage resistor divider. |
| 24 | NC | No connection |

**Table 2. MAXIMUM RATINGS** (Notes 1, 2)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| VIN Pin Input Voltage | $V_{IN}$ | –0.3 to 26 | V |
| SFB Pin Input Voltage | $V_{SFB}$ | –0.3 to 26 | V |
| BLD Pin Input Voltage | $V_{BLD}$ | –0.3 to 26 | V |
| LGATE Pin Input Voltage | $V_{LGATE}$ | –0.3 to 31 | V |
| VDD Pin Input Voltage | $V_{DD}$ | –0.3 to 6 | V |
| IREF Pin Input Voltage | $V_{IREF}$ | –0.3 to 6 | V |
| VREF Pin Input Voltage | $V_{VREF}$ | –0.3 to 6 | V |
| CSP Pin Input Voltage | $V_{CSP}$ | –0.3 to 6 | V |
| CSN Pin Input Voltage | $V_{CSN}$ | –0.3 to 6 | V |

**Table 5. ELECTRICAL CHARACTERISTICS**

$V_{IN}$ = 5 V, LPC = 1.25 V, LPC width = 2 μs at $T_J$ = −40~125°C, $F_{LPC}$ = 100 kHz, unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **VDD SECTION** | | | | | | |
| Turn−On Valid Threshold Voltage | | $V_{DD-valid}$ | 2.6 | | | V |
| VIN Operating Voltage at 20V | $V_{IN}$ = 20 V, $I_{VDD}$ = 0 mA | $V_{DD}$ | 4.750 | 5.125 | 5.500 | V |
| VDD Source Current | $V_{IN}$ = 3.3 V, $V_{DD}$ = 2.9 V | $I_{DD}$ | 10 | | | mA |
| **VIN SECTION** | | | | | | |
| Continuous Operating Voltage (Note 5) | | $V_{IN-OP}$ | | | 22.5 | V |
| Operating Supply Current at 5 V | $V_{IN}$ = 5 V, $V_{CS}$ = −25 mV, Rcs = 5 mΩ | $I_{IN-OP-5V}$ | | | 10 | mA |
| Operating Supply Current at 20 V (Note 5) | $V_{IN}$ = 20 V, $V_{CS}$ = −25 mV, Rcs = 5 mΩ | $I_{IN-OP-20V}$ | | 8 | | mA |
| Turn−On Threshold Voltage | $V_{IN}$ Increases | $V_{IN-ON}$ | 2.9 | 3.2 | 3.4 | V |
| Turn−Off Threshold Voltage | $V_{IN}$ Decreases after $V_{IN}$ = $V_{IN-ON}$ | $V_{IN-OFF}$ | 2.805 | 2.875 | 3.005 | V |
| Green Mode Operating Supply Current | $V_{IN}$ = 5.2 V (default), $V_{CS}$ = 0 mV excluding $I_{P-CC1}$ and $I_{P-CC2}$ | $I_{IN-Green}$ | | | 1.3 | mA |
| **VIN UVP SECTION** | | | | | | |
| Ratio $V_{IN}$ Under−Voltage−Protection to $V_{IN}$ | Whole output mode, $V_{CS}$ = 0 mV | $K_{IN-UVP}$ | 65 | 70 | 75 | % |
| CC Mode UVP Debounce Time | | $t_{D-VIN-UVP}$ | 45 | 60 | 75 | ms |
| UVP Blanking Time during Mode Change from Lower Vout to Higher Vout | Whenever does mode change from lower Vout to higher Vout | $t_{BNK-UVP}$ | 160 | 200 | 240 | ms |
| **VIN OVP SECTION** | | | | | | |
| Ratio $V_{IN}$ Over−Voltage−Protection to $V_{IN}$ | Whole output mode, $V_{CS}$ = 0 mV | $K_{IN-OVP}$ | 116.0 | 121.5 | 127.0 | % |
| $V_{IN}$ Maximum Over−Voltage−Protection | | $V_{IN-OVP-MAX}$ | 23.5 | | | |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
$V_{IN}$ = 5 V, LPC = 1.25 V, LPC width = 2 μs at $T_J$ = −40~125°C, $F_{LPC}$ = 100 kHz, unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **TYPE C SECTION** | | | | | | |
| $CC_1$ Pin Over−Voltage Protection | | | | | | |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)

$V_{IN}$ = 5 V, LPC = 1.25 V, LPC width = 2 μs at $T_J$ = −40~125°C, $F_{LPC}$ = 100 kHz, unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **LPC SECTION** | | | | | | |
| SR Enabled Threshold Voltage @ Low−Line | $V_{LPC-HIGH-L-12V} = V_{LPC-TH-L-12V} / 0.875$ | $V_{LPC-HIGH-L-20V}$ | 0.897 | 0.981 | 1.065 | V |
| Low−to−High Line Threshold Voltage on LPC Pin | Spec. = (0.70 + 0.02 * $V_{IN}$) * 2, $V_{IN}$ = 5 V | $V_{LINE-H-5V}$ | 1.46 | 1.60 | 1.74 | V |
| High−to−Low Line Threshold Voltage on LPC Pin | Spec. = (0.65 + 0.02 * $V_{IN}$) * 2, $V_{IN}$ = 5 V | $V_{LINE-L-5V}$ | 1.37 | 1.50 | 1.63 | V |
| Line Change Threshold Hysteresis (Note 5) | $V_{LINE-HYS-5V} = V_{LINE-H-5V} - V_{LINE-L-5V}$ | $V_{LINE-HYS-5V}$ | | 0.1 | | V |
| Low−to−High Line Threshold Voltage on LPC Pin | Spec. = (0.70 + 0.02 * $V_{IN}$) * 2, $V_{IN}$ = 9 V | $V_{LINE-H-9V}$ | 1.62 | 1.76 | 1.90 | V |
| High−to−Low Line Threshold Voltage on LPC Pin | Spec. = (0.65 + 0.02 * $V_{IN}$) * 2, $V_{IN}$ = 9 V | | | | | |

**Table 5. ELECTRICAL CHARACTERISTICS** (continued)
$V_{IN}$ = 5 V, LPC = 1.25 V, LPC width = 2 μs at $T_J$ = −40~125°C, $F_{LPC}$ = 100 kHz, unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BMC TRANSMITTER NORMATIVE REQUIREMENTS** | | | | | | |
| Unit Internal | 1/fBitRate | $t_{UI}$ | 3.03 | 3.33 | 3.70 | μs |
| Rise Time | $C_{VDD}$ = 4.7 F | $t_{Rise-TX}$ | 300 | 500 | 700 | ns |
| Fall Time | $C_{VDD}$ = 4.7 μF | $t_{Fall-TX}$ | 300 | 500 | 700 | ns |
| Transmitter Output Impedance | Transmitter output impedance at Niquist frequency of USB2.0 low speed (750 kHz) while Source driving the CC line | zDriver | 33 | | 75 | Ω |
| Transitions for Signal Detect | | $n_{TransitionCount}$ | 3 | | | |
| Time Window for Detecting Non−idle | | $t_{TransitionWindow}$ | 12 | | 20 | μs |
| Rx bandwidth Limiting Filter (Digital or Analog) | | $t_{RxFilter}$ | 100 | | | ns |
| Receiver Input Impedance | | zBmcRx | 1 | | | MΩ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
5. Guaranteed by Design

## TYPICAL CHARACTERISTICS

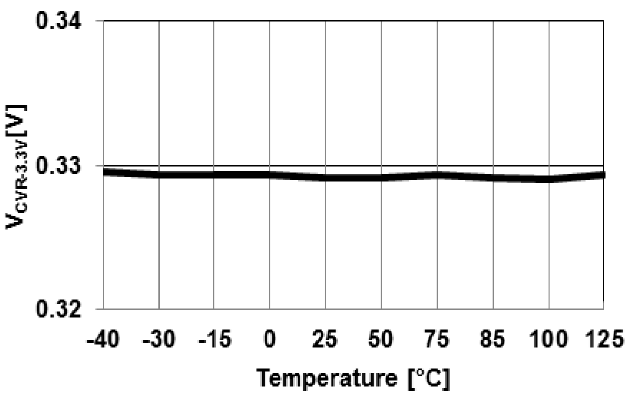



Figure 4. $V_{CVR\ 3.3V}$ vs. Temperature

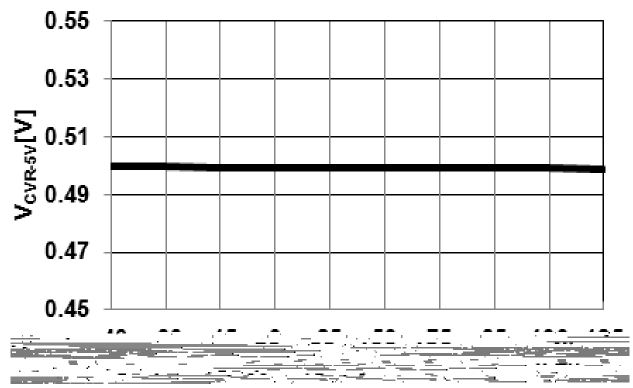



Figure 5. $V_{CVR\ 5V}$ vs. Temperature

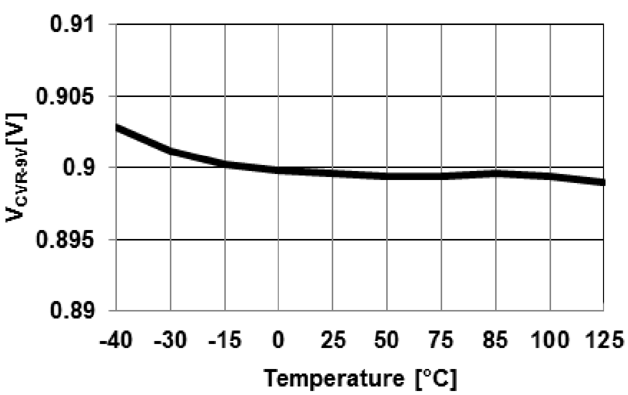



Figure 6. $V_{CVR\ 9V}$ vs. Temperature

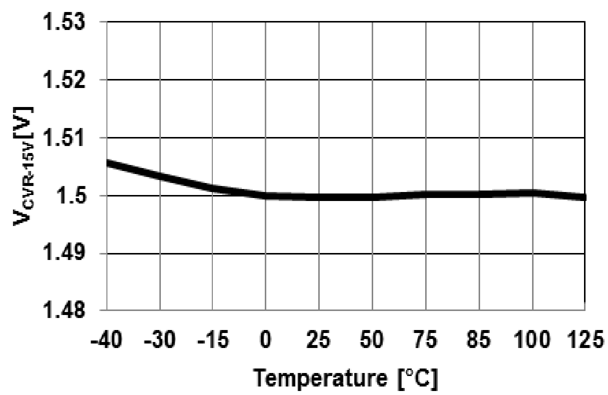



Figure 7. $V_{CVR\ 15V}$ vs. Temperature

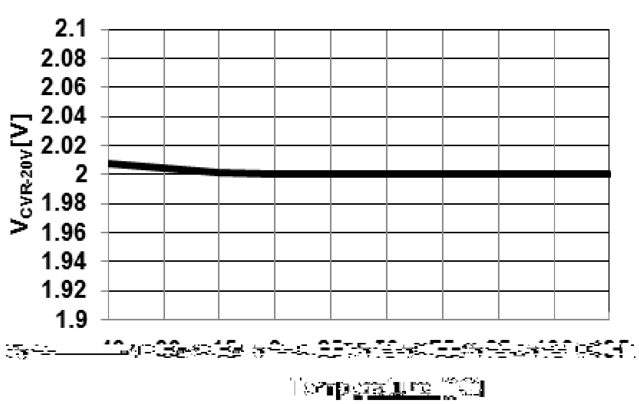



Figure 8. $V_{CVR\ 20V}$ vs. Temperature

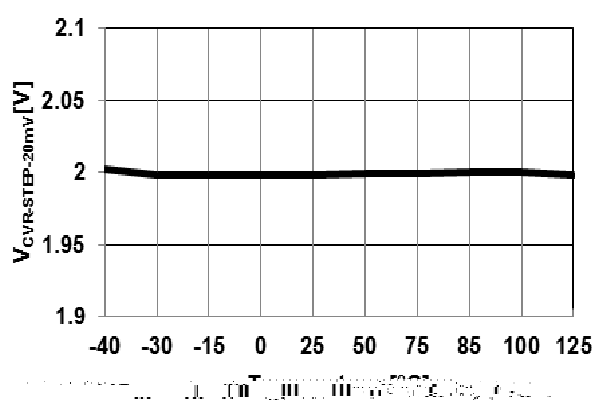



Figure 9. $V_{CVR\ STEP\ 20mV}$ vs. Temperature

**TYPICAL CHARACTERISTICS** (Continued)

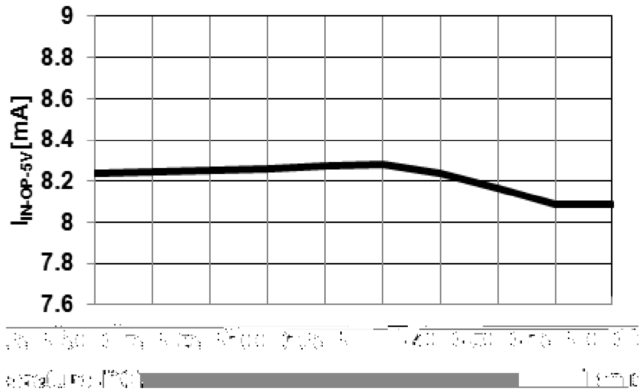



Figure 10. $I_{IN\_OP\_5V}$ vs. Temperature

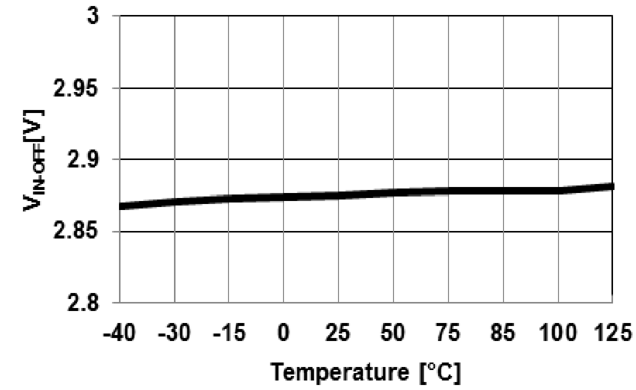



Figure 11. $V_{IN\_OFF}$ vs. Temperature

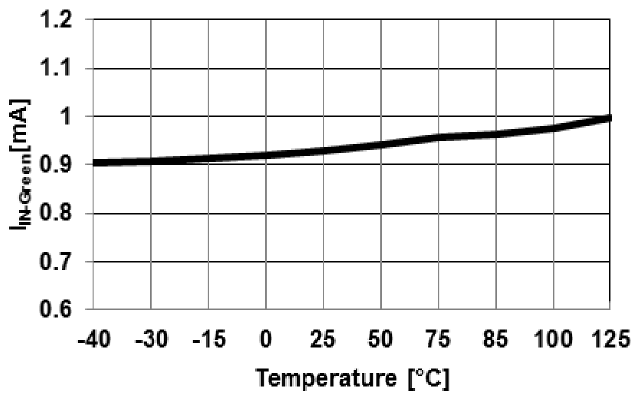



Figure 12. $I_{IN\_Green}$ vs. Temperature

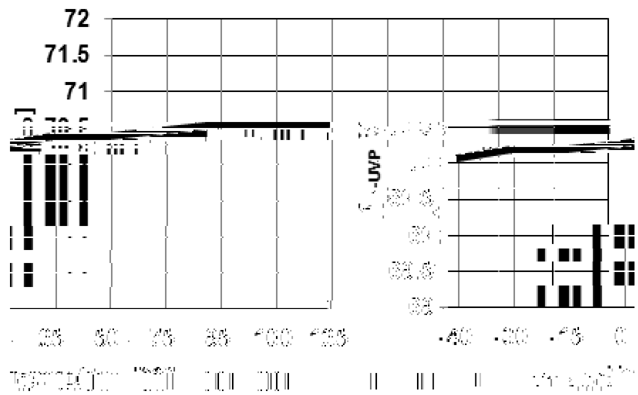



Figure 13. $K_{IN\_UVP}$ vs. Temperature

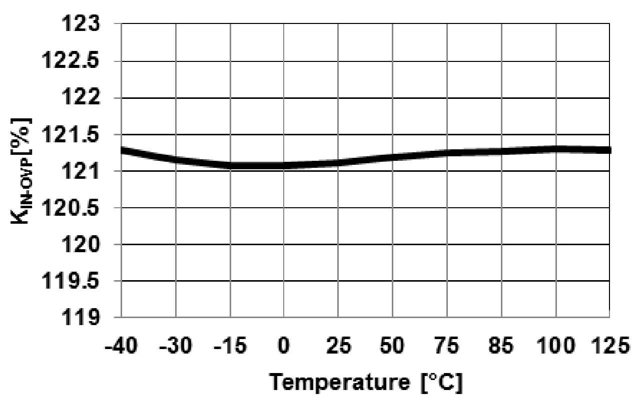



Figure 14. $K_{IN\_OVP}$ vs. Temperature

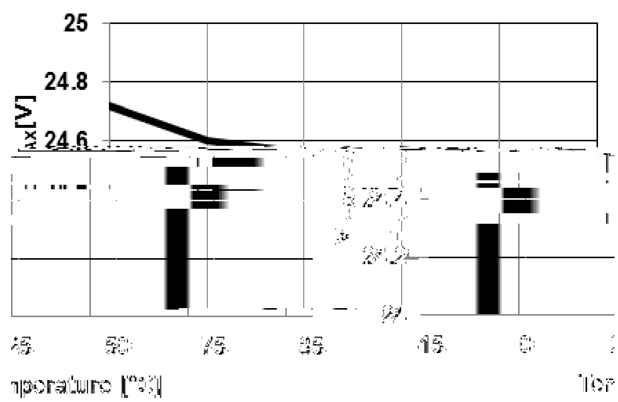



Figure 15. $V_{IN\_OVP\_MAX}$ vs. Temperature

## TYPICAL CHARACTERISTICS (Continued)

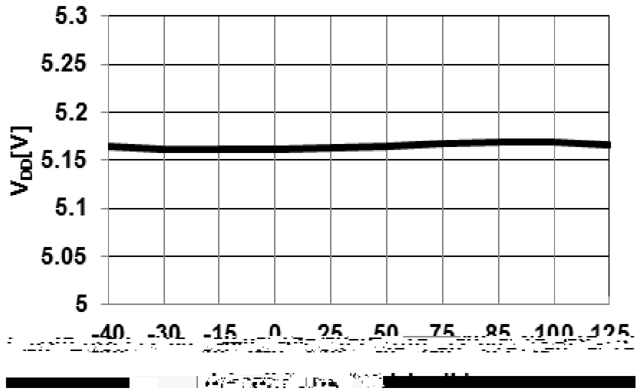



Figure 16. $V_{DD}$ vs. Temperature

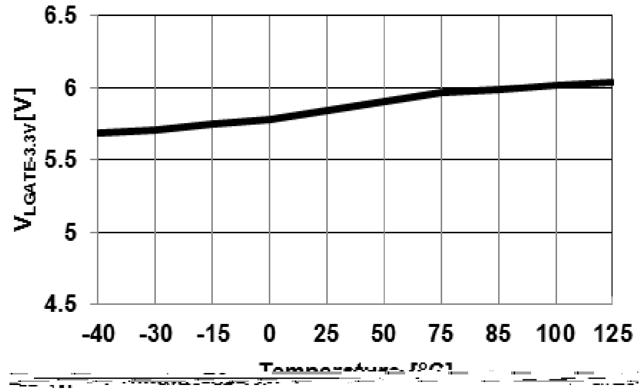



Figure 17. $V_{LGATE\_3.3V}$ vs. Temperature

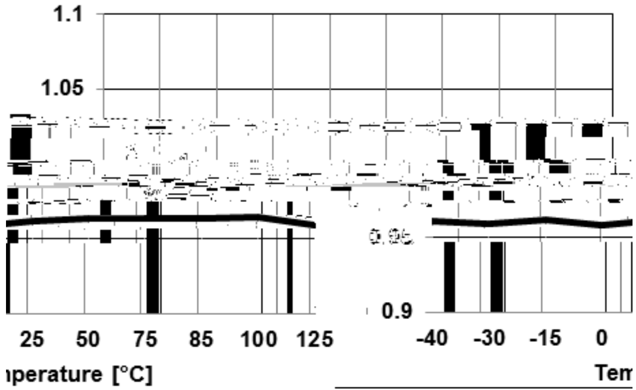



Figure 18. $I_{CS\_1.00A}$ at $V_{IN}$ = 20 V vs. Temperature

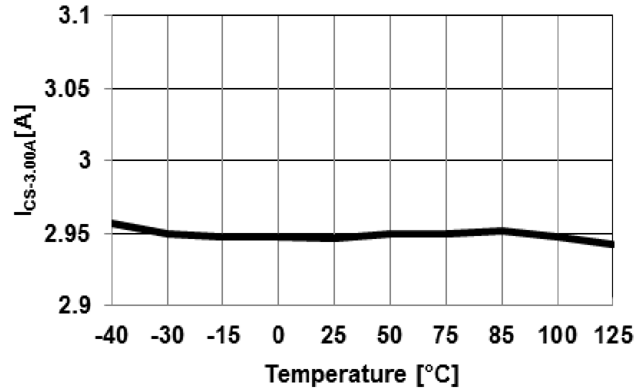



Figure 19. $I_{CS\_3.00A}$ at $V_{IN}$ = 20 V vs. Temperature

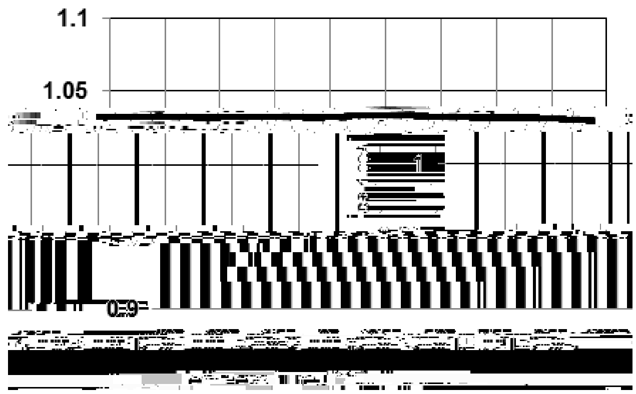



Figure 20. $I_{CS\_1.00A}$ at $V_{IN}$ = 3.3 V vs. Temperature

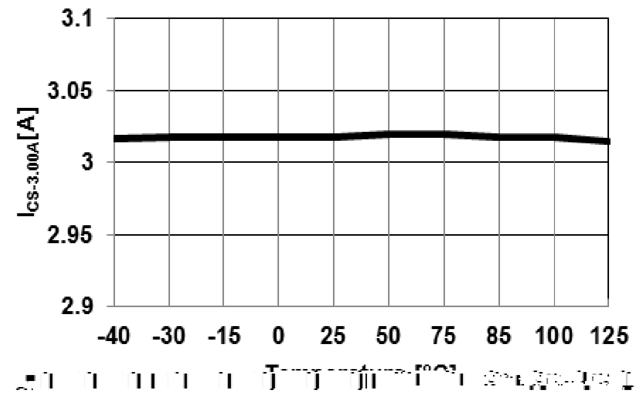
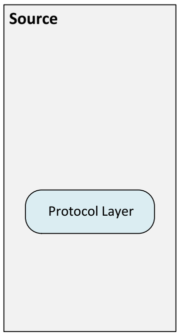


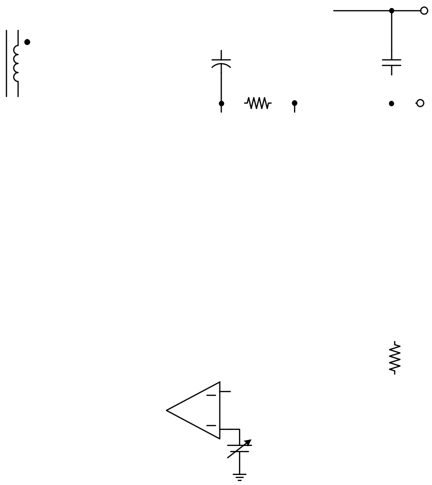

Figure 21. $I_{CS\_3.00A}$ at $V_{IN}$ = 3.3 V vs. Temperature

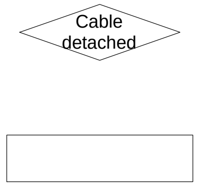
| | | | |
|---|---|---|---|
| Internal RES ratio= 1/$Ratio_{RRES}$ | 00: 0.14 (for $N_P/N_S$ = 7.5~10)<br>01: 0.18 (for $N_P/N_S$ = 9.5~13)<br>10: 0.11 (for $N_P/N_S$ = 6.5~7.5)<br>11: 0.10 (for $N_P/N_S$ = 5~6.5)<br>Note: $N_P$ and $N_S$ are primary and secondary transformer turns | “10” is selected. | |
| Cable Compensation for PDO | ratio= 1/Rt.I.5789 .np46.59Sa(13cO1: 0.14 (f)Tj0 -1.55.395 668.92 .90709 42.236 ref59.754 5581.556 .9.641 ..9071 refBBT8 0 0 | | |

### USB Type C Support

The USB Type


Source
Protocol Layer




Cable
detached

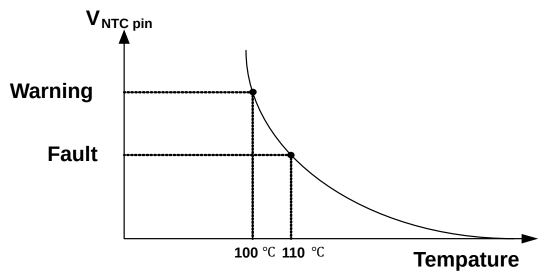



Figure 38. NTC vs. Temperature

**Table 14. EXTERNAL OVER TEMPERATURE PROTECTION THRESHOLD**

| Message | Threshold | Setting |
|---|---|---|
| Warning | 100°C | $R_p$=20k Ω@25°C<br>$R_{NTC}$=100k Ω±1%@25°C<br>($B_{25/50}$=4300 k±1%) |
| Fault | 110°C | |

### Internal Over Temperature Protection

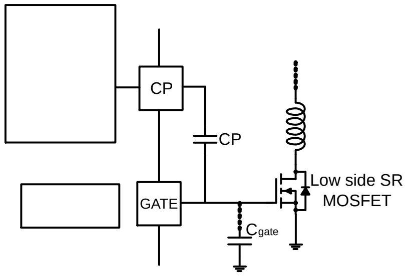
The FAN6390MPX also implements internal over temperature protection through an internal temperature sensing circuit. Once the internal temperature exceeds the fault protection threshold of 140℃, the FAN6390MPX sends an Alert indicating an Fault and the device will enter Auto Restart Mode.

### Cable Fault Protection

In order to avoid the cable line melting caused by the pollution such as low impedance across ground to BUS. FAN6390MPX implements USB BUS line impedance detection. Before $t_{CCDebounce}$ which is debonce time detecting cable attach status, load switch is not turned on and FAN6390MPX start Bus line impedance detecting. If output is low impedance under 2 kΩ, FAN6390MPX will enter Auto Restart Mode so the load switch will not turn on. No power deliver to output ensure system safety.

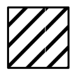
### CC Signal Over Voltage Protection

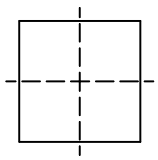
The USB Type−C CC pins are located physically close to VBUS on the connector and could be shorted to VBUS via conductive materials as shown in Figure 39 This not only impacts PD protocol communication, but possibly damages the CC pins because of high VBUS voltages. The

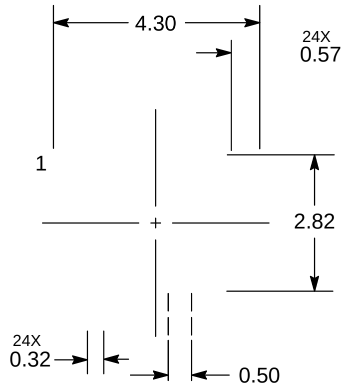

CP
CP
GATE
Low side SR
MOSFET
$C_{gate}$

**WQFN24, 4x4, 0.5P**
CASE 510BE
ISSUE O

DATE 02 OCT 2013








DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting