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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.



Typical Application Circuit

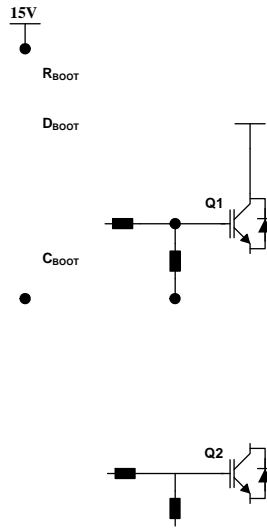
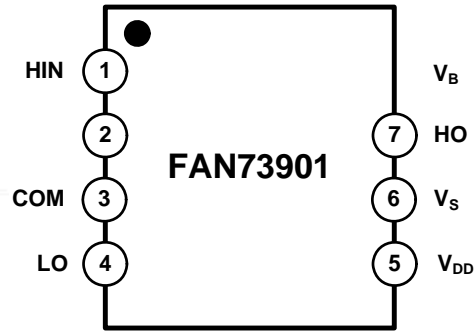


Figure 1. Application Circuit for Half-Bridge

Internal Block Diagram

Figure 2. Functional Block Diagram

Pin Configuration



FAN73901 Rev.01

Figure 3. Pin Assignments (Top View)

Pin Definitions

Pin #	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-Side Driver Return
4	LO	Low-Side Driver Output
5	V_{DD}	Low-Side and Logic Part Supply Voltage
6	V_S	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	V_B	High-Side Floating Supply

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A



Typical Characteristics



Figure 4. Turn-on Propagation Delay vs. Temperature

Figure 5. Turn-off Propagation Delay vs. Temperature

Figure 6. Turn-on Rise Time vs. Temperature

Figure 7. Turn-off Fall Time vs. Temperature

Typical Characteristics (Continued)

Figure 10. Quiescent V_{DD} Supply Current vs. Temperature

Figure 11. Quiescent V_{BS} Supply Current vs. Temperature

Figure 12. Operating V_{DD} Supply Current vs. Temperature

Figure 13. Operating V_{BS} Supply Current vs. Temperature

Figure 14. V_{DD}

Typical Characteristics (Continued)

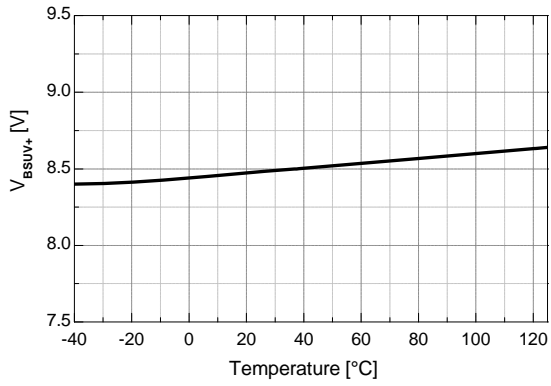


Figure 16. V_{BS} UVLO+ vs. Temperature



Figure 17. V_{BS} UVLO- vs. Temperature

Figure 18. High-Level Output Voltage vs. Temperature

Figure 19. Low-Level Output Voltage vs. Temperature

Figure 20. Logic High Input Voltage vs. Temperature

Figure 21. Logic Low Input Voltage vs. Temperature

Typical Characteristics (Continued)

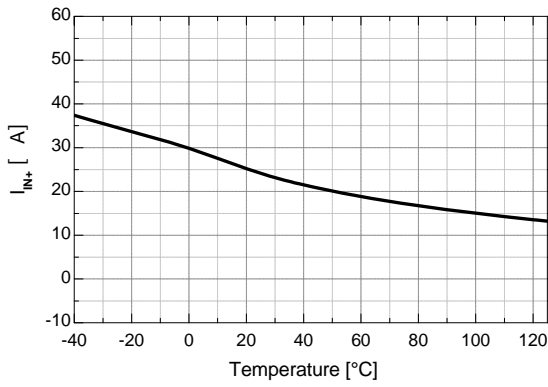


Figure 22. Logic Input High Bias Current vs. Temperature

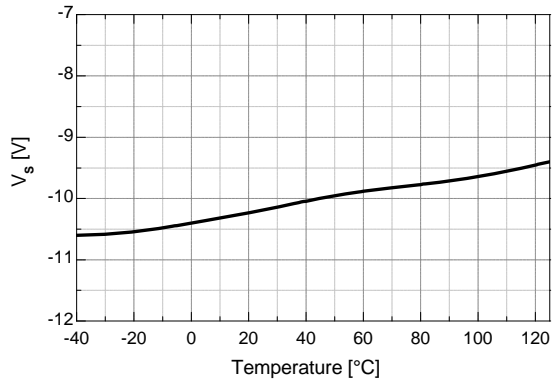


Figure 23. Allowable Negative V_S Voltage vs. Temperature

Switching Time Definitions

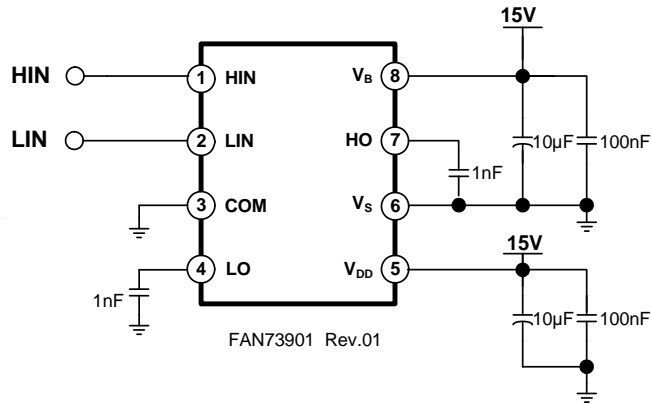


Figure 24. Switching Time Test Circuit

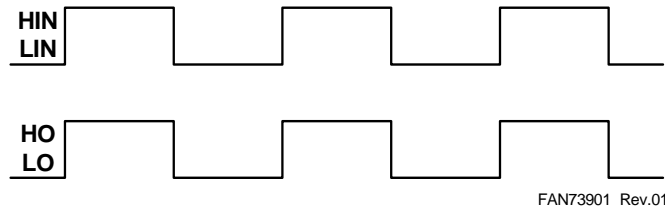
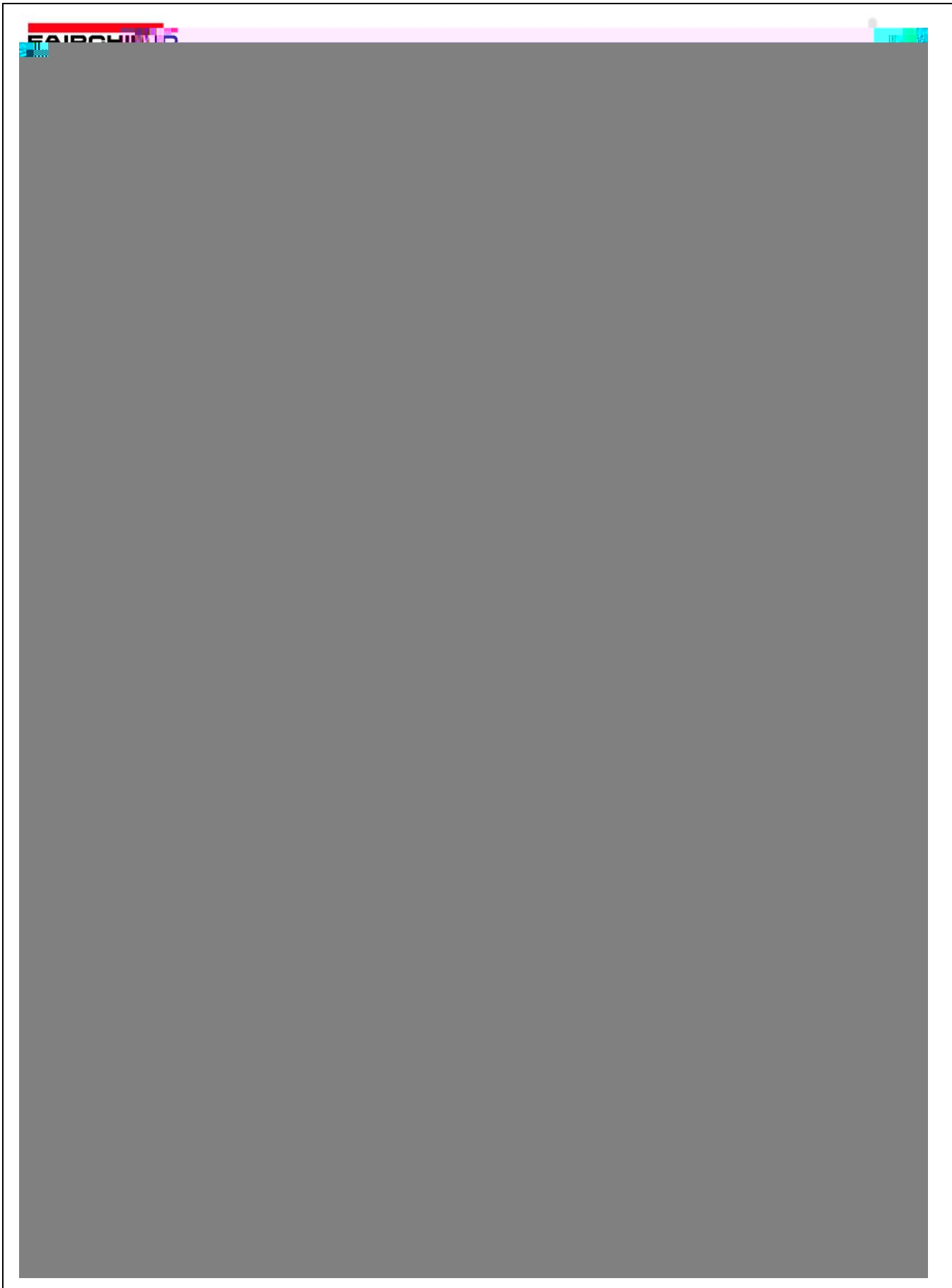


Figure 25. Input / Output Timing Diagram

Figure 26. Switching Time Waveform Definitions

Figure 27. Delay Matching Waveform Definitions



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